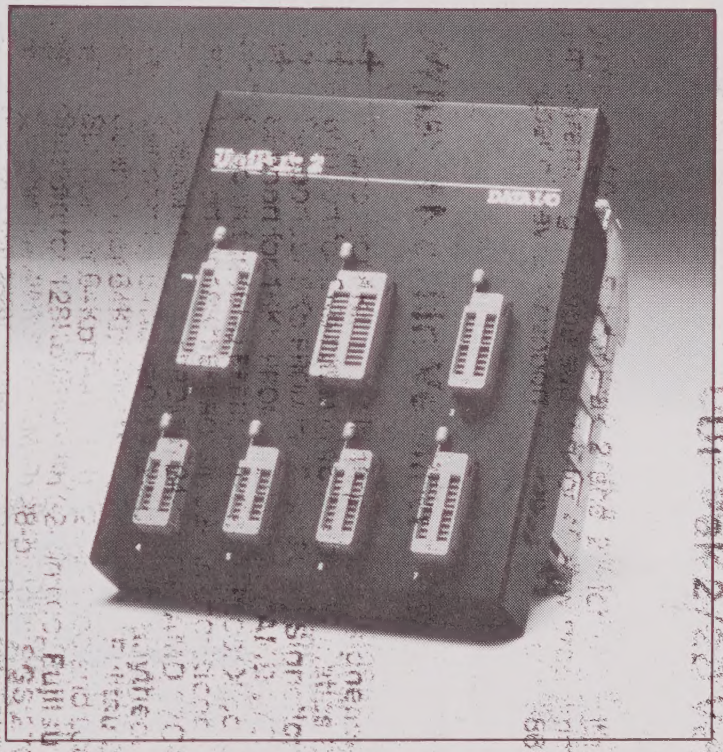
DATA I/O



UniPak 2™

981-0001-003

JUNE 1987

Copyright © Data I/O Corporation, 1987. All rights reserved.

Data I/O has made every attempt to ensure that the information in this document is accurate and complete. However, Data I/O assumes no liability for errors, or for any damages that result from use of this document or the equipment which it accompanies.

Data I/O reserves the right to make changes to this document without notice at any time.

NOTE

Before using the UniPak 2™, read section 1.2 for programmer mainframe compatibility information.

Applies to: Engineering Part Number 950-0059-013 and up

TABLE OF CONTENTS

SECTION 1. INTRODUCTION

1.1 OVERVIEW 1-1
1.2 PROGRAMMER COMPATIBILITY 1-1
1.3 APPLICATIONS 1-2
1.4 SPECIFICATIONS 1-2
1.5 FIELD APPLICATION SUPPORT 1-2
1.6 WARRANTY 1-2
1.7 SERVICE 1-2
1.8 ORDERING 1-2

SECTION 2. INSTALLATION

2.1 INSPECTION 2-1
2.2 UniPak 2™ INSTALLATION 2-1
2.3 UniPak 2™ REMOVAL 2-1
2.4 REPACKING FOR SHIPMENT 2-1

SECTION 3. OPERATION

3.1 OVERVIEW 3-1
3.2 POWER UP 3-2
3.3 POWER DOWN 3-2
3.4 BASIC OPERATION 3-2
3.4.1 Load RAM With Data From Master Device 3-3
3.4.2 Verify RAM Data Against Master Device Data 3-3
3.4.3 Program Device With RAM Data 3-3
3.4.4 Extended Select Functions 3-4
3.5 ELECTRONIC IDENTIFIERS 3-5
3.6 FAMILY CODE AND PINOUT CODE SELECTION 3-5
3.7 DEVICE INSERTION 3-5
3.8 DEVICE REMOVAL 3-6

SECTION 4. MAINTENANCE/TROUBLESHOOTING/CALIBRATION

4.1 OVERVIEW 4-1
4.2 MAINTENANCE 4-1
4.2.1 UniPak 2™ Disassembly 4-1
4.2.2 Cleaning 4-3
4.2.3 Inspection 4-3
4.2.4 UniPak 2™ Assembly 4-3
4.3 TROUBLESHOOTING 4-4
4.3.1 No System Operation 4-4
4.3.2 Poor Yields 4-4
4.3.3 UniPak 2™ Failure 4-4
4.4 CALIBRATION 4-8
4.4.1 DC Calibration 4-10

SECTION 5. CIRCUIT DESCRIPTION

5.1 OVERVIEW 5-1
5.2 GENERAL ARCHITECTURE 5-1
5.2.1 The Link Between the UniPak 2™ and the Programmer 5-1
5.2.2 The Buses 5-1
5.3 COMPONENT LAYOUT 5-1
5.3.1 Motherboard 5-2
5.3.2 Waveform Generator 5-2
5.3.3 Address Card 5-4
5.3.4 Socket Card 5-5
5.3.5 Memory Card 5-6

APPENDIX A

APPENDIX B

TIMING DIAGRAMS B-1

APPENDIX C

SCHEMATICS C-1

30-701-2126 Memory Card
30-701-1655 Address Card
30-702-1659 Socket Card
30-702-1661 Motherboard
30-701-1690 Waveform Generator

LIST OF FIGURES

1-1 Example of a "Modification Status" Sticker 1-1
2-1 UniPak 2™ Installation 2-2
3-1 Typical 29A Programmer Operation 3-1
3-2 Programmer Power Switch Location 3-2
3-3 UniPak 2™ Sockets and Device Installation 3-6
4-1 UniPak 2™ Disassembly 4-1
4-2 Socketboard Interconnect Cable Disconnect 4-2
4-3 Circuit Board Removal 4-2
4-4 Memory Card Removal 4-2
4-5 Calibration Setup 4-9
4-6 UniPak 2™ Scope Trigger Test Point 4-10
4-7 Pin Numbers of Device Sockets 4-11
4-8 Adjustment Locations 4-11
4-9 Pin Names by Pinout Code Numbers 4-12
5-1 Block Diagram, UniPak 2™ Electronics 5-1
5-2 Principal Components 5-1
5-3 Block Diagram, Motherboard 5-2
5-4 Block Diagram, Waveform Generator 5-2
5-5 Block Diagram, Address Card 5-4
5-6 Block Diagram, Socket Card 5-5
5-7 Block Diagram, Memory Card 5-6

LIST OF TABLES

1-1 Programmer Compatability 1-1
4-1 Troubleshooting Chart 4-5
4-2 Key Sequence to Access the Calibration Mode 4-10
4-3 Measurement Chart 4-17
5-1 Pin Functions, Device Bus (at J1) 5-3

This page left intentionally blank.

Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_05330

SECTION 1
INTRODUCTION

1.1 OVERVIEW

Data I/O's UniPak 2™ reliably programs over 600 popular MOS and bipolar devices. Values for programming variables, including pinouts, voltage levels and timing, are stored in firmware tables. When you choose the family and pinout codes for a particular device, the programmer uses information in these tables to assemble a specialized programming routine in scratch RAM. This method allows high-speed operation with minimum firmware overhead. The UniPak 2™ is designed to adapt to the programming requirements of many different devices. Pinout variations are handled by seven device sockets on the UniPak 2™ and, in some cases, by adapters which connect to socket 1 or 2. Specially designed electronic switches allow programming of both bipolar and MOS devices.

To maximize control speed during programming, the UniPak 2™ makes extensive use of addressable latches for control signals. For flexibility in waveform generation, digital-to-analog converters (DACs) control all major power supplies, with several rise and fall times selected by firmware.

1.2 PROGRAMMER COMPATIBILITY

To be compatible with the UniPak 2™, your programmer may require a hardware and/or firmware update, depending on the model, configuration, and age. The information that follows will help you determine whether your programmer requires updating. If you find that your programmer does require updating, contact your nearest Data I/O Service Center.

- System 17—The System 17 must be converted into a System 19 with the latest firmware installed and latest hardware modifications.
- System 19—Check to determine whether your System 19 contains a 702-1520 or 702-1980 controller board by performing the following steps:

  1. Remove the programming pak (section 2.3).
  2. Remove the metal shield (if any) shown in figure 2-1.
  3. Count the number of EPROM firmware sockets located just behind the pak interface connector. If there are four sockets, it is a 702-1520 board. If there are eight sockets, it is a 702-1980 board.

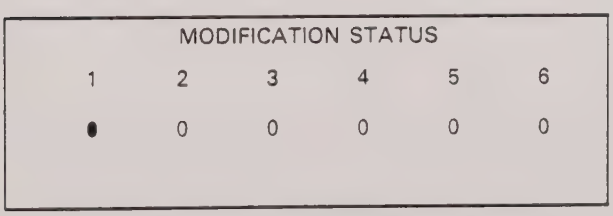


Figure 1-1. Example of a "Modification Status" Sticker

If your System 19 contains a 702-1520 controller board, check the modification status sticker (figure 1-1) on the bottom of the programmer. If the sticker is not there or if only "1" is marked off, your System 19 requires hardware and firmware updating; contact the nearest Data I/O Service Center. If "2" is marked, your System 19 is compatible with the UniPak 2™. If your System 19 contains a 702-1980 controller board, it may require a firmware update. To display the configuration number of the firmware in your programmer, key in "SELECT-B2-START". If the configuration number displayed matches the number listed below, your firmware needs updating.

Model	Configuration Number
• 990-1902	3599
• 990-1903	CC8B

- 29A Universal Programmer—To be compatible with the UniPak 2™, the 29A programmers must have Rev C or later firmware. To determine the configuration of the firmware in your 29A, key in "SELECT-B2-START" and observe the display. If the hex number matches one listed in table 1-1, your firmware needs to be updated.
- 29B Universal Programmer—The UniPak 2™ is compatible with Rev A or later software.
- 100A Production Programmer—To be compatible with the UniPak 2™, the 100A programmers must have Rev E or later firmware. To determine the configuration of the firmware in your 100A, key in "SELECT-10" and observe the display. If the hex number displayed matches one listed in table 1-1, your firmware needs to be updated.

Table 1-1. Programmer Compatibility

Model	Rev	Configuration Number
29A	A	1ECA
	B	20A4
29A (with computer remote control)	A	BB41
	B	C00B
100A	A	917F
	B	9405
	C	9DEE
	D	9BED

1.3 APPLICATIONS

Table A-1 (in appendix A) lists all the devices that could be programmed with the UniPak 2™ when this manual was published. In many cases when a new device with industry-standard pinout is introduced within a manufacturer's family, the UniPak 2™ WILL NOT require a revision to program it. For some new applications, such as to accommodate a new device family, a firmware update of the UniPak 2™ may be required. The revision number is stamped after the part number (950-0059) along the underside of the top edge of the UniPak 2™ socket assembly.

1.4 SPECIFICATIONS

The UniPak 2™ receives its power from the programmer mainframe. Programming waveforms are generated from raw programmer supplies using regulators controlled by the programmer's microprocessor. The controlling firmware is located on a circuit card within the UniPak 2™.

The physical and environmental specifications are:

- Altitude: Sea level to 3 km (10,000 ft.)
- Dimensions: 20.9 x 17.0 x 10.5 cm (8.2 x 6.7 x 4.2 in.)
- Humidity (operating): 90% maximum (noncondensing)
- Humidity (storage): 95% maximum (noncondensing)
- Temperature (operating): 0 to 40°C (32 to 104°F)
- Temperature (storage): −40 to 55°C (−40 to 131°F)
- Weight: 1.38 kg (3 lb. 0.5 oz.)

1.5 FIELD APPLICATION SUPPORT

Data I/O has field applications engineers (FAE's) throughout the world. They can provide additional information about interfacing Data I/O products with other equipment and answer questions about equipment. FAE's are located within the United States at the addresses listed in the back of this manual. For international applications support, contact your nearest Data I/O representative.

1.6 WARRANTY

Data I/O equipment is warranted against defects in materials and workmanship. The warranty period of one year, unless specified otherwise, begins when you receive the equipment. The warranty card inside the back cover of this manual explains the length and conditions of the warranty. For warranty service, contact your nearest Data I/O service center.

1.7 SERVICE

Data I/O maintains service centers throughout the world, each staffed with factory-trained technicians to provide prompt, quality service. This includes not only repairs, but also calibration of all Data I/O products. A list of all Data I/O service centers is located in the back of this manual.

1.8 ORDERING

To order equipment, contact your Data I/O sales representative. Orders must contain the following information:

- Description of the equipment (see the latest Data I/O price list or contact your sales representative for equipment and part numbers)
- Quantity of each item ordered
- Shipping and billing address of firm, including ZIP code
- Name of person ordering equipment
- Purchase order number
- Desired method of shipment

SECTION 2
INSTALLATION

2.1 INSPECTION

Your UniPak 2™ was tested both electrically and mechanically before it was shipped, and was carefully packaged to prevent shipping damage. It should, therefore, arrive free of any defect, without marks or scratches, and in perfect operating condition. However, carefully inspect the instrument for any damage that may have occurred in transit. If you note any damage, file a claim with the carrier and notify Data I/O.

2.2 UniPak 2™ INSTALLATION

The UniPak 2™ may be installed and removed with the programmer's power on; this feature allows you to retain data in RAM during module changes. If the programmer power is turned on before the UniPak 2™ is installed, you will hear a beep until the UniPak 2™ is installed.

NOTE

Voltage transients can cause device damage. Thus, be sure that all sockets are empty when:

- *switching power on or off*

or

- *installing or removing the UniPak 2™*

To install the UniPak 2™, do the following:

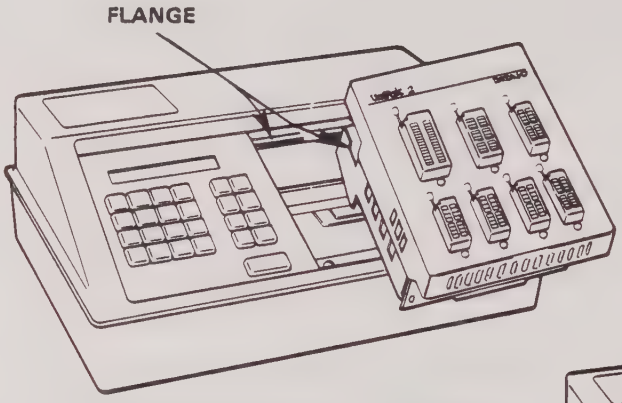
1. Slide the UniPak 2™ into the opening in the programmer (figure 2-1).
2. Tilt the UniPak 2™ up and gently push it back to hook the flange of the UniPak 2™ over the back edge of the programmer opening (figure 2-1, a).
3. Lower the UniPak 2™ into position as shown in figure 2-1, b.
4. Press gently on the front edge of the UniPak 2™ to ensure a good connection (figure 2-1, c).

2.3 UniPak 2™ REMOVAL

1. Check to make sure the programmer is not in the process of an operation. If it is, wait until the operation is complete (the action symbol on the display disappears).
2. Check to make sure a device is not in a socket. If one is in a socket, remove it as described in section 3.7.
3. Tilt the UniPak 2™ up and gently remove it from the programmer.

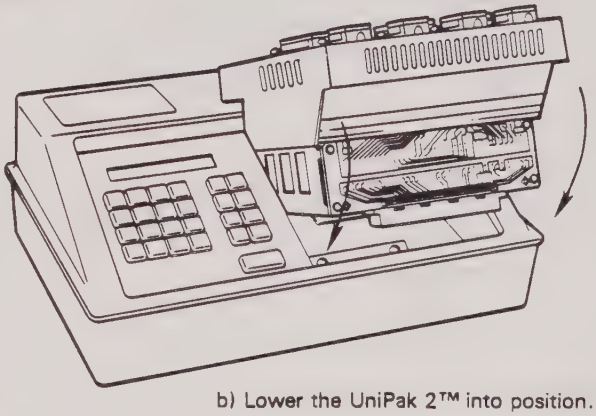
2.4 REPACKING FOR SHIPMENT

If the UniPak 2™ is to be shipped to Data I/O for service or repair, attach a tag to it describing the work required and identifying the owner. In correspondence, identify the unit by part number, revision level, and name. If the original shipping container is to be used, place the UniPak 2™ in the container with the appropriate packing material and seal the container with strong tape. If another container is used, be sure that it is a heavy carton, wrapped with heavy paper or plastic; use appropriate packing material and seal well with strong tape. Mark the container "DELICATE INSTRUMENT" or "FRAGILE."

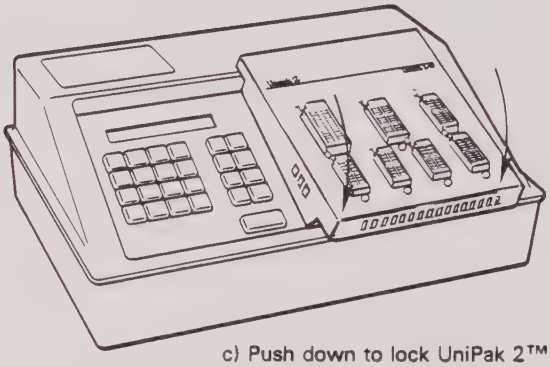


NOTE: Although the System 29A is shown here, the insertion procedure is the same for all systems.

a) Tip the UniPak 2™ up and back to lock flanges.



b) Lower the UniPak 2™ into position.



c) Push down to lock UniPak 2™ into place.

Figure 2-1. UniPak 2™ Installation

SECTION 3
OPERATION

3.1 OVERVIEW

The UniPak 2™ can be used in 29A, 29B, System 19, or 100A programmers of any configuration; see section 1.2 for firmware revision levels required. The typical programming operation with a 29A programmer and a UniPak 2™ is illustrated in figure 3-1. As can be seen from this figure, the UniPak 2™ can obtain data from three sources (a master device, a serial port, or the keyboard). Because the serial port and keyboard operations are unique for each type of programmer, you will be referred to your 29A, 29B, System 19, or 100A programmer manual for details on how to program using these mainframes.

When using a master device as the data source to program a blank device, you must first instruct the programmer to copy the device data into programmer RAM (shown as COPY in figure 3-1 and described in section 3.4). Then enter the family code and pinout code as described in section 3.6. The data in the device will have been copied to the RAM of your 29A when you press START, as shown in figure 3-1. You must then remove the master device and instruct the programmer to copy the information just stored in its RAM to a blank device. This completes the basic programming operation.

The procedures to perform basic operations with your UniPak 2™ are described in this section. You should follow these procedures to properly operate your UniPak 2™. Wherever possible, key sequences have been included for using your UniPak 2™ with a 29A Universal Programmer with Rev C firmware (read section 1.2 carefully to determine your programmer's firmware revision level). Refer to your programmer manual for key sequences for the System 19, 29B, and 100A programmers.

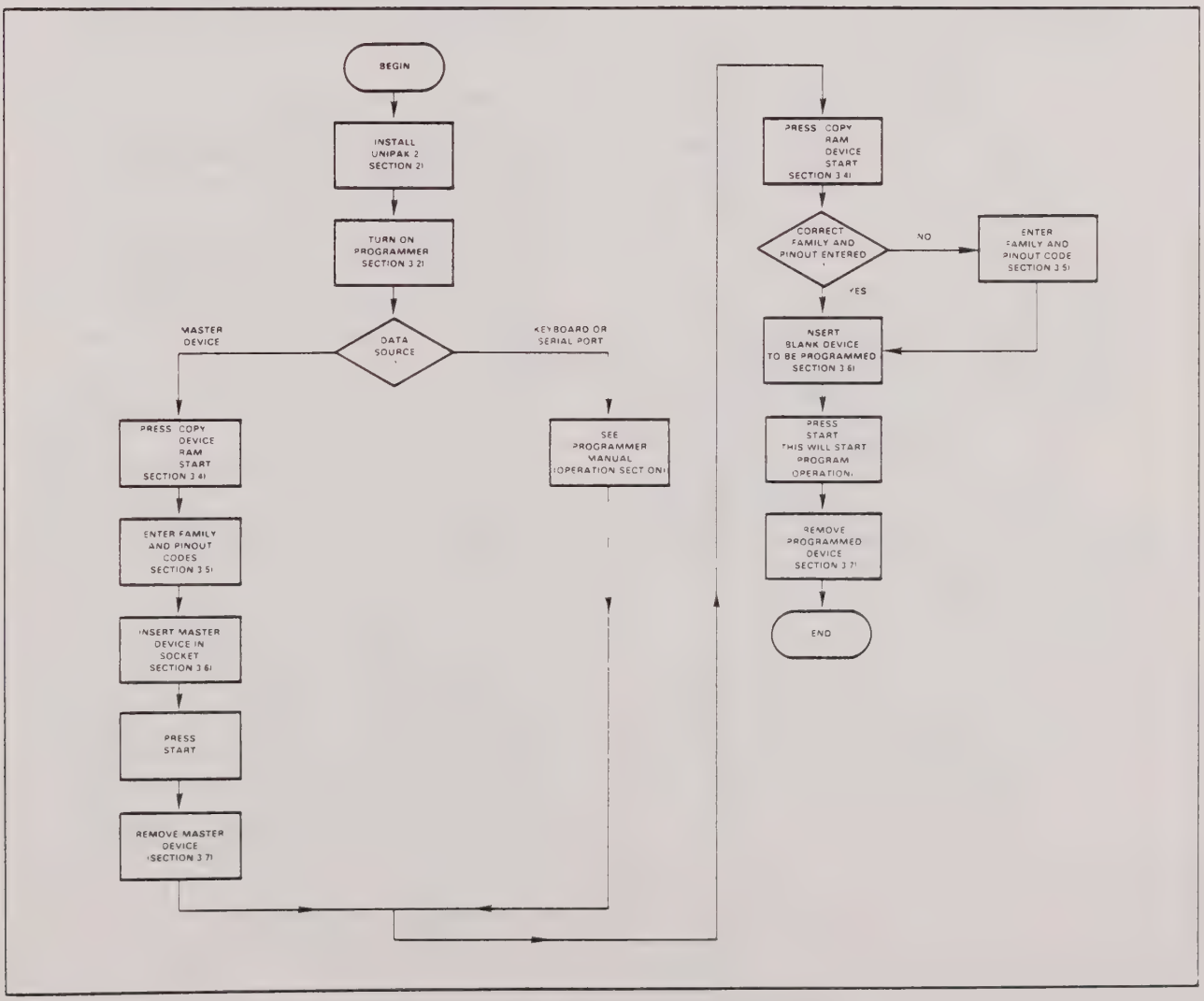


Figure 3-1. Typical 29A Programmer Operation

3.2 POWER UP

NOTE

If the UniPak 2™ is not installed in the programmer before power is turned on, you will hear a beep until the UniPak 2™ is installed.

When turned on, the programmer will perform an automatic self-test routine. When the self-test routine is complete, the programmer will signal its readiness.

To turn the programmer on, do the following:

1. Check to make sure a device is not in a socket. If a device is in a socket, lift up the lever (located on the upper left of the socket; see section 3.8), then gently lift the device out of the socket.
2. Plug the AC power cord into the power outlet.
3. Flip the power switch up to the "ON" position (see figure 3-2).

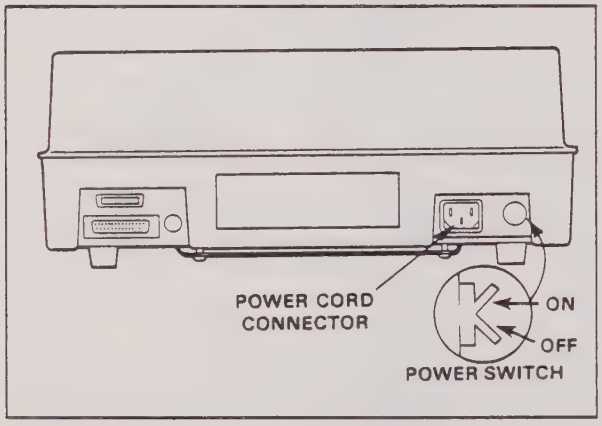


Figure 3-2. Programmer Power Switch Location

3.3 POWER DOWN

CAUTION

Do not turn the power off while the programmer is doing an operation or when a device is in a socket; voltage transients may damage the device.

To turn the programmer power off, do the following procedure:

1. Check to make sure that the programmer is not in the middle of an operation. If it is, wait until that operation is through.
2. Check to make sure a device is not in a socket. If a device is in a socket, remove it as described in section 3.8.
3. Flip the power switch down to the "OFF" position (figure 3-2).

3.4 BASIC OPERATION

All data transfer or verification operations take place between the programmer's internal RAM and the device or between the RAM and serial port in your programmer. Because the procedure to transfer data via a serial port varies from programmer to programmer, this manual describes only data transfer with the 29A. For other programmers, refer to your programmer operation manual.

The basic data transfer operations that can be performed with the UniPak 2™ and the 29A Universal Programmer are:

- Load RAM with data from a master device (described in section 3.4.1).
- Verify RAM data against the device data (described in section 3.4.2).
- Program a device with RAM data (described in section 3.4.3).

3.4.1 Load RAM With Data From Master Device

To load the 29A RAM with data from a master device, follow the steps listed below.

1. Press COPY; 29A displays COPY DATA FROM
2. Press DEVICE; 29A displays DEV ∧ ADDR/SIZE TO

NOTE
The device is the source of data.

3. Press RAM; 29A displays CO DEV > RAM ∧ ADDR

NOTE
The RAM is the destination of the data from the master device.

4. Press START; 29A displays FAM ∧ 00 PIN 00
5. Enter the family code and pinout code (see section 3.6).
6. Insert the master device into the UniPak 2™ (see section 3.7).
7. Press START; 29A displays LOADING DEVICE
   LOAD DONE XXXX

NOTE
XXXX is the sumcheck of the device.

8. Remove the master device from the UniPak 2™ (see section 3.8).

During source destination operations (copy and verify), ADDR and SIZE appear in the 29A prompts. These correspond to starting address and block size, respectively. For more detail on these parameters, see your programmer operation manual. When reading a device, the UniPak 2™ applies a nominal V_{CC} level. To simulate loading on device outputs, each output is driven by a 1.6 mA current source.

3.4.2 Verify RAM Data Against Master Device Data

The two-pass verify consists of comparing the device data to RAM data and is performed at two V_{CC} levels; these levels, plus the output-sink currents and the output-level-sense voltages, vary according to each manufacturer's requirements.

To verify that data entered in the 29A RAM duplicate the master device data, follow these steps:

1. Press VERIFY; 29A displays VERIFY DATA FROM
2. Press DEVICE; 29A displays DEV ∧ ADDR/SIZE TO

NOTE
The device is the source of data.

3. Press RAM; 29A displays VE DEV > RAM ∧ ADDR

NOTE
The RAM is the destination of the data from the master device.

4. Press START; 29A displays FAM 00 PIN 00
5. Enter the family code and pinout code (see section 3.6).
6. Insert the master device into the UniPak 2™ (see section 3.7).
7. Press START; 29A displays VERIFY DEVICE
   VE DEV DONE XXXX

NOTE
XXXX is the sumcheck of the device.

8. Remove the master device from the UniPak 2™ (see section 3-8).

3.4.3 Program Device With RAM Data

When programming a device, the system performs illegal-bit tests and blank checks at nominal V_{CC} and with nominal output loading.

To program a blank device with the data in the 29A RAM, follow these steps:

1. Press COPY; 29A displays COPY DATA FROM
2. Press RAM; 29A displays RAM ∧ ADDR/SIZE TO
3. Press DEVICE; 29A displays CO RAM > DEV ∧ ADDR
4. Press START; 29A displays FAM ∧ 00 PIN 00
5. Enter the family code and pinout code (see section 3-6).
6. Insert the blank device into the UniPak 2™ (see section 3-7).
7. Press START; 29A displays TEST DEVICE
   PROGRAM DEVICE
   VERIFY DEVICE
   PRG DONE 01 XXXX
8. Remove the device from the UniPak 2™ (see section 3.8).

NOTE
XXXX represents the sumcheck of the device.

3.4.4 Extended Select Functions

In addition to the three basic source-destination functions (copy, verify and edit) and the select functions described in the Operation section of your programmer manual, the UniPak 2™ offers eight extended select functions (BC, BD, C3, CC, CD, CE, CF and EF). These functions are not required for normal operation of the UniPak 2™.

Functions BC and BD are used to disable and enable the electronic identifier function for device families listed in section 3.5, with the exception of family FF.

To disable the electronic identifier test (BC), follow the procedure below.

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press BC START; 29A displays SELECT CODE **

To enable the electronic identifier test (BD), follow the procedure below.

1. Press SELECT; 29A displays SELECT CODE ∧
2 Press BD START; 29A displays SELECT CODE **

Function C3 gives access to options for specific family/pinout code combinations. If the UniPak 2™ is being used in a Model 19, this select code will work only from terminal remote.

To enter the options, follow the procedure below.

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press C3 START; 29A displays FXX PYY OPTIONS
3. Press START; 29A displays "NAME OF FIRST OPTION"

To select different options, press the REVIEW key. To execute an option, press START (in terminal remote, the RETURN key is used for the START key, and the space bar is used for the REVIEW key). If the option has subheadings under it, once the START key has been pressed, the REVIEW key can select the desired subheading. The START key is then pressed to execute the subheading. Once an option has been completely executed, an asterisk will be displayed after the option name. Complete execution may require doing a number of subheadings. Pressing the START key a second time after an option is completely executed will exit the options file, and the 29A will display OPTIONS DONE **.

NOTE

For the 8751H, the option "PROG SECTY ONLY" will program the security fuse as soon as the option is selected and executed.

Functions CC and CD are used in conjunction with electronic identifiers and may be used from the keyboard or from remote control.

Function CC displays the family and pinout codes of the last algorithm moved to RAM, usually the algorithm for the last device programmed or read. This function helps determine the family and pinout codes used by the programmer when in the automatic electronic identifier mode.

Function CD displays in hexadecimal 16 bytes of the device's electronic identifier. Byte Ø identifies the manufacturer; byte 1 identifies the device. For information on the purpose of the remaining bytes, consult the device data sheets.

To display the family and pinout codes of the last algorithm moved to RAM, follow the procedure below.

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press CC START; 29 A displays XXYY **

NOTE

XX represents the family code; YY represents the pinout code.

To display the electronic identifier, proceed as follows:

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press CD START; 29A displays 0000 YY
3. To display additional bytes of electronic identifier, press START; 29A displays 000X YY. To back up through previously displayed identifiers, press REVIEW; 29A displays 000X YY

NOTE

000X represents the byte number of the identifier displayed (i.e., 0001 represents byte 1 of the electronic identifier which is the device code). YY represents the identifier byte in hexadecimal.

Functions CE and CF are used to set the reject count (the number of programming pulses applied to a fuse or cell before it is rejected); CE sets the reject count back to the commercial specification (this is the default value) and CF sets the single-pulse reject count. This feature was accomplished in older UniPak™ models by adding 50 to the family code).

To select the commercial (default) reject count (CE), follow the procedure below.

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press CE START; 29A displays SELECT CODE **

To select the single-pulse reject count (CF), take the following steps:

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press CF START; 29A displays SELECT CODE **

Function EF calls up a four-digit hexadecimal configuration number and a two-digit decimal version number that correspond to the revision level and version number of the UniPak 2™ firmware. This function can be useful to identify firmware revision levels when communicating with Data I/O regarding field bulletins and updates.

To display the UniPak 2™ firmware configuration and version number, do the following:

1. Press SELECT; 29A displays SELECT CODE ^
2. Press EF START; 29A displays XXXX YY **

NOTE

XXXX represents the UniPak 2™ firmware configuration number, and YY represents the version number.

3.5 ELECTRONIC IDENTIFIERS

This version of the UniPak 2 ™ can read and use electronic identifiers in two modes.

The first mode occurs when family code 79, 93, 27, A5, BF, C5, AB, AF, C1, DD, or 45 is selected. The identifier is read and used to prohibit programming a device using the wrong family and pinout codes. The new low Vpp devices are protected from the old high Vpp algorithms which might destroy them. Older devices without signatures are permitted to program. An error will occur if you attempt to program using the wrong family or pinout codes.

The second mode is automatic. It is selected by entering family and pinout codes FF/FF. In this mode the operator need not look up any family or pinout codes; the electronic identifier is read and the correct algorithm is used for each device. An error will occur if you attempt to program on older devices without electronic identifiers or on newer devices whose identifiers are not yet supported.

3.6 FAMILY CODE AND PINOUT CODE SELECTION

Any device that can be programmed with the UniPak 2™ is specified by a unique combination of a two-digit family code and a two-digit pinout code (table A-1). Once the codes for a particular device are entered, the UniPak 2™ remains set up for any operation with that device until new codes are entered.

Your programmer manual will tell you where in the key sequence the family and pinout codes should be entered. If invalid family and pinout codes are entered, a beep will sound as either START or ENTER is pressed, or Err 30 (error 30) will be displayed and the operation will be aborted.

To select the family and pinout codes, do the following procedure:

1. Locate the manufacturer name and part number stamped on the device.
2. Turn to table A-1, Family and Pinout Codes, in appendix A, and find the same manufacturer name.
3. Then, in the first column (Device Part Number), find the number which corresponds to the part number stamped on the device.
4. Move to columns two and three, entitled Family and Pinout Codes, to find the numbers on the same line as the particular device number.
5. Enter these selected family and pinout code numbers.
6. Press "START."

NOTE

An LED (light-emitting diode) will light under one of the sockets.

Valid family and pinout codes must be in effect to use the System 19 DEVICE DATA key. When you press the DEVICE DATA key, either nominal, first-pass, or second-pass verify level is applied to the device. The level applied depends on the System 19's position in executing the selected mode. If the KEYBD light is on, the nominal verify level is applied.

3.7 DEVICE INSERTION

Once you have chosen the appropriate family and pinout codes, the UniPak 2™ is ready to accept a device in the socket located above the lighted LED.

NOTE

In the automatic electronic identifier mode, no LED is lighted unless UniPak 2™ is performing an operation on a device. An empty socket will always be unlighted. In this mode, disregard any reference to lighted LEDs; use the socket with the correct number of pins.

A good electrical connection between the device and the socket is essential. To ensure a good connection, do the following:

1. Check to make sure the programmer is not doing an operation. If it is, wait until the operation is complete.
2. Lift up the lever on the upper left side of the socket above the lighted LED; see figure 3-3. (The lever will stay locked into the upright position.)
3. Gently insert the device in the socket above the lighted LED. Make sure pin 1 of the device is aligned with pin 1 of the socket, as shown in figure 3-3.
4. Push the lever down to lock the device in the socket.

Once the family and pinout codes have been entered, the UniPak 2™ is ready for device-related operations. The key sequence to load, program, and verify are described in the Operation section of your programmer manual.

3.8 DEVICE REMOVAL

1. Check to make sure the programmer is not doing an operation. If it is, wait until the operation is complete.
2. Lift up the lever on the left side of the socket; see figure 3-3. (The lever will lock into the upright position.)
3. Lift the device out of the socket; the LED will remain illuminated.

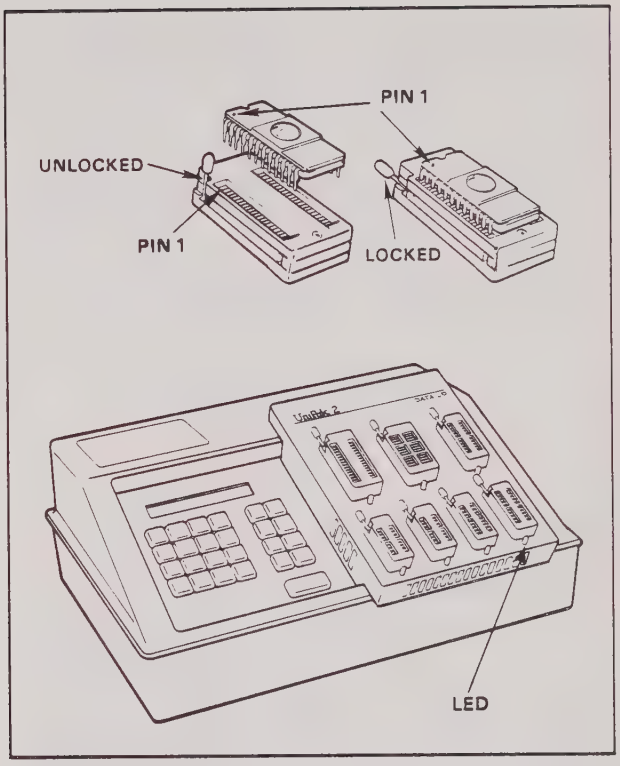


Figure 3-3. UniPak 2™ Sockets and Device Installation

UNIPAK 2™

Acceptance Test Procedure

Data I/O Corporation warrants to the original purchaser of the product described by the UniPak 2 Operator's Manual that the product was fully functional to the extent of its specification at the time of shipment from the factory. Data I/O further certifies that the test equipment used to test the product was calibrated to standards that are traceable to the National Bureau of Standards as appropriate.

This procedure is provided for customers whose company policy requires that an inspection test be performed before the unit may be accepted.

ACCEPTANCE TEST PROCEDURE

INTRODUCTION

WARNING

This procedure is for qualified engineering personnel only; do not attempt the operation if you are not qualified to do so.

Your UniPak 2 was tested both electrically and mechanically before it was shipped, and was carefully packaged to prevent shipping damage. It should arrive free of any defect, without marks or scratches, and in perfect operating condition. However, carefully inspect the instrument for any damage that may have occurred in transit. If you note any damage, file a claim with the carrier and notify Data I/O.

The UniPak 2 performance check consists of a brief procedure to check supply current/voltages to the socket pins, followed by a keyboard verification of proper operation. The supply current/voltage check is documented on a measurement chart and includes a photograph to compare with the oscilloscope waveforms.

PERFORMANCE CHECK

The following equipment is necessary to do the first part of the performance check:

- Three and a half-digit digital multimeter (DMM). The dcV accuracy of the DMM must be ±0.25% or better.
- Dual-trace oscilloscope (Tektronix 465 or equivalent)
- 100-ohm, 2W, 5% carbon-composition resistor

CAUTION

Remove all devices from the sockets before entering the calibration mode. Waveform generation may damage any device in the UniPak 2 sockets.

Current/Voltage Verification

To complete the first part of the performance check, do the following.

NOTE

If readings for any test do not fall within the specification given in the measurement chart, contact your nearest Data I/O customer support center.

1. Install the UniPak 2 into the programmer.
2. Turn the programmer power on (see the programmer manual).
3. Put the programmer into the calibration mode by following the key sequences in the following table.

NOTE

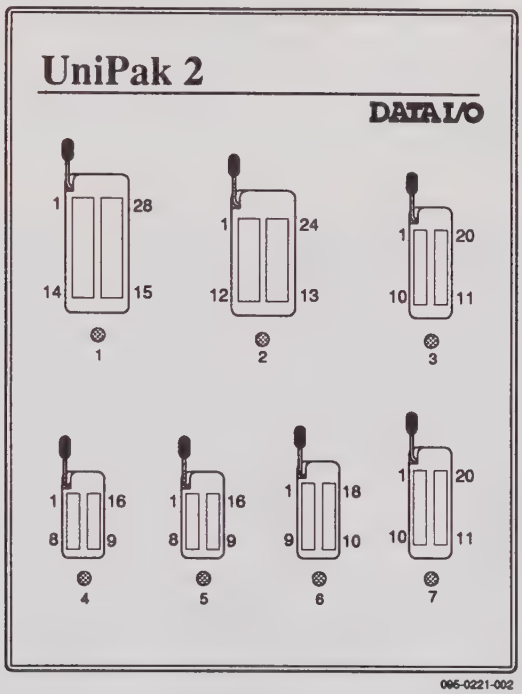
Because the current/voltage verification test checks only supplies that can be accessed externally, some steps of the standard calibration procedure are omitted on the measurement chart. Press the ***ENTER*** *or* ***START*** *key to increment the programmer to each step listed on the chart.*

Key Sequence to Access the Calibration Mode

Programmer System	Enter Calibration Mode	Key Sequence To Increment Step No.	Decrement Step No.
19	Press **SELECT** Press **C 2** Press **ENTER** Enter Step Number Press **START**	Press **ENTER**	Press **REVIEW**
29A/29B	Press **SELECT** Press **C 1** Press **START** Enter Step Number Press **START**	Press **START**	Press **REVIEW**
100A	Press **SELECT** Press **1 2** Enter Step Number Press **START**	Press **START**	Press **BACKSPACE**

4. Perform the steps on the measurement chart. For each general calibration step on the measurement chart do the following:

   - Take measurement readings at the device sockets described on the measurement chart; the figure shows the pin numbers for the sockets.



   - Ground the digital multimeter to socket 7, pin 10 on the front panel of UniPak 2.

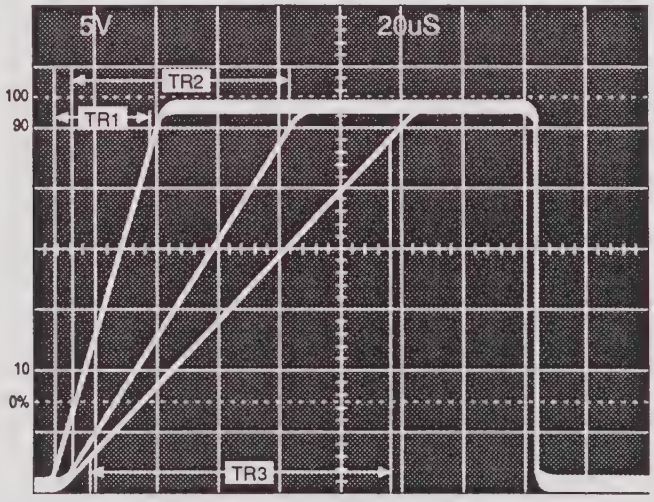
   - Access each new step by pressing the **START** (or **ENTER**) key. The new step number will appear in the display when the UniPak 2 is ready for the next step. To go back to a previous test, press the **REVIEW** (or **BACKSPACE**) key.

The voltage measurement chart on the following page includes the following headings:

- **Step No.** — tells which step to use for each test. Step numbers are keyed in at the programmer keyboard and are reflected in the display.
- **Test No.** — identifies individual tests for each step.
- **Test Description** — identifies the functions being tested.
- **Measurement Test Location** — tells which socket pins to probe for measurement.
- **Measurement** — specifies allowable measurement ranges. If a reading falls outside the range, contact your nearest Data I/O customer support center.
- **Comments** — gives special instructions for particular tests.

UniPak 2 Performance Check Measurement Chart

Step No.	Test No.	Test Description	Measurement Location Socket Pin	Measurement Min	Nom	Max	Comments
1		V reference supply					
	1	Vcc supply	2/24	11.9V	12.00V	12.10V	
	2	CE supply	2/24	11.90V	12.00V	12.10V	
	3	Bit supply	2/9	25.70V	26.00V	26.20V	
	4	Address supply	2/8	14.80V	15.00V	15.20V	
4	5	Current source supply	2/9	118.mA	120.mA	122.0mA	Use a 100-ohm, ±5% 5W resistor in series with the multimeter.
5	6	Bit switch rise waveform	2/14				See illustration.



095-0202-001

Variable		Min	Nom	Max	Unit
PROGRAM	TR1	26	33	37	µs
	TR2	62	66	70	µs
	TR3	81	100	119	µs

NOTE: All TR's are measured from 10% to 90%.

Step No.	Test No.	Test Description	Measurement Location Socket Pin	Measurement Min	Nom	Max	Comments
17	7	Socket #1 LED					Ensure that socket LED is illuminated.
	8	Odd address and data high	1/2,3,5,7,9,11,13,16,18, 22,24,26.	3.5V		6.00V	
	9	Even address and data low	1/1,4,6,8,10,12,15,17,19, 21,23,25,27.	–0.10V		0.40V	
18	10	Odd address and data low	1/2,3,5,7,9,11,13,16,18, 22,24,26.	–0.10V		0.40V	
	11	Even address and data high	1/1,4,6,8,10,12,15,17,19, 21,23,25,27.	3.50V		6.00V	
19	12	Odd data lines high	1/11,13,16,18.	25.50V		26.50V	
	13	Even data lines pullups	1/12,15,17,19.	4.50V		5.50V	
20	14	Odd data lines pullups	1/11,13,16,18.	4.50V		5.50V	
	15	Even data lines high	1/12,15,17,19.	25.50V		26.50V	

Verification of Operation

Once the current/voltage verification is finished, you may proceed to the operational verification part of the test. This procedure consists of programming a blank PROM with data from a master PROM.

NOTE

You should see your programmer's manual for specific details on doing load operations; the procedure here gives only general instructions. The sumcheck of the master device must be known and written down prior to beginning this operation.

Do the following to complete the verification of operation.

1. Install the UniPak 2 into the programmer.

2. Turn the programmer power on (see the programmer manual).

3. Transfer the device data from the master PROM to the programmer's RAM (see the programmer manual).

4. Transfer the RAM data to the blank device (see the programmer manual). The sumcheck displayed then the operation is completed must match the known sumcheck of the master PROM; if not, contact your nearest Data I/O Customer Support Center.

SECTION 4
MAINTENANCE/TROUBLESHOOTING/CALIBRATION

4.1 OVERVIEW

The support material in this section has been provided to help you keep your UniPak 2™ in good operating condition. General maintenance practices are discussed in section 4.2, while the basic troubleshooting steps are listed in section 4.3. For those UniPak 2™ users who prefer to do their own calibration, detailed procedures, including measurement charts and timing diagrams, are provided in section 4.4.

4.2 MAINTENANCE

Before the UniPak 2™ can be cleaned (section 4.2.2) and/or inspected (section 4.2.3), it must be disassembled as described below.

4.2.1 UniPak 2™ Disassembly

To disassemble the UniPak 2™, refer to figure 4-1 and follow the procedure outlined below.

1. Remove the UniPak 2™ from the programmer; see section 2.3 for details.
2. Place the UniPak 2™ face down on a flat surface.
3. Unscrew the captive fasteners (figure 4-1a) until they hang loosely; the screws will not separate from their standoffs.
4. Lift the card cage up slightly, then pull out (as shown in figure 4-1b) to unlock the flanges.

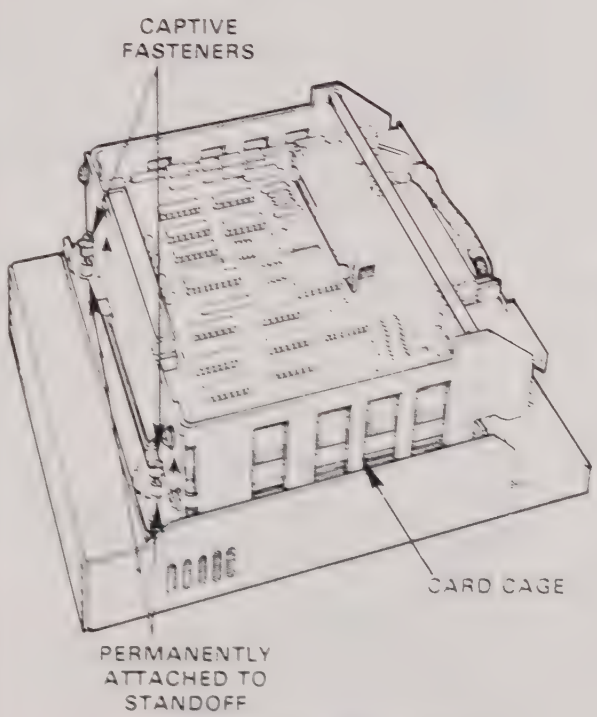


Figure 4-1a) Unscrew captive fasteners.

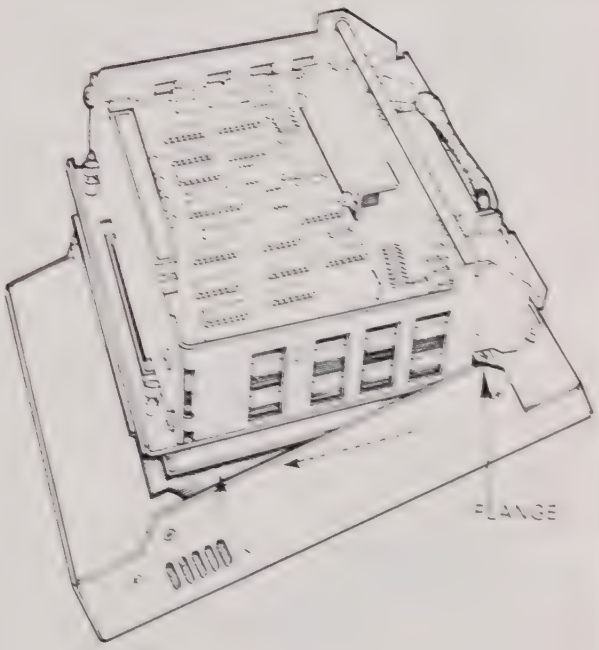


Figure 4-1b) Lift card cage up and out.

Figure 4-1. UniPak 2™ Disassembly

5. Lift the card cage up until you can see the socketboard interconnect cable and its connector (figure 4-2).
6. Flip the extraction tabs out on each side of the connector (figure 4-2).
7. Pull the cable out of the connector.
8. Disconnect the ground wire from the socketboard (see figure 4-2).
9. Flip the extraction tabs out on the top card (waveform generator card) and unplug the interconnect cable from its connector (figure 4-3).
10. Flip the extraction tabs out on the top card (waveform generator card).
11. Pull the waveform generator card out along the guides (figure 4-3).
12. Repeat steps 9, 10, and 11 for the extraction tabs on the address card.
13. Remove the two screws and the shield, and pull the memory card down to unplug it from the edge connector (as shown in figure 4-4).

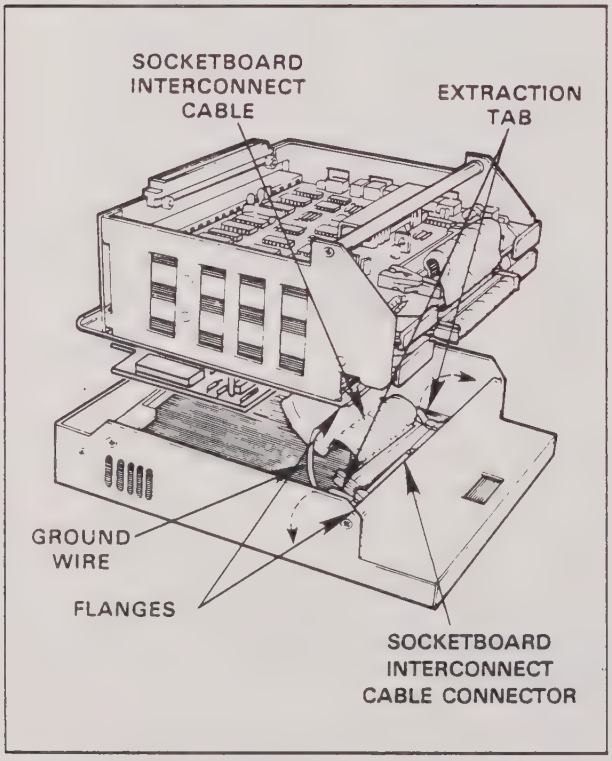


Figure 4-2. Socketboard Interconnect Cable Disconnect

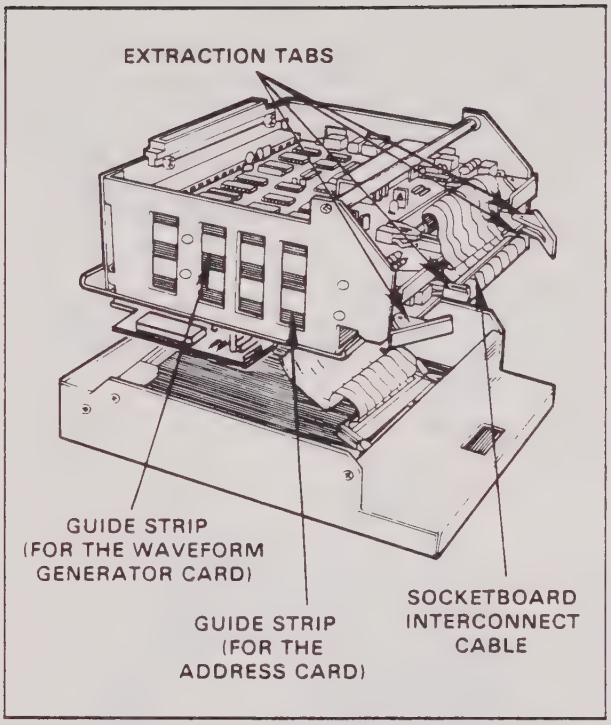


Figure 4-3. Circuit Board Removal

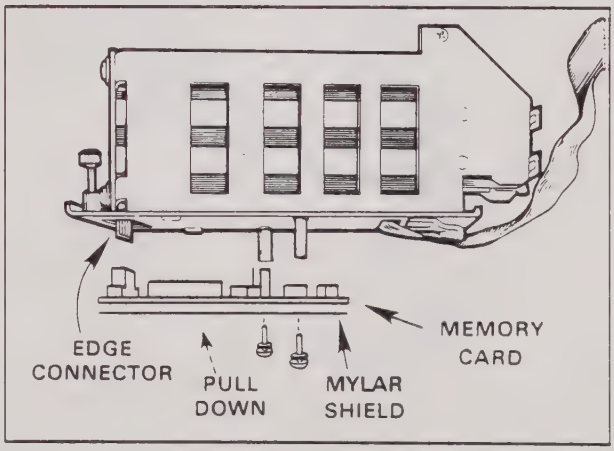


Figure 4-4. Memory Card Removal

4.2.2 Cleaning

Inspect the UniPak 2™ inside and out for accumulated dirt or dust. To clean the UniPak 2™, follow the procedure below.

1. Wipe any dust and/or dirt off the outside of the UniPak 2™ with a clean, damp cloth.

   NOTE

   Do not use abrasive cleaners or solvents. They will etch the paint.

2. Remove dust from the circuit boards with a blast of dry, compressed air or a clean, soft-bristled brush.

4.2.3 Inspection

You can help prevent malfunctions by periodically inspecting your UniPak 2™. Check cable connections, card seating, mounting of socketed components, etc., for shorts, opens or unstable continuity.

If you find heat-damaged components, be particularly careful to find and correct the cause of the overheating. This will prevent further damage.

4.2.4 UniPak 2™ Assembly

1. Plug the memory card onto its edge connector, as shown in figure 4-4.
2. Replace the shield, washers, and the two screws.
3. Flip the two extraction tabs down on the address card.
4. Using the flat surfaces of the extraction tabs, gently push the address card along the guides into its connector.
5. Make sure the extraction tabs on the interconnect cable connector are flipped open.
6. Firmly, but gently, push the socketboard interconnect cable into the connector. Notice that the extraction tabs will move back to their locked positions when the cable is locked into the connector.
7. Repeat steps 3 through 6 to replace the waveform generator card.
8. Reconnect the ground wire to the socketboard.
9. Plug the socketboard interconnect cable into its connector on the socketboard (figure 4-2).
10. Replace the card cage by tilting it up to lock the flanges, as shown in figure 4-1, then gently setting it down. Make sure the captive fasteners line up with the fastener holes on the UniPak 2™ frame.
11. Tighten the captive fasteners finger tight.

4.3 TROUBLESHOOTING

This section will help you interpret and isolate failures in the UniPak 2™. Use it in conjunction with section 5 (Circuit Description) and the schematics provided in the back of this manual.

There are three major classes of failures that can occur in a system comprised of a programmer and a UniPak 2™. The first is no system operation, the second is poor yields, and the third is UniPak 2™ failure.

After successfully troubleshooting the UniPak 2™, you must calibrate it according to the instructions in section 4.4. It is very important that the programmer be calibrated before the UniPak 2™ is calibrated.

4.3.1 No System Operation

You should perform the following steps if the system will not initialize with the UniPak 2™ installed. After completing each step, determine whether the problem still exists.

1. Check to be sure the UniPak 2™ is properly installed in your programmer.
2. Check the UniPak 2™ programmer mating connector (J1) for bent or broken pins. (Pin HH is intentionally shorter.)
3. Check the UniPak 2™ cards to be sure they are correctly installed in their connectors (section 4.2).
4. Check the ribbon cable to be sure it is properly inserted in the connectors (section 4.2).
5. Check the programmer power supplies for proper voltage output levels (see programmer manual).
6. If steps 1 through 5 fail to isolate the problem, contact your local Data I/O Service Center.

4.3.2 Poor Yields

If the yield rate begins to decrease, perform a complete calibration (see section 4.4). Be sure that the programmer has been calibrated first. After calibration, if the problem still exists, contact your local Data I/O Service Center.

4.3.3 UniPak 2™ Failure

Perform the following steps if a device will not program at all or if error messages are displayed. After completing each step, determine whether the problem still exists.

1. Check that the family and pinout codes are correct for the device, and that the device is being inserted in the correct socket.
2. If possible, try a known-good device to determine whether there is a hardware problem.
3. Check to be sure the UniPak 2™ is properly installed.
4. Check the UniPak 2™ programmer mating (J1) connector for bent or broken pins. (Pin HH is intentionally shorter.)
5. Check the UniPak 2™ cards to be sure they are correctly installed in their connectors (section 4.2).
6. Check to be sure the ribbon cable is correctly oriented and properly inserted in the connectors.
7. Perform a complete calibration, noting any measurements falling outside the indicated limits. Refer to the corresponding test number in table 4-1 for suspected boards and components, as well as the circuit description (section 5) and the schematics, to attempt to isolate the problem.
8. Perform waveform observations and note any discrepancies. Referring to the circuit description and the schematics may be helpful in isolating the problem.
9. If steps 1 through 8 fail to resolve the problem, contact your local Data I/O Service Center.

Table 4-1. Troubleshooting Chart

TEST NUMBER	SUSPECT CARDS	SUSPECT COMPONENTS
1	701-1655	VR1, U17, U25
2	701-1655	VR1, U16, U25, Q2, Q3
3	701-1655	VR1, U16, U25, Q2
4	701-1690	U15, U7, U12, Q21, R52, CR15, CR16, VR1, Q15
	702-1659	CR18, U10
5	701-1690	U14, U7, U3, Q3, R15, CR4, CR3, U10, U9, U11, Q24, Q25, Q19, CR14, Q16, U18, U17, VR1, Q15
	702-1659	C5, R11, CR9
6	701-1690	U13, U7, U6, Q9, R31, CR10, CR11, Q2, CR19, VR1, Q15
	701-1655	U23, R1, Q15, Q17, RP8, RP3, RP4, RP2, Q4, U24, U11, CR6
7	701-2126	U8, U1, VR3, Q2, R23
	702-1659	CR24, Q10, U20
	701-1655	U4, U14
8	701-1655	VR1, U17, U25
9	701-1655	VR1, U16, U25, Q2
10	701-1655	VR1, U17, U25
11	701-2126	U17, Q3, R2, VR1, U2, Q1, CR1, CR2
	701-1655	U23, R1, Q15, Q17, RP8, RP3, RP4, RP2, Q4, CR6, U24, U11
12	701-2126	U17, Q3, R1, VR1, U2, Q1, CR1, CR2, VR2, U1, UU1, U4, R1
	701-1655	U23, R1, Q15, Q17, RP8, RP3, RP4, RP2, Q4, U24, U11, CR6
13	701-1690	U17, U18, U11, Q22, Q25, Q2, CR19
	701-1655	U23, R1, RP8, Q16, RP3, Q14, RP4, RP2, Q12, U19, U24, CR9
14	701-1690	U15, U7, U12, Q21, U16
	702-1659	CR18, U10
15	701-1690	U16, U13, U7, U6, Q9
16	701-1690	U16, U14, U7, U3, Q3
17	701-1655	U26, U17, U25, VR1
18	701-1655	U26, U16, U25, VR1, Q2
19	701-2126	U1, UU1, U17, U4, Q3, U2, CR1, CR2, Q1, U10
	701-1655	U23, R1, RP8, Q15, RP3, Q17, RP4, RP2, Q4, CR6, U11, U24
20	701-1690, 701-1655, 702-1659	
21	702-1659	U4, DS2
	701-1655	U18
22	701-1690	U15, U7, U12, Q21, CR15, CR14, U16
	702-1659	CR18, U10
23	702-1659	CR26, Q6, Q7, Q5
	701-1690	U16, U13, U7, U6, Q9, CR10, CR11
	701-2126	U10, U6, U5, U9, U4, U12
24	701-1690	U16, U14, U7, U3, Q3, U9, U10, U11, Q24, Q25, Q19, CR14, Q16, CR4, CR3
	702-1659	C5, R11

Table 4-1. Troubleshooting Chart (Continued)

TEST NUMBER	SUSPECT CARDS	SUSPECT COMPONENTS
25	701-1690	U16, U14, U7, U3, Q3, U9, U10, U11, Q24, Q25, U5, Q6, Q8, CR8, CR4, CR3
	702-1659	C5, R11
26	701-1690	U16, U14, U7, U3, Q3, U9, U10, U11, Q24, Q25, U5, Q13, CR9, Q4, Q10, Q12, Q5, Q7, CR4, CR3
	702-1659	C5, R11
27	701-1690	U16, U13, U7, U6, Q9, CR10, CR11, Q2, CR19
	701-1655	U23, R1, Q16, RP3, Q17, RP4, RP2, Q8, CR9, U19, U24
28	701-1690	U16, U13, U7, U6, Q9, Q2, Q18, U17, Q11, CR2, Q14, U5
29	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	CR18, U10
30	701-1690	U16, U14, U7, U3, Q3, CR4, CR3, U9, U10, U11, Q24, Q25, U5, Q6, Q8, CR8
	702-1659	C5, R11
31	701-2126	U8, U1, VR3, Q2, R23
	702-1659	CR24, Q10, U20
	701-1655	U4, U14
32	701-1690	U18, U10, U5, U7, Q20, Q7, Q5, Q12, U9, CR9, Q13, U11, Q24
	702-1659	CR8, C5, R11
33	701-1690	U11, CR17, VR2, U18, Q19, Q16, U9, Q24, U10
	702-1659	CR9, R11, C5
34	701-1690	U16, U13, U7, U6, Q9, CR10, CR11
	702-1659	CR4, CR3, CR2, U22, CR5, Q1, CR32, CR31, CR28, C3, C13
	701-2126	U1, VR2, UU1, U17, U4, Q3, U2, Q1, CR1, CR2, VR1
	701-1655	U19, U24, U23, R1, Q16, RP3, Q17, RP4, RP2, Q8, CR9
35	701-2126	U1, VR2, UU1, U17, U4, Q3, U2, Q1, CR1, CR2, VR1
	701-1655	U19, U24, U23, R1, Q16, RP3, Q17, RP4, RP2, Q8, CR9
36	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	CR18, U10
37	701-1690	U16, U14, U7, U3, Q3, CR4, CR3, U9, U10, U11, Q24, Q25, U5, Q13, CR9, Q7, Q5, Q12, Q20, U7
	702-1659	C5, R11
38	701-1690	U16, U13, U7, U6, Q9, CR10, CR11
	702-1659	CR4, CR3, CR2, U22, CR5, Q1, CR32, CR31, CR28, C3, C13
	701-2126	U1, VR2, U1, U17, U4, Q3, U2, Q1, CR1, CR2, VR1
	701-1655	U24, U11, U23, R1, RP8, Q15, RP3, Q17, RP4, RP2, Q4, CR9
39	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	CR18, U10
40	701-1655	VR1, U16, U25, Q2, RP5, U28, U22, CR9, CR6, U24, U11, U19, CR4, CR7
	702-1659	Q2, CR29, R30, CR28, CR31, CR32
41	701-1655	VR1, U16, U25, Q2, RP5, U28, U22, CR9, U24, U11, U19, CR4
	702-1659	Q2, CR29, R30, CR28, CR31, CR32
42	701-1655	VR1, U16, U25, Q2, RP5, U28, U22, CR9, U24, U11, U19,
43	701-1655	VR1, U16, U25, Q2, RP5, U28, U22, CR9, CR6, U24, U11, U19, CR4, CR7
	702-1659	Q2, CR29, R30, CR28, CR31, CR32

Table 4-1. Troubleshooting Chart (Continued)

TEST NUMBER	SUSPECT CARDS	SUSPECT COMPONENTS
44	702-1659	DS1, U4
	701-1655	U18
45	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	CR7, U10
46	701-1655	U2, U3, U4, U14
	701-2126	U8, VR3, CR3, Q2, U1
	702-1659	CR24, Q10, U20, U21, U13
47	701-1655	U2, U3, U4, U14
	701-2126	U8, VR3, CR3, Q2, U1
	702-1659	CR24, Q10, U20, U21, U13
48	701-1655	U2, U3, U4, U14
	701-2126	U8, U1, U3, CR3, Q2
	702-1659	CR24, Q10, U20, U21, U13
49	701-1655	U2, U3, U4, U14
	701-2126	U8, U1, VR3, CR3, Q2
	702-1659	CR24, Q10, U20, U21, U13
50	701-1655	Q4, Q8, Q12, Q5, Q14-17, U23
51	701-1655	Q6, Q11, Q9, Q7, Q14-Q17, U23
52	701-1655	Q4, Q8, Q12, Q5, Q14-17, U23
53	701-1655	Q6, Q11, Q9, Q7, Q14-17, U23
54	702-1659	DS3, U4
	701-1655	U18
55	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1669	CR22, U10
56	702-1659	DS4, U4
	701-1655	U18
57	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-1659	U10, CR1
58	702-1659	DS5, U4
	701-1655	U18
59	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	U10, CR11
60	702-1659	DS6, U4
	701-1655	U18
61	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-1659	U10, CR19
62	702-1659	DS7, U4
	701-1655	U18
63	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	U10, CR23
64	702-1659	Q3, CR14, RP1, R10, CR17, U10
	701-1655	U18, U22
65	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-1655	VR1, U16, U17, U25, Q2, Q3, Q1
	702-1659	CR17, CR1, CR11, CR19, CR23, CR22, CR7, CR18, U10
66	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-1655	VR1, U16, U17, U25, Q2, Q3, Q1
	702-1659	CR17, CR1, CR11, CR19, CR23, CR22, CR7, CR18, U10

4.4 CALIBRATION

The need for calibration varies with the amount of use your UniPak 2™ receives. Generally, we suggest calibration whenever: 1) programming yields fall below the manufacturer's recommended minimums, or 2) troubleshooting has been completed, or 3) the user's company policy requires periodic calibration certification.

NOTE

If calibration or repair is required but you lack the facilities to accomplish it, contact the nearest Data I/O Service Center.

Because of differences in programmer mainframes, this manual does not attempt to cover all areas of programmer calibration. Instead, it lists the steps necessary to calibrate only the UniPak 2™.

Calibration of the UniPak 2™ consists of three parts:

1. Power Supply Calibration—measures the DC supply voltages of the programmer. All other voltages depend on these supplies; therefore, this part of the calibration procedure must be done first. Refer to your programmer manual.
2. DC Calibration—consists of measuring and adjusting critical DC voltage levels generated by the UniPak 2™.
3. Waveform Observation—enables observation of waveforms on an oscilloscope to ensure compliance with the device manufacturers' critical voltage and timing specifications.

The first part of the calibration procedure (power supply calibration) varies with the type of programmer you have. Therefore, this manual refers you to your programmer manual for details on power supply calibration. DC calibration is discussed in section 4.4.1.

The following equipment is necessary to calibrate the UniPak 2™:

- Data I/O calibration extender (part number 910-1521)
- Three and a half-digit digital voltmeter (DVM)
- Dual-trace oscilloscope (Tektronix 465 or equivalent)

Check the appropriate programmer manual for any additional equipment that you may need to calibrate the programmer.

To prepare your UniPak 2™ for calibration, follow the procedures outlined below.

1. Turn the programmer power off; see section 3.3 for details.
2. Remove the UniPak 2™ from the programmer; see section 2.3 for details.
3. Insert the calibration extender into the programmer the same way you insert the UniPak 2™ (section 2.2).
4. Unscrew the two thumb screws (captive fasteners) located on the underside of the top cover of the UniPak 2™ (figure 4-1); they connect the card cage to the socket assembly. Separate the two parts of the assembly.

CAUTION

Do not let the fasteners short to the motherboard.

5. Insert the 64-pin connector of the card cage into the mating connector on the calibration extender (figure 4-5, detail B).
6. Lean the top portion of the UniPak 2™ against its bottom portion at a 45-degree angle; see figure 4-5.

NOTE

Be sure the socket assembly flange locks into the card cage flange (see figure 4-5, detail A).

Do not allow the frame of the socket assembly to short to the memory board.

Be careful not to strain the cable or scratch the top of the programmer.

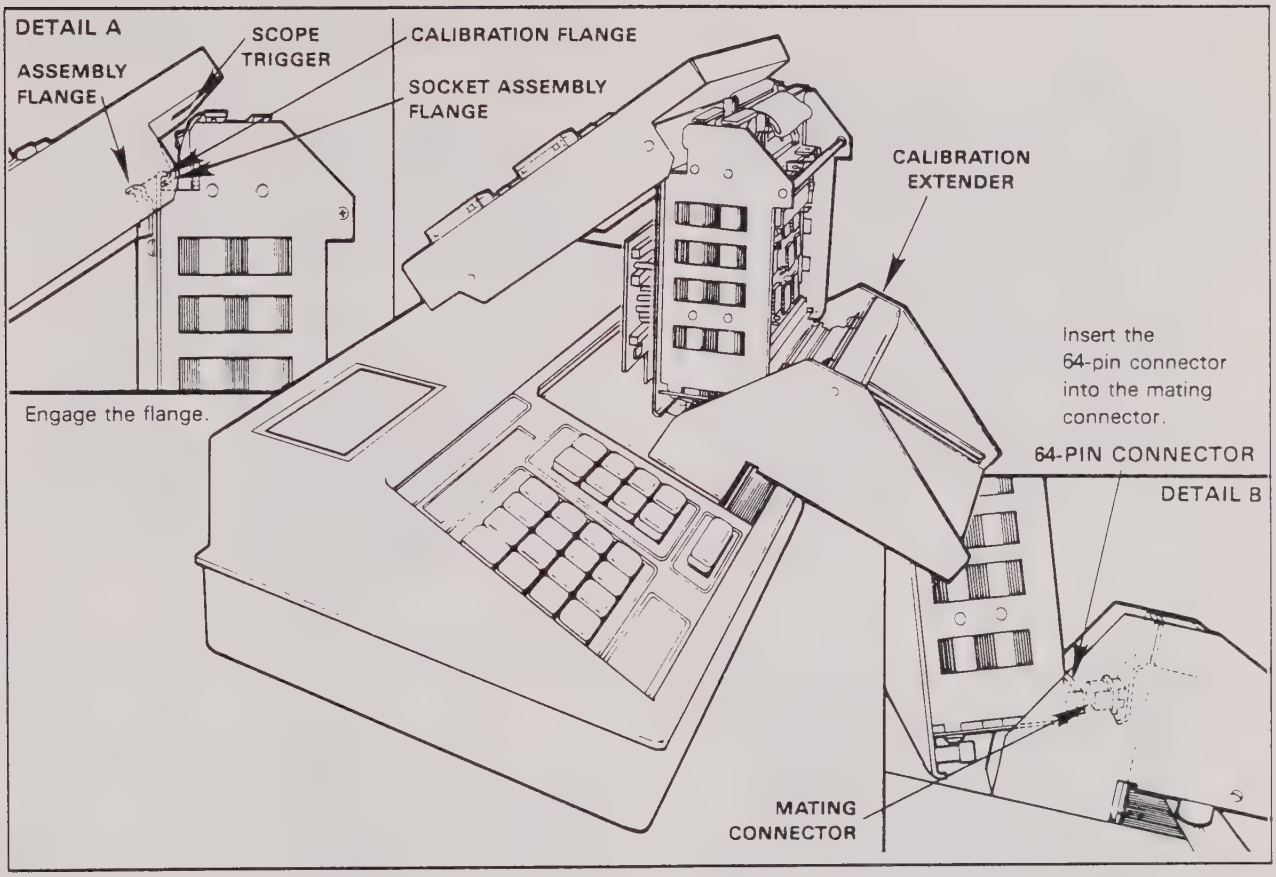


Figure 4-5. Calibration Setup

4.4.1 DC Calibration

The DC calibration procedure described in this section enables you to adjust critical DC voltage levels generated by the UniPak 2™. To follow this procedure, use the measurement chart at the end of this section. This measurement chart contains the information needed for all DC calibration tests. This information is included on the measurement chart in columns with the following headings:

- Step No.—tells which step to use for each test. Step numbers are set at the programmer keyboard and reflected in the display.
- Test No.—identifies individual tests.
- Test Description—identifies the functions being tested.
- Measurement Test Location—tells which socket pins, circuit boards, or test points to probe for measuring voltages.
- Measurement—specifies allowable measurement ranges. If a reading falls outside the range and you cannot adjust it to within the range, do not use the UniPak 2™ until the problem is corrected.
- Adjustment Location—tells which potentiometer to adjust if a measurement is out of range.
- Comments—gives special instructions for particular tests.

The DC calibration procedure is as follows:

CAUTION

Remove all devices from the sockets before entering the calibration mode (see section 3.8 for details). Waveform generation may damage any device in the UniPak 2™ sockets.

1. Turn the programmer power on (section 3.2).
2. Put the programmer into the calibration mode by following the key sequences in table 4-2.
3. Perform the general calibration steps (steps 1 through 24) on the measurement chart. For steps 5, 6, and 7, refer to the figures at the end of the measurement chart to observe the bit switch rise waveform the DAC step waveforms, and the current DAC step waveform. Trigger your oscilloscope by connecting to the test point under the top edge of the socket assembly (see figure 4-6).

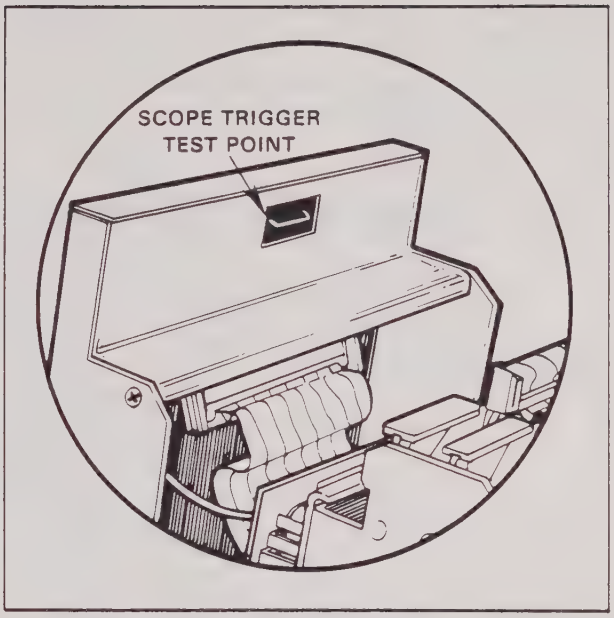


Figure 4-6. UniPak 2™ Scope Trigger Test Point

Table 4-2. Key Sequence To Access the Calibration Mode

Programmer System	Key Sequence To Enter Calibration Mode	To Increment Step No.	To Decrement Step No.
19	Press SELECT Press C2 Press ENTER Enter Step Number* Press START	Press ENTER	Press REVIEW
29A/ 29B	Press SELECT Press C1 Press START Enter Step Number* Press START	Press START	Press REVIEW
100A	Press SELECT Press 12 Enter Step Number* Press START	Press START	Press BACK-SPACE

*Optional

For each general calibration step on the measurement chart do the following:

- Take measurement readings at the device sockets or test points indicated on the measurement chart (table 4-3); figure 4-7 shows the pin numbers for the sockets; figure 4-8 shows test points; and figure 4-9 shows the device pin names by pinout code numbers.
- Ground the digital voltmeter to socket 7, pin 10 on the front panel of UniPak 2™.
- The adjustment pots on the waveform generator, memory board, and the address card enable you to make adjustments when your measurements do not match the measurement chart; figure 4-8 shows the location of these adjustment points.
- Access each new step by pressing the START (or ENTER) key. The new step number will appear in the display when the UniPak 2™ is ready for the next step. To go back to a previous test, press the REVIEW (or BACKSPACE) key.

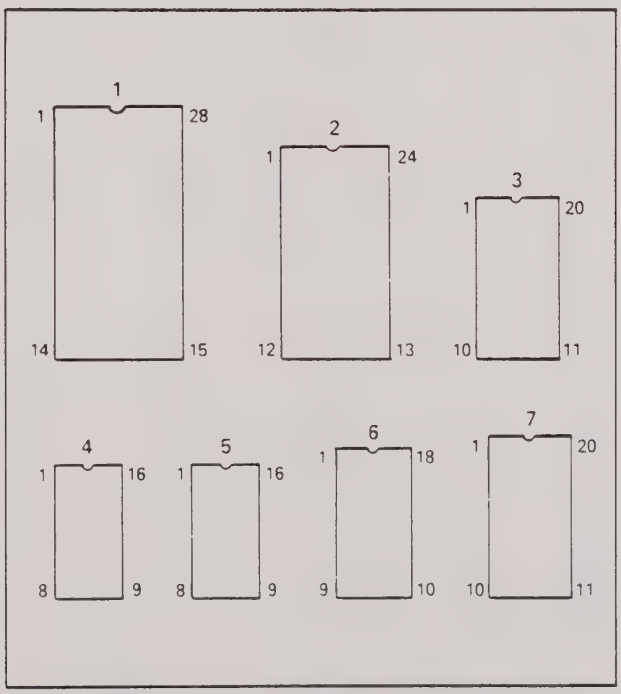


Figure 4-7. Pin Numbers of Device Sockets

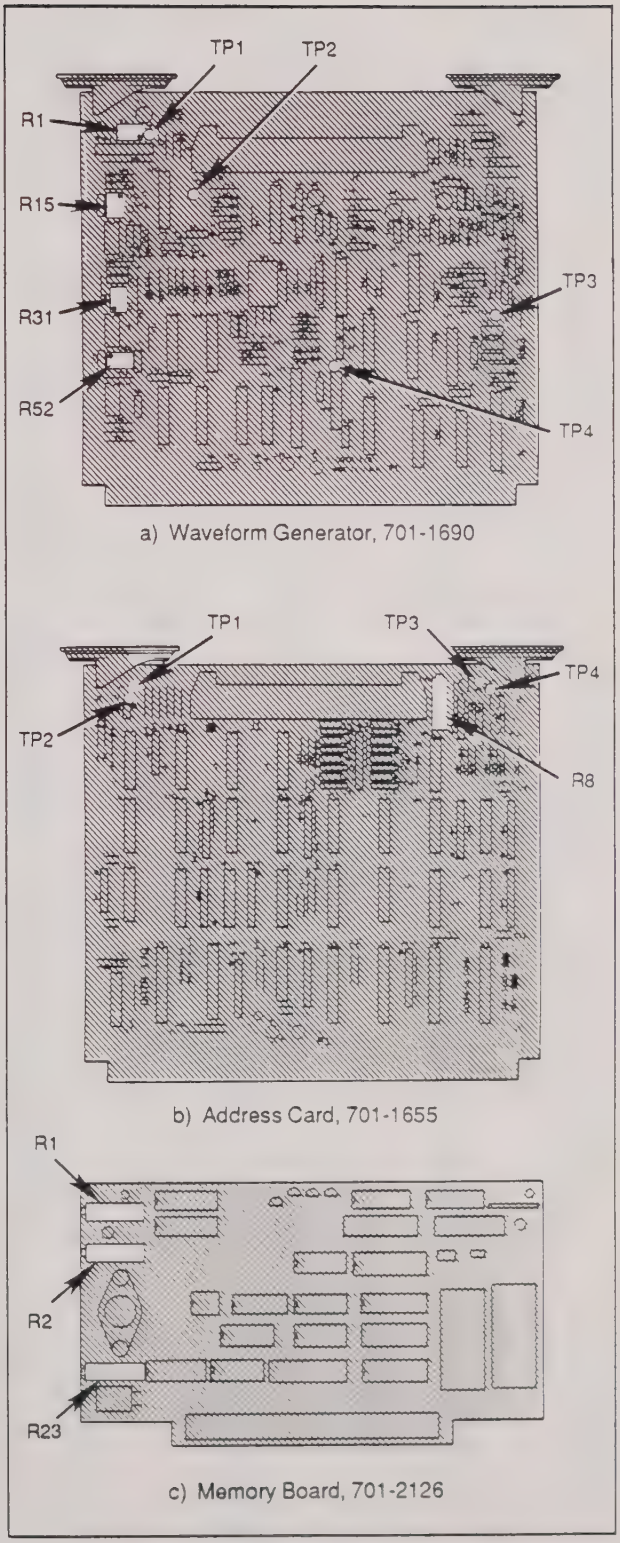


Figure 4-8. Adjustment Locations

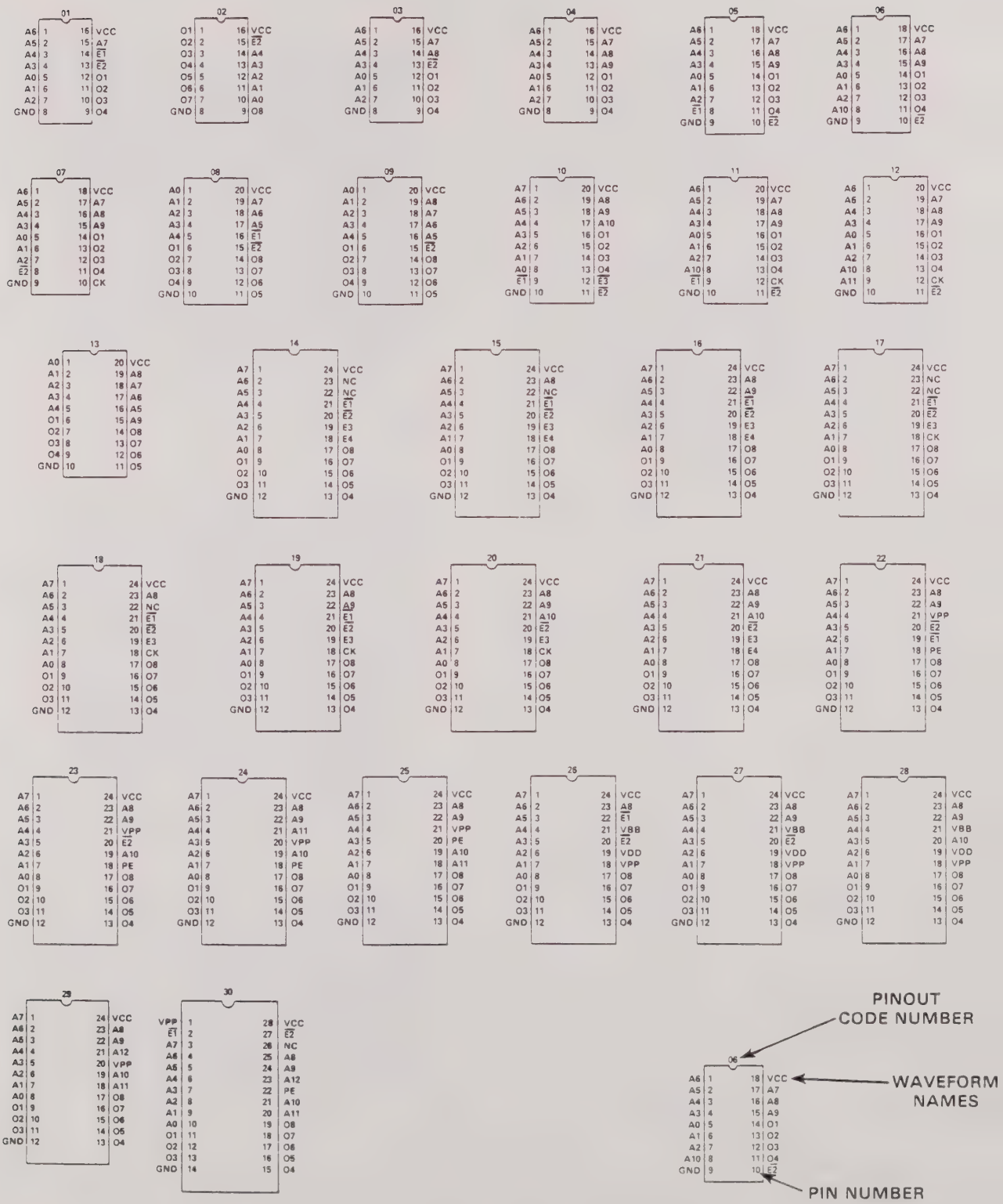


Figure 4-9. Pin Names by Pinout Code Numbers

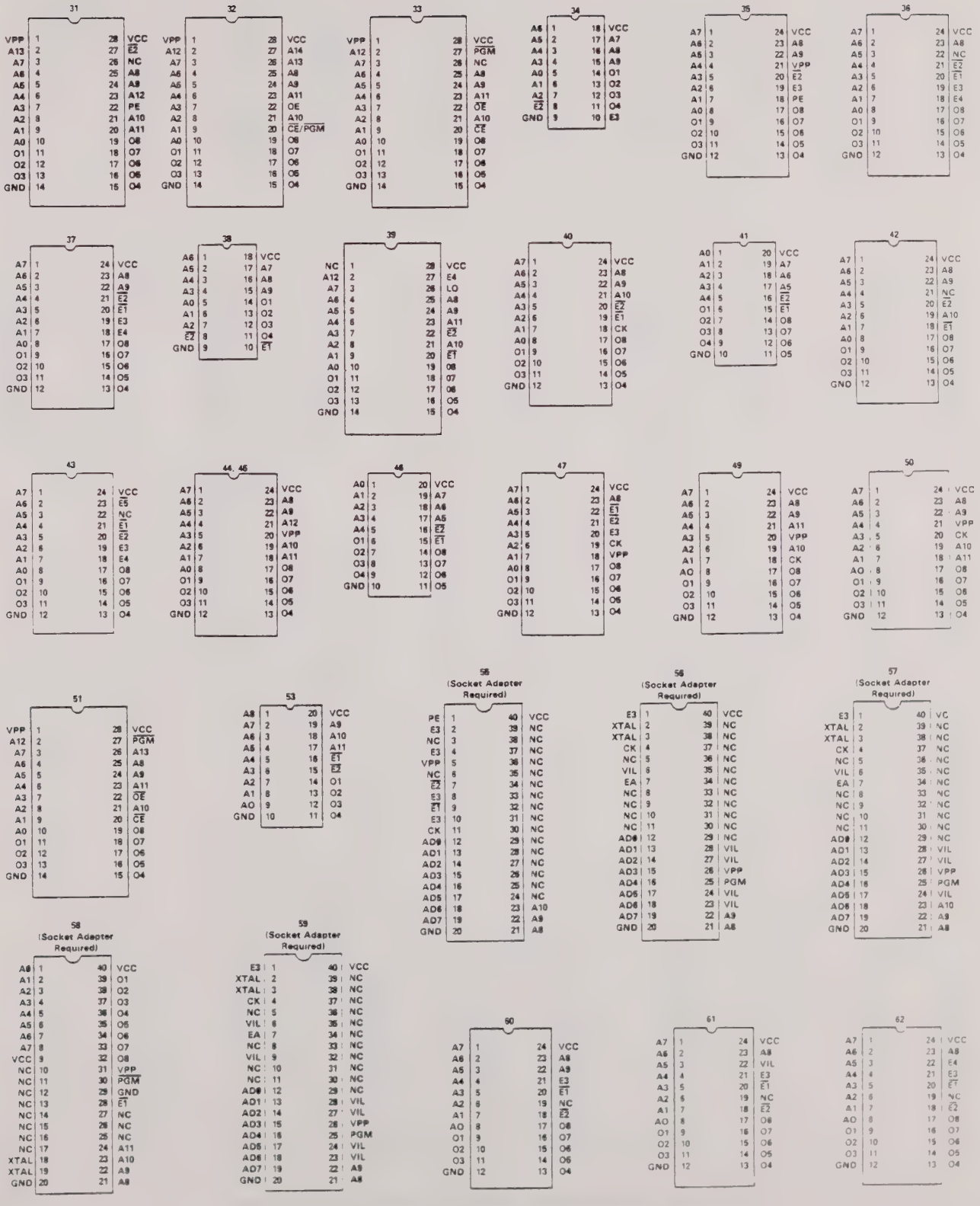


Figure 4-9. Pin Names by Pinout Code Numbers (Continued)

Figure 4-9. Pin Names by Pinout Code Numbers (Continued)

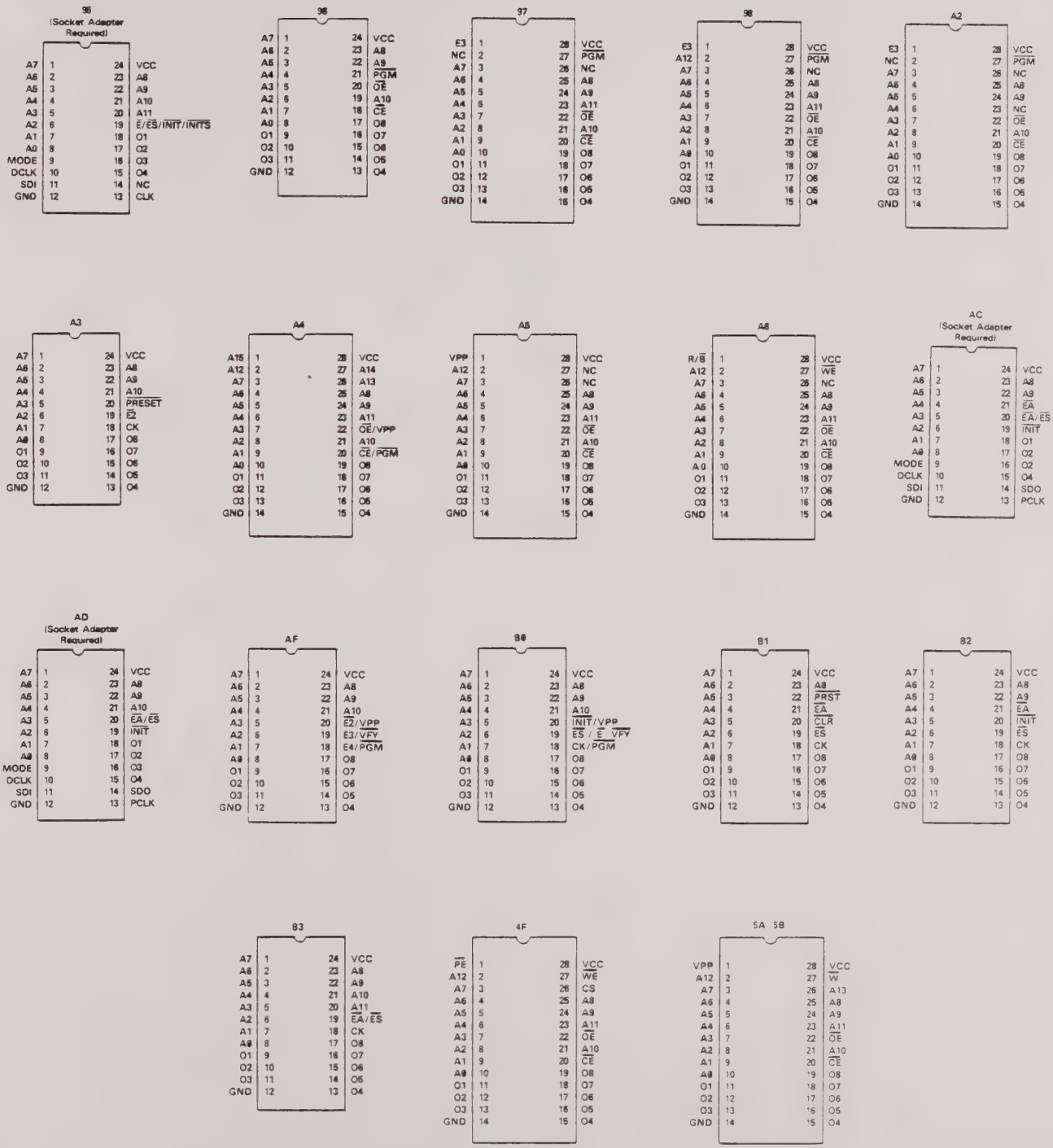


Figure 4-9. Pin Names by Pinout Code Numbers (Continued)

This page left intentionally blank.

Table 4-3. Measurement Chart

REVISIONS

LTR	DESCRIPTION	P E	DATE
A			10/82
C	ECN 4831		5/83
D	ECN 5023		2/84

UniPak 2^{tm} Measurement Chart

STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/Pin	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DMM to socket 7, pin 10
			The following tests are performed					
			with the UniPak 2™ on the calibration					
			extender.					
1	1	V reference supply	701-1655/TP2	14.4V	14.5V	14.6V	R8,701-1655	
	2	Load supply (high range)	701-1655/TP4	25.0V		26.0V		
	3	Load supply (low range)	Socket/Pin 701-1655/TP3	25.0V		26.0V		
	4	V_{CC} supply	2 24	11.9V	12.0V	12.1V	R52,701-1690	
	5	CE supply	2 20	32.7V	33.0V	33.2V	R15,701-1690	
	6	Bit supply	2 9	25.7V	26.0V	26.2V	R31,701-1690	
	7	Address supply	2 8	14.8V	15.0V	15.2V	R23,701-2126	
2	8	V reference supply	701-1655/TP2	6.70V		6.90V		
	9	Load supply	701-1655/TP3	10.3V		11.7V		
3	10	V reference supply	701-1655/TP2	3.30V		3.50V		
	11	Current source 20 mA	2 9	19.5 mA	20.0 mA	20.5 mA	R2,701-2126	Use a 100-ohm, 2W carbon comp resistor in series with the current meter.
4	12	Current source supply	2 9	118 mA	120 mA	122 mA	R1,701-2126	Use a 100-ohm, 2W carbon comp resistor in series with the current meter.

Table 4-3. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P E	DATE
A			10/82
C	ECN 4831		5/83
D	ECN 5023		2/84

UniPak 2 Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/Pin	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DMM to socket 7, pin 10
5	13	Bit switch rise waveform	2 14				R1, 701-1690	See waveform photograph (page 30).
6		DAC step waveforms						
	14	V_{CC}	2 24					See waveform photograph (page 31).
	15	Bit supply	701-1690/TP2					See waveform photograph (page 32).
	16	CE supply	701-1690/TP1					See waveform photograph (page 31).
	17	V_{REF} supply	701-1655/TP2					See waveform photograph (page 32).
	18	Load supply	701-1655/TP3					See waveform photograph (page 29).
			The following tests are performed					
			with the UniPak 2™ installed in its					
			normal operating position.					
			Socket/Pin					
7	19	Current DAC step waveform	2 9					Place a 200-ohm, 5W resistor between pins 9 and 12, socket 2. See waveform photo (page 29).
8	20	All votages off	All All	-0.1V		0.4V		
9	21	Socket 2 LED						Confirm that socket 2 LED is on.
	22	V_{CC} supply load	2 24	11.8V		12.1V		Place a 20-ohm, 2W resistor between pins 24 and 12, socket 2.
10	23	Fast V_{CC} supply load	2 24	12.0V		13.0V		Same as above; no LEDs on.

Table 4-3. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P E	DATE
A			10/82
C	ECN 4831		5/83
D	ECN 5023	CB	2/84

UniPak 2™ Measurement Chart

STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
								Ground DMM to socket 7, pin 10
11	24	CE supply load	2 20	32.3V		33.2V		Place a 100-ohm, 10W resistor
								between pins 20 and 12,socket 2.
	25	Pin 18 voltage switch	2 18	32.7V		33.2V		
	26	Pin 21 voltage switch	2 21	32.7V		33.2V		
12	27	Bit supply load	2 11	25.2V		26.0V		Place a 100-ohm, 5W resistor
								between pins 11 and 12,socket 2.
	28	Pin 19 voltage switch	2 19	25.6V		26.2V		
13	29	V_{CC} voltage linearity	2 24	3.90V		4.10V		
	30	CE supply linearity	2 18	23.0V		23.5V		Place a 2.2K-ohm, 1/2W resistor
								between pin 12 and 18,
								socket 2.
	31	Address supply	2 8	4.70V		5.30V		
	32	-5V supply	2 21	-5.2V		-4.8V		
	33	12-volt supply	2 20	11.4V		12.6V		
	34	Clamp supply	2 11	20.5V		21.5V		
	35	Current source linearity	2 11	88 mA		92 mA		Use a 100-ohm, 2W carbon
								comp resistor in series with
								the current meter.
14	36	V_{CC} voltage linearity	2 24	4.90V		5.10V		

Table 4-3. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P E	DATE
A			10/83
C	ECN 4831		5/83
D	ECN 5023		2/84

UniPak 2™ Measurement Chart

STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
								Ground DMM to socket 7, pin 10
	37	CE supply linearity	2 21	11.4V		12.0V		
	38	Clamp supply linearity	2 9	6.7V		7.3V		
15	39	V_{CC} voltage linearity	2 24	5.90V		6.10V		
	40	I source and pulldowns	2 9,11,14,16	2.0V		2.6V		
	41	I source and pulldowns	2 10,13,15,17	0.0V		1.0V		
16	42	I source and pulldowns	2 10,13,15,17	2.0V		2.6V		
	43	I source and pulldowns	2 9, 11, 14, 16	0.0V		1.0V		
17	44	Socket 1 LED						Confirm that socket 1 LED is on.
	45	V_{CC} voltage supply	1 28	4.90V		5.10V		
	46	Odd address and data	1 2,3,5,7,9,11,13,16,18,	3.5V		6.0V		
		high	20,22,24,26					
	47	Even address and data	1 1,4,6,8,10,12,15,17,19,21,	-0.1V		0.4V		
		low	23,25,27					
18	48	Odd address and data	1 2,3,5,7,9,11,13,16,18,	-0.1V		0.4V		
		low	20,22,24,26					
	49	Even address and data	1 1,4,6,8,10,12,15,17,19,21,	3.5V		6.0V		
		high	23,25,27					
19	50	Odd data lines high	1 11,13,16,18	25.5V		26.5V		
	51	Even data lines pullups	1 12,15,17,19	4.5V		5.5V		

Table 4-3. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A			10/82
C	ECN 4831		5/83
D	ECN 5023		2/84

UniPak 2™ Measurement Chart

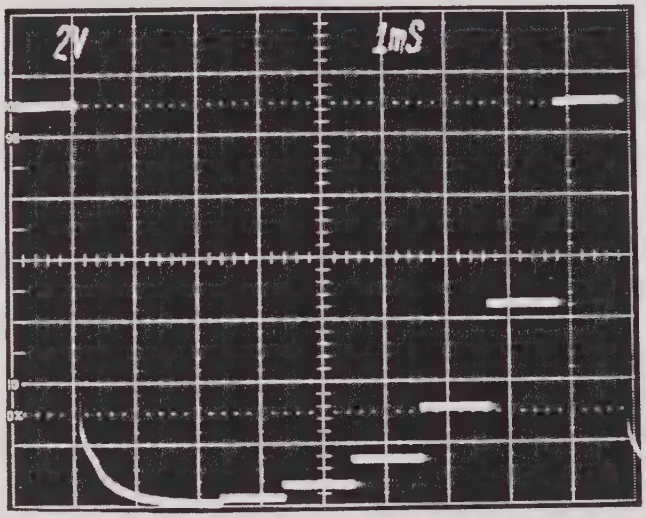
STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION		MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
									Ground DMM to socket 7, pin 10
20	52	Odd data lines pullups	1	11,13,16,18	4.5V		5.5V		
	53	Even data lines high	1	12,15,17,19	25.5V		26.5V		
21	54	Socket 3 LED							Confirm that socket 3 LED is on.
	55	V_{CC} voltage supply	3	20	4.90V		5.10V		
22	56	Socket 4 LED							Confirm that socket 4 LED is on.
	57	V_{CC} voltage supply	4	16	4.90V		5.10V		
23	58	Socket 5 LED							Confirm that socket 5 LED is on.
	59	V_{CC} voltage supply	5	16	4.90V		5.10V		
24	60	Socket 6 LED							Confirm that socket 6 LED is on.
	61	V_{CC} voltage supply	6	18	4.90V		5.10V		
25	62	Socket 7 LED							Confirm that socket 7 LED is on.
	63	V_{CC} voltage supply	7	20	4.90V		5.10V		
26	64	V_{CC} pullup 1 on	1	28	4.0V		5.2V		
		V_{CC} pullup 2 on	2	24	4.0V		5.2V		
		V_{CC} pullup 3 on	3	20	4.0V		5.2V		
		V_{CC} pullup 4 on	4	16	4.0V		5.2V		
		V_{CC} pullup 5 on	5	16	4.0V		5.2V		
		V_{CC} pullup 6 on	6	18	4.0V		5.2V		
		V_{CC} pullup 7 on	7	20	4.0V		5.2V		

Sheet 5 of 5

Measurement Chart

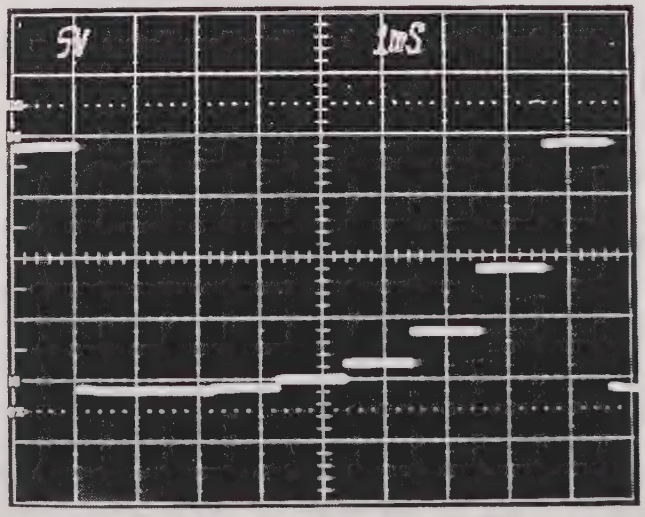
PROGRAM ELECTRONICS UNIPAK 2™

DAC Step Waveform



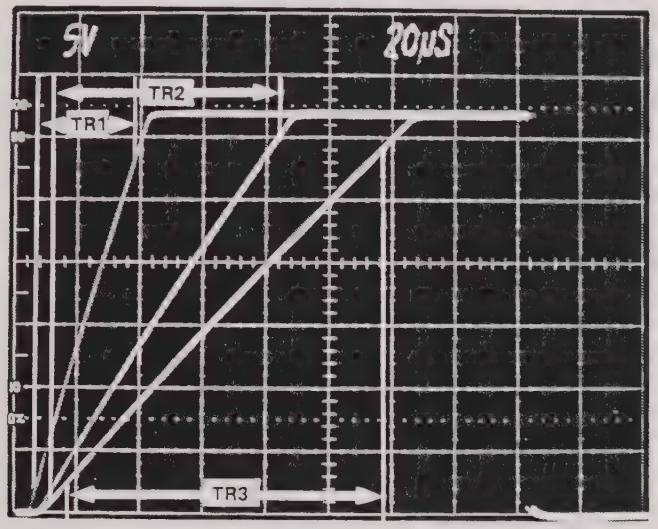
LOAD SUPPLY DAC

Current DAC Step Waveform



DATE	REV	REVISION RECORD	DR	CK
10-82				
3-84				CTZ

Bit Switch Rise-Time Waveform



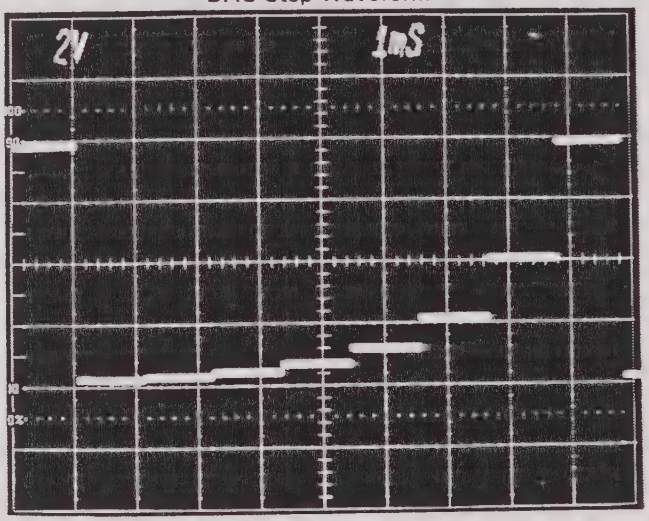
	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	TR1	29	33	37	μs	
	TR2	62	66	70	μs	Adjust R1, 701-1690.
	TR3	90	100	110	μs	

NOTE: All TR's are measured from 10% to 90%.

Measurement Chart

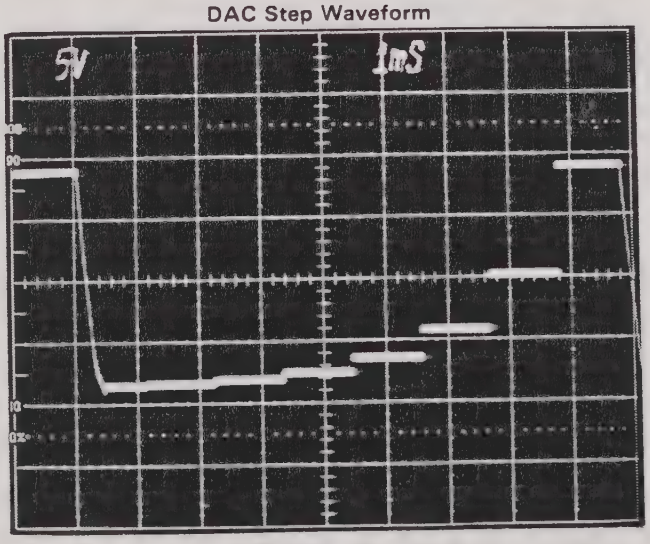
PROGRAM ELECTRONICS UNIPAK 2™

DAC Step Waveform



V_{CC} DAC

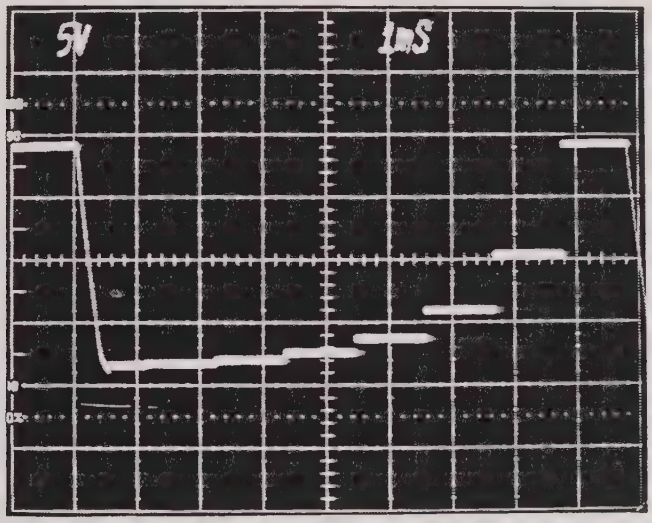
DAC Step Waveform



$\overline{CE}$ SUPPLY DAC

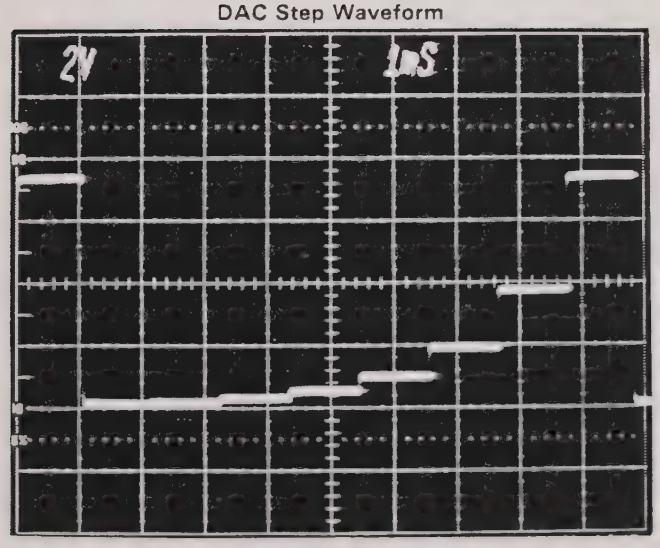
DATE	REV	REVISION RECORD	DR	CK
10-82				
3-84				CTJ

DAC Step Waveform



BIT SUPPLY DAC

DAC Step Waveform



V_{REF} SUPPLY DAC

This page left intentionally blank.

SECTION 5
CIRCUIT DESCRIPTION

5.1 OVERVIEW

This section defines the functions of UniPak 2™ principal hardware components. Each circuit-card assembly is depicted by a block diagram accompanied by a written description.

5.2 GENERAL ARCHITECTURE

5.2.1 The Link Between the UniPak 2™ and the Programmer

The UniPak 2™ is controlled by the programmer's extended processor bus through the UniPak 2™ mating connector (J1). The control software for the UniPak 2™ is located in EPROM on the memory card (702-1650).

5.2.2 The Buses

The programmer's address bus, data bus, R/$\overline{W}$ line and $\overline{V \bullet \emptyset_2}$ line access the software on the memory card and control the gates and registers on the waveform generator (701-1690) and address cards (701-1655). The UniPak 2™'s device bus gathers the programming waveforms produced by these cards and transmits them to the socket card (702-1659). Figure 5-1 shows the relationships between the buses.

5.3 COMPONENT LAYOUT

The principal components of the UniPak 2™ are the motherboard, the waveform generator, the address card, the socket card, and the memory card. The component layout of the UniPak 2™ is shown in figure 5-2 and described in the following subsections.

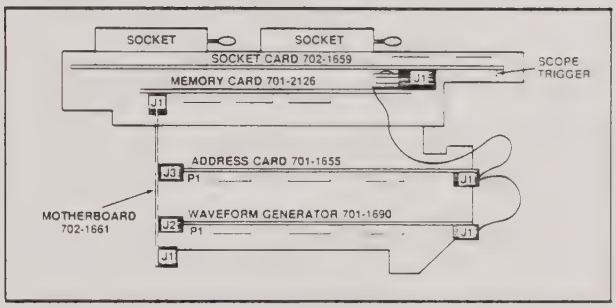


Figure 5-2. Principal Components

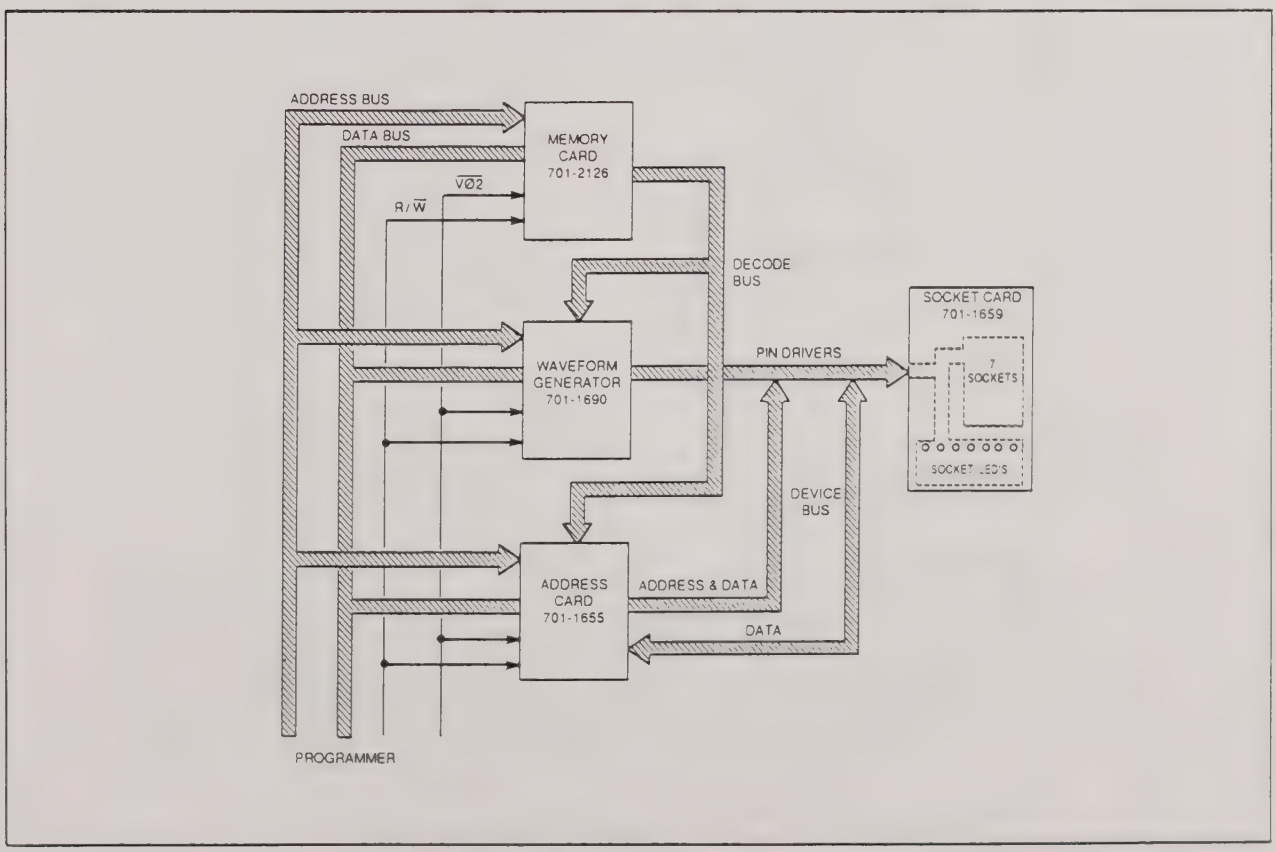


Figure 5-1. Block Diagram, UniPak 2™ Electronics

5.3.1 Motherboard

The motherboard accepts the signals and power supplies from the J6 of the programmer and transmits them to two identical 72-pin edge connectors and a 50-pin edge connector (see figure 5-3 and schematic 30-702-1661).

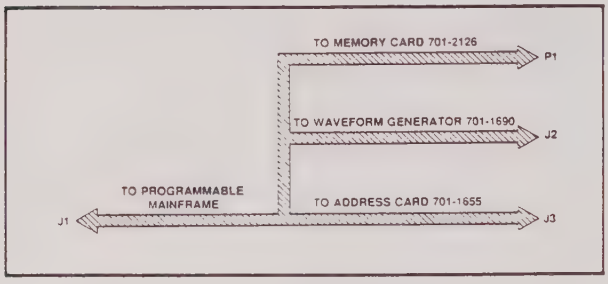


Figure 5-3. Block Diagram, Motherboard

5.3.2 Waveform Generator

The waveform generator provides signals required for programming devices. These signals are generated by the blocks shown in figure 5-4.

Three major supplies are the V_{CC} supply, the $\overline{CE}$ supply and the bit supply, which are used to generate the respective signals. Each supply is software-controlled via a D/A converter. All DACs obtain their reference voltage from the DAC reference.

The V_{CC} waveforms are generated by writing appropriate DAC values from the firmware. The rise and fall times are fixed by the slewing rate of the op amp. Two overcurrent detectors are included, one for low currents and one for high currents (above 1 amp). If a detector is activated, the control latch is reset; the DAC-reference kill output then causes the DAC reference to go to zero, in turn causing all supplies to return to zero.

The V_{CC} supply senses the V_{CC} voltage at the PROM socket via the V_{CC} sense line. This remote sensing compensates for all cable drops between the supply and the socket.

The $\overline{CE}$ waveforms are generated by using the $\overline{CE}$ supply in conjunction with one of the pin switches. The voltage level is selected by writing the appropriate value to the $\overline{CE}$ DAC. One of two rise times is selected by the control latch and rise-time control circuitry. Either the pin 18, 20 or 21 switch can be enabled by the switch-control latch to output the high-level $\overline{CS}$ voltage. Switches that are not enabled can output TTL levels.

Each pin switch consists of an emitter follower with the collector tied to the $\overline{CE}$ supply. A current source is provided for the base of each switch to charge the common rise-time capacitor. When the base is released, a linear ramp is generated which is truncated at the $\overline{CE}$ supply level. An NPN-transistor pulldown is included in the switch to provide a 20V/μs controlled fall time. Logic circuitry prevents the pulldown and pullup circuits from being active simultaneously.

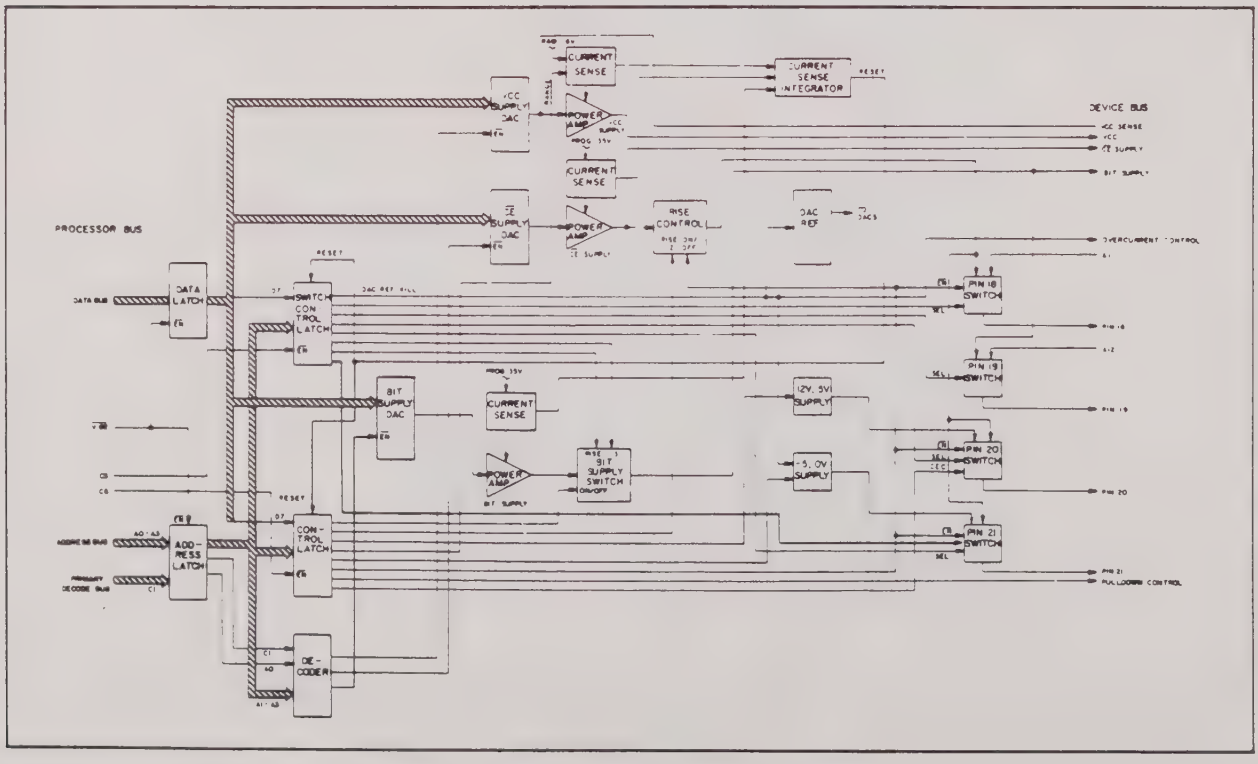


Figure 5-4. Block Diagram, Waveform Generator

The pin 21 switch uses the same principles as the pin 18 and pin 20 switches. However, a power amplifier output (0/-5V supply) provides the ground reference for the switch. For certain programming algorithms this amplifier output is brought to -5V.

The pin 20 switch includes a pullup that is connected to the +12/+5V supply, thus allowing the switch in the TTL mode to switch from 0 to 12V as well as from 0 to 5V. The +12/+5V supply consists of a monolithic regulator and a 5.1V zener diode controlled by the switch-control latch.

Signals to be applied to the data lines of a device are generated with the bit-supply signals and controlled by the bit-supply switch. The bit supply is nearly identical to the $\overline{CE}$ supply, but has one less diode in the feedback path, compensating for one less drop in the switch paths. The bit-supply switch consists of an emitter follower, a current source, and three rise-time control capacitors. The collector of the emitter follower is connected to the bit supply; the base is connected to the current source and timing capacitor. The control latch can select the timing capacitor and also control the base of the switch. When the base is released, the output ramps linearly to the bit-supply level. The output on the bit-supply switch is sent to the address card and to the pin 19 switch; unlike the pin 20, 21 and 18 switches, the pin 19 switch consists of a simple PNP-saturating switch controlled by the switch-control latch.

The current-sense integrator smoothes the transient overcurrent pulses occurring from charging supply capacitors. When an overcurrent condition from the V_{CC}, $\overline{CE}$, bit or (0/-5V) supply exists for sufficient time, the control latch is reset, in turn causing the DAC reference and the supplies to go to zero. The state of the overcurrent-control line can be read by the address card and used by the programmer to detect shorted devices.

Table 5-1 lists the functions of the device-bus pins. The data latch buffers the data bus and holds data to satisfy the long DAC data-hold requirement. The address latch buffers the lower-order address lines and the primary decode bus. These buffered lines are then sent to the decoder and the address latches. The decoder provides decode signals to the DACs for the V_{CC}, $\overline{CE}$ and bit supplies. The switch-control latch and the control latch receive their clocks from a decoder on the address card.

Table 5-1. Pin Functions, Device Bus (at J1)

Pin	Function	Pin	Function
1	PA_8	26	PA_1
2	PA_9	27	PA_6
3	PA_{10}	28	PA_5
4	PA_{11}	29	PA_4
5	PA_{12}	30	PA_3
6	PA_{13}	31	PA_2
7	PA_{14}	32	PA_1
8	PA_{15}	33	PA_0
9	GND	34	Vcc
10	Vcc Sense	35	GND
11	$\overline{CE}$ Supply	36	GND
12	Bit Switch	37	Bit Supply
13	Pin 20	38	Pin 18
14	Pin 21	39	Pin 19
15	Scope Trigger	40	PD_1
16	-9V	41	PD_2
17	+24V	42	PD_4
18	$\overline{\text{Overcurrent}}$	43	PD_4
19	$\overline{\text{Pull-Down Control}}$	44	S1
20	$\overline{\text{Vcc Pull-Up Control}}$	45	S2
21	Address Supply +5V Select	46	$\overline{S3}$
22	PD_8	47	$\overline{\text{Vcc Pulse}}$
23	PD_7	48	Address DAC
24	PD_6	49	-5V
25	PD_5	50	Bit Switch Control

5.3.3 Address Card

The address card, illustrated in figure 5-5, provides the device address, device data, data loads and supply measurement capability of the UniPak 2™.

The address drivers consist of addressable latches driving the device address bus. The addressable latches receive data from the most-significant-bit line of the data bus.

The data switch register drives PNP data switches which direct the output of the bit switch to the appropriate device-data line. The PNP switches are driven by current sources to provide a constant-base drive at all bit-switch voltages.

The data sink register is used to shunt programming currents to ground. Device data is read via the data comparators and strobed to the processor bus via the data gate. The comparators receive their reference voltage from the V_{REF} amplifier, which is controlled by the V_{REF} DAC. Loading the device data bus is controlled by the load DAC, the load amplifier and the high/low-range load switch. This supply develops a voltage that is applied to either the low-range or high- and low-range load resistor banks. These resistors are fed through isolation diodes, which are connected to the device data pins. The load sink register enables the UniPak 2™ to select which device data pins will have loads applied to them. The diode clamps limit the voltage applied by the load resistors to the data bus to approximately 5V when the load clamp switch is closed.

The supply comparators read the V_{CC}-sense line, the $\overline{CE}$ supply and the bit-switch line. The comparator gate/multiplexer strobes the data from the supply comparators and the overcurrent-read line to the most significant-bit line of the data bus.

The socket-select latch provides a control line for the high-/low-range switch and control lines for the socket card.

The data latch buffers the data bus and holds data to satisfy the DAC requirements.

The current source latch will supply a 4-mA current to a device provided there is a 15V zener diode inside the device on pin 18, 19 or 20. The address supply 5V select determines whether the address supply DAC or a fixed 5V will be applied to PA0-PA3.

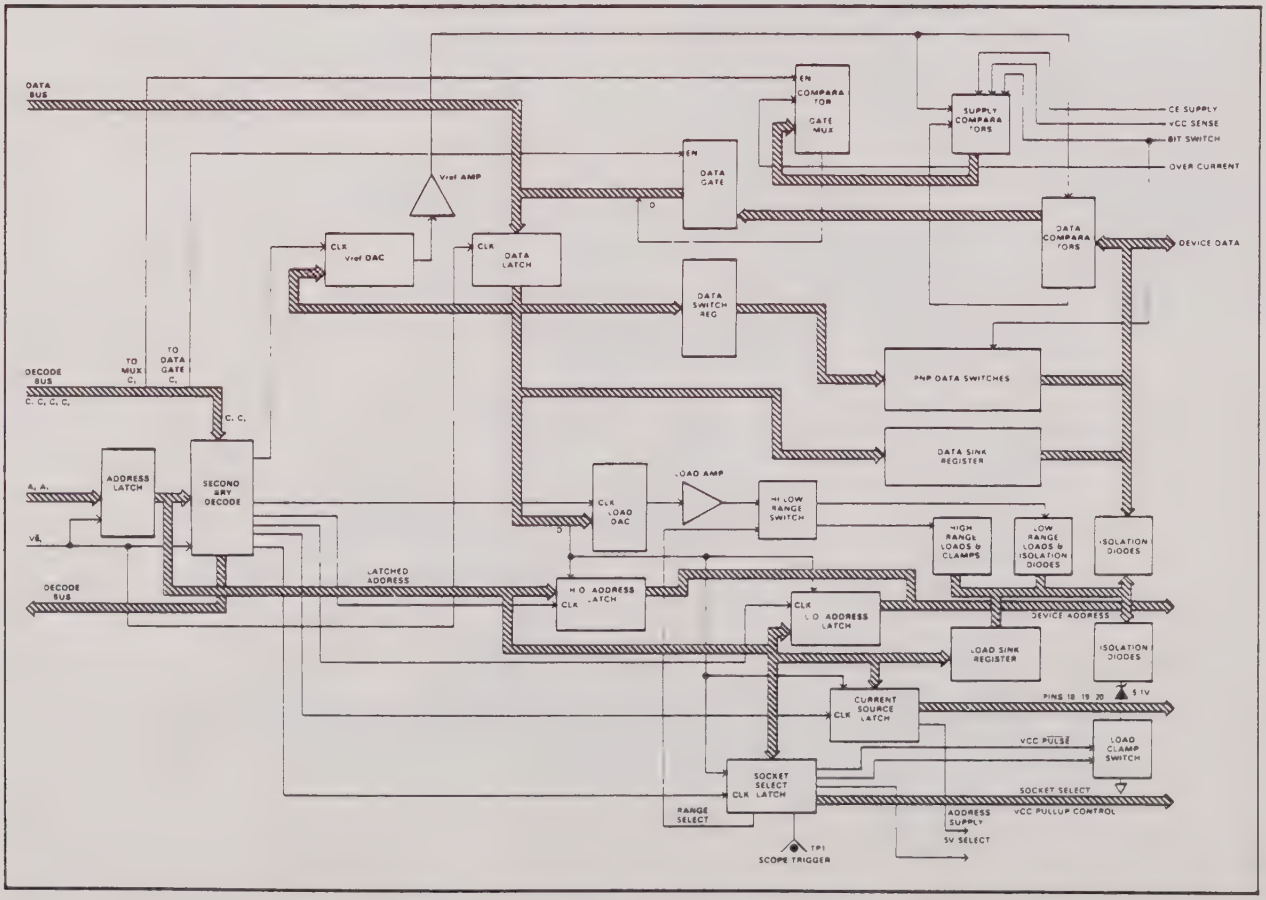


Figure 5-5. Block Diagram, Address Card

The address latch buffers low-order addresses for the secondary decoder. The secondary decoder provides the appropriate signals for the DACs and registers, as well as the latches on this card and on the waveform generator. The $\overline{V \bullet \emptyset_2}$ signal controls the timing of the various clock signals developed by the decoder.

5.3.4 UniPak 2™ Socket Card

The socket card distributes to the device sockets the signals developed on the address card and the waveform generator (refer to figure 5-6).

The device address bus (PA0-PA15) is generated on the address card and fed to the socket card via the ribbon cable. On the socket card, the bus is fed into CMOS buffers. The address supply DAC connects to the V_{DD} supply on these buffers. This allows the VOH level to be under DAC control. The address supply 5V select line allows PA0-PA3 to switch at TTL levels while all other address lines switch between "0" and the address supply level. The address clamps provide overvoltage protection and are connected to a comparator that senses overvoltage, shutting down all the supplies when excessive voltage is detected.

The device-data bus connects directly to all sockets. Four-bit devices are connected to PD1-PD4. The data pulldowns consist of 1K-ohm resistors and a diode network. The data clamp has two modes of operation controlled by the bit switch control line.

When voltage pulses are being applied to a device, the pass element of the data clamp is switched out of the circuit. The op amp and 2.2K-ohm resistor precharge the 0.1 μF capacitors to the level set by the bit supply so that the network does not absorb energy from the actual data-line programming pulses.

When current pulses are being applied to a device, the pass element is switched into the circuit. The data clamp will be set to a voltage level by the bit supply and will sink all unnecessary current.

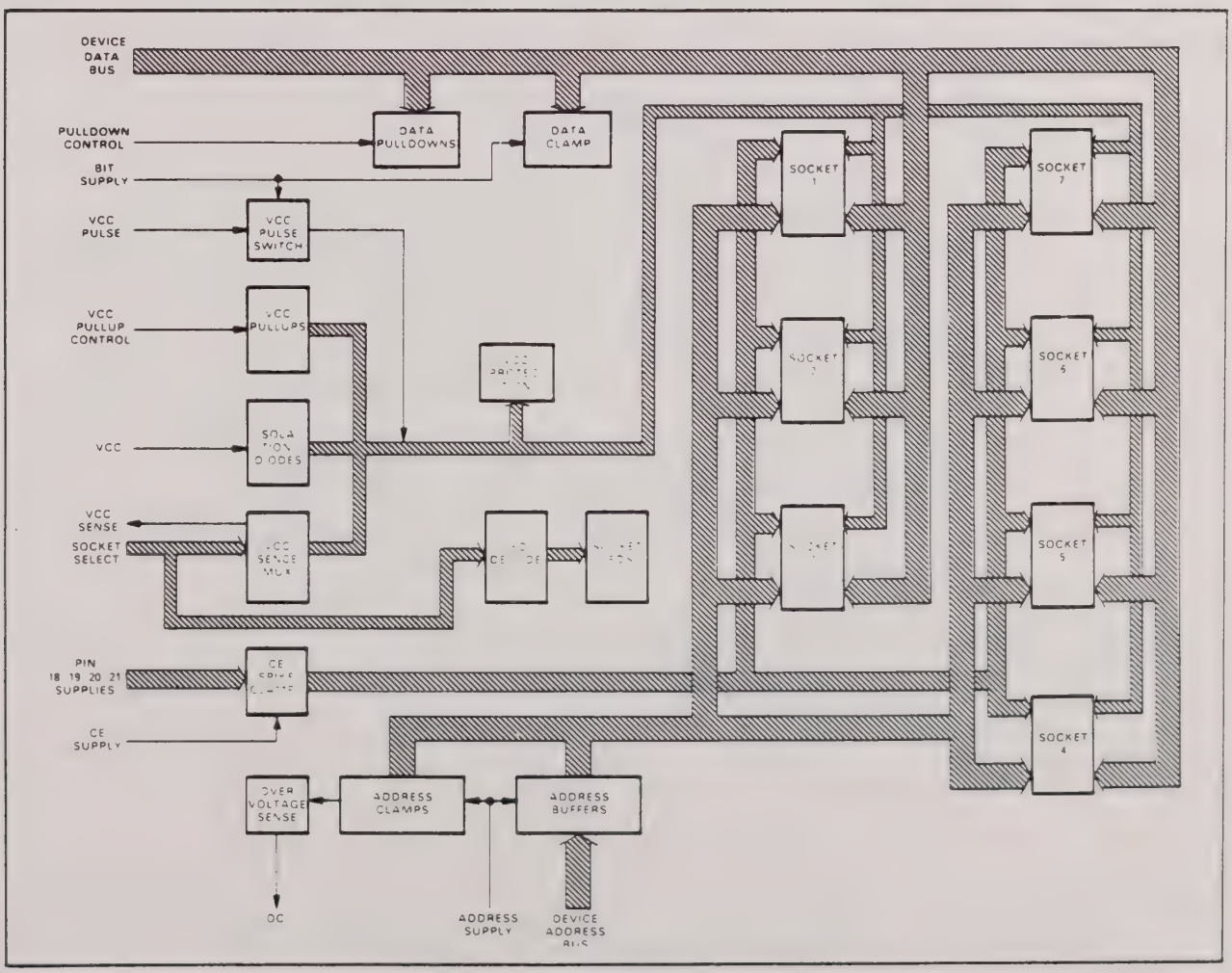


Figure 5-6. Block Diagram, Socket Card

Pins 18, 19, 20 and 21 of the 24-pin device socket receive signals directly from the waveform generator via the corresponding pin switches. A spike-suppression network is provided where the $\overline{CE}$ supply charges the RC network. V_{CC} is applied to all sockets through seven diodes. Remote sensing of the voltage at the selected socket is provided by the analog switch of the V_{CC}-sense multiplexer. When V_{CC} is brought to zero, the device's V_{CC} lines can be pulled up by the V_{CC} pullups. The V_{CC} sense-multiplexer and a comparator on the address card are then used to read the V_{CC} voltage. If a device is properly inserted in a socket, the V_{CC} voltage will be above 2V. If it is in backwards it will be below 1V, and if no device is in the socket, the voltage will approach 4V.

The V_{CC} pulse switch is used to switch from a level set by the V_{CC} supply to a level set by the bit supply. The switch uses a HEX JFET with an RC network to control the rise and fall times. When the HEX FET is switched on, the V_{CC} isolation diode is reversed biased and the V_{CC} sense line sees a dummy load. The V_{CC} pulse switch is applied only to the 24-pin socket. When the switch is on, the .01 μF decoupling capacitor for the 24-pin socket is switched off.

The LED decoder is used to light the LEDs below the selected socket.

5.3.5 Memory Card

The UniPak 2 memory card block diagram is shown in figure 5-7. EPROMs which store the UniPak 2 firmware are contained on the memory card. These EPROMs connect to the address bus and the data bus through the address latch and data buffer respectively.

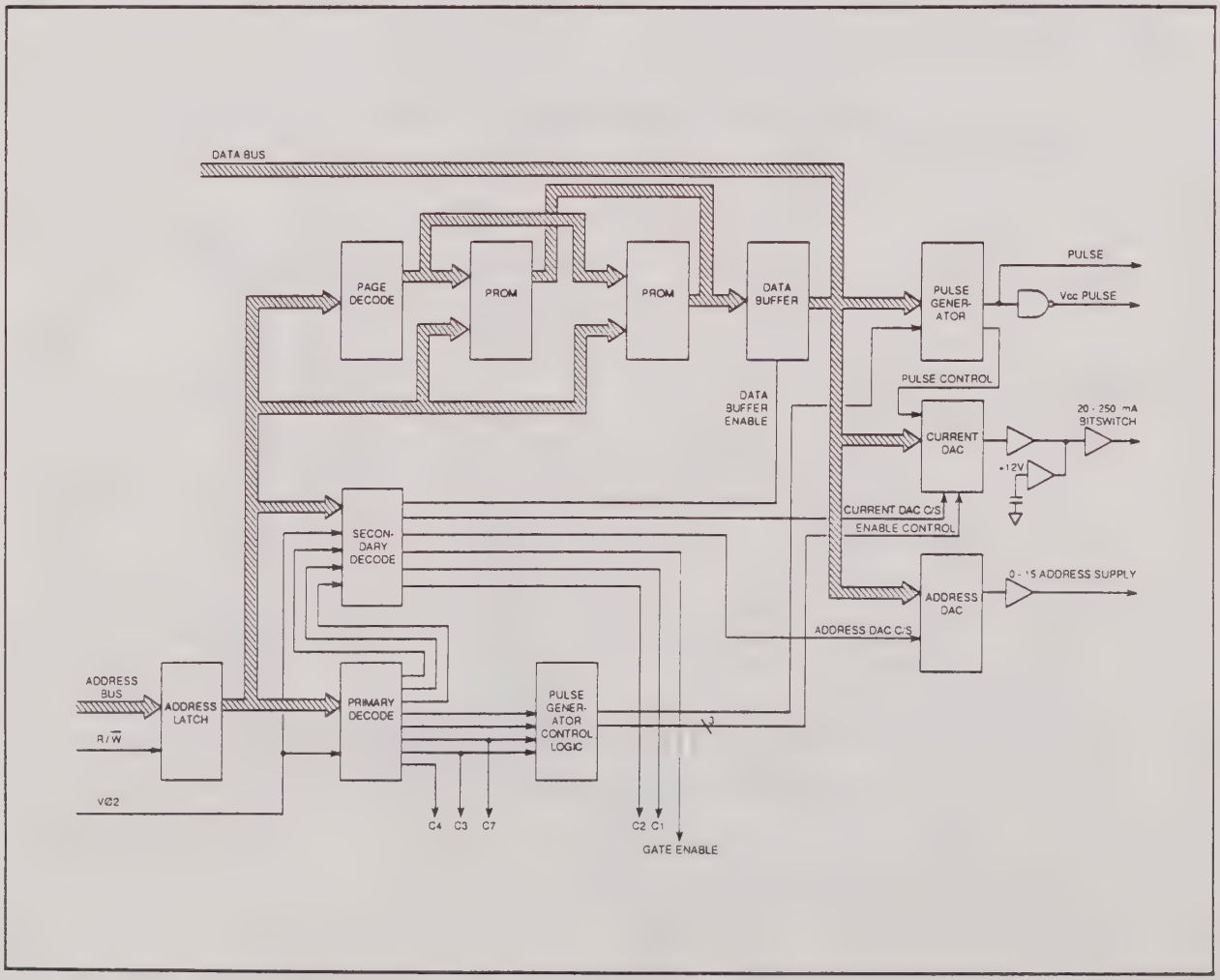


Figure 5-7. Block Diagram, Memory Card

The high order EPROM addressing and chip select is decoded with a PAL. Two PALs comprise the primary decoding for the entire UniPak 2. The EPROMs connect to the 12 low-order address lines and the $V \bullet \emptyset_2$ line. Outputs from the primary-decoder PAL connect to the secondary decoder PAL and also to secondary decoders on the address card and the waveform generator. Additional outputs from the secondary decoder PAL enable the data buffer during all software-read operations and lower the data gate enable line during any access of the UniPak 2. The primary and secondary decode PALs also control the pulse generator, current source, and address supply.

The pulse generator consists of a count-up ripple counter, an 8-bit latch, and a 10-mHz crystal-controlled clock. The latch is connected to the data bus and is used to load the counter, allowing the pulse generator to be programmable between 0.1 and 25.5 *u*s.

The current source consists of a fixed 20-mA current source and a programmable current source. The control logic selects which current source is active. The pulse generator can be selected to control the programmable current source.

The address supply generates the voltage necessary to drive the CMOS buffers located on the socket card. The voltage is generated from the 24V power supply using an NPN transistor driven by an op amp. The input of the op amp is a DAC, which allows the voltage to be software selectable.

This page left intentionally blank.

ERROR CODES

NOTE

In the case of an error condition, be sure that the family and pinout codes are correct for the PROM installed; refer to the Device List earlier in Appendix A to cross check family and pinout codes.

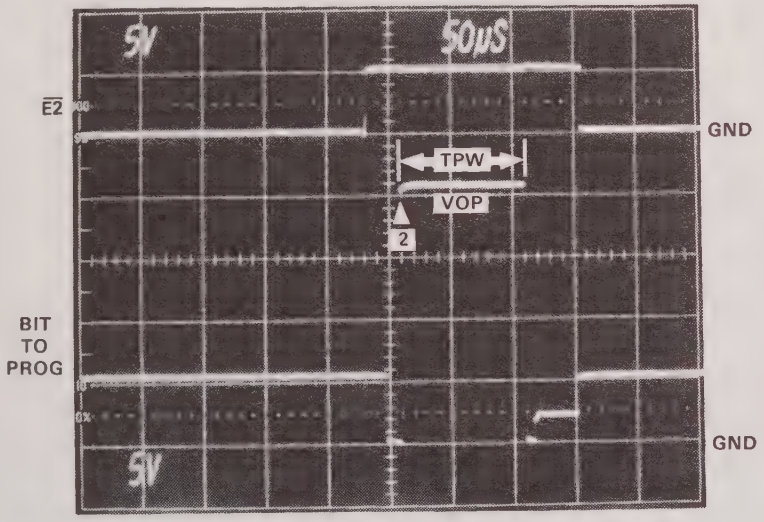
CODE	NAME	DESCRIPTION
21	Illegal-Bit Error	The device cannot be programmed due to already programmed locations of incorrect polarity.
23	First-Pass Verify Error	The device data was incorrect on the first pass of the automatic verify sequence during device programming.
24	Second-Pass Verify Error	The device data was incorrect on the second pass of the automatic verify sequence during device programming.
27	Insufficient RAM	Due to the value of the Begin RAM Address, there is insufficient RAM to program the device, or the total allotment of RAM resident is less than the word limit of the device.
30	No Programming Algorithm	Valid family and pinout codes are not selected, or family code selection not followed by pinout code selection.
31	Excessive Current Drain	The operation aborted due to excessive current drain by a device.
32	Backward Device	The operation aborted due to V_{CC} level test indicating a backward device.
35	Faulty Chip Select	The operation aborted due to data being present while a device is disabled.
37	Socketing Error	Operation is aborted due to a low V_{CC} level indication on sockets presumed to be empty. A device may be in the wrong socket, or two or more devices may be socketed simultaneously.
38	Illegal Operation During Calibration	An illegal or invalid operation was attempted during calibration.
39	Failure to Lock Security Fuse	The security bit did not program and the device is not locked.

CODE	NAME	DESCRIPTION
70	Faulty Bit Supply	The operation aborted due to a faulty bit supply. Do not use UniPak 2 until repaired.
71	Faulty CS Supply	The operation aborted due to a faulty CS supply. Do not use UniPak 2 until repaired.
72	Faulty Vcc Supply	The operation aborted due to a faulty Vcc supply. Do not use UniPak 2 until repaired.
A1	No Identifier Found	The device does not have an electronic identifier. The electronic identifier mode cannot be used.
A2	Invalid Identifier	The electronic identifier of the device has been read and it indicates that the device cannot be programmed using the selected family and pinout codes. Consult the Device List for the correct family and pinout codes. Try again using these codes.
B0	Byte Erase Error	The device does not have a byte erase mode. Block limits must be removed and a chip erase performed. The entire chip may then be reprogrammed.
B1	Chip Erase Error	The device does not have a chip erase mode.
B5	Invalid Pinout	This pinout will not work with this programming mainframe configuration.

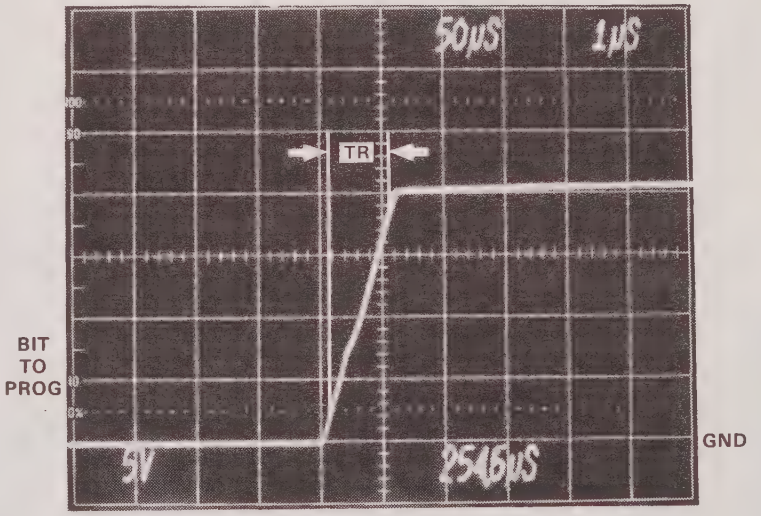
APPENDIX B
TIMING DIAGRAMS

The timing diagrams are no longer a part of the UniPak 2 manual; however, they are available for purchase from the Data I/O Corporate Service department.

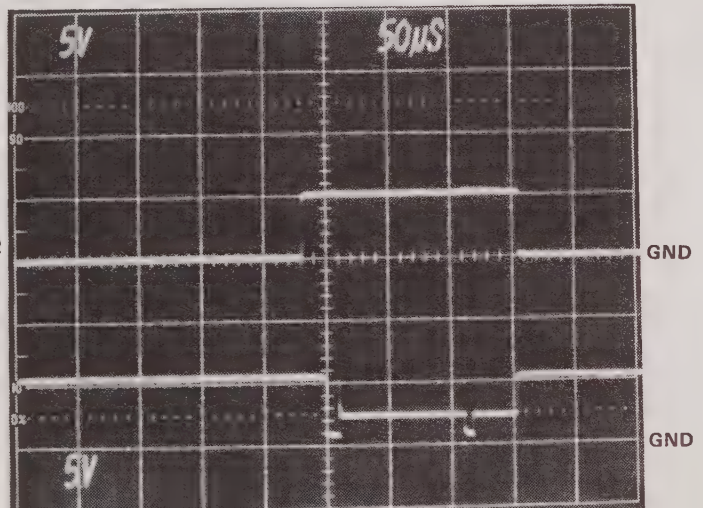
APPENDIX B
TIMING DIAGRAMS

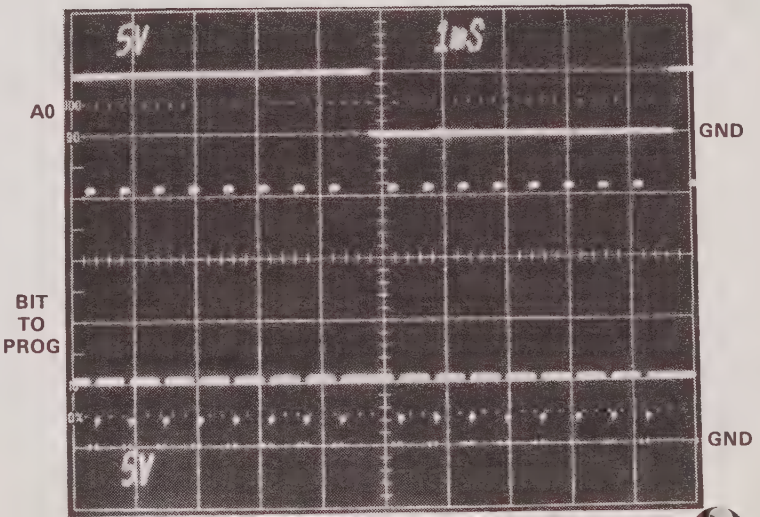

5V
50µS
E2
GND
TPW
VOP
2
BIT
TO
PROG
GND
5V

1


50µS
1µS
TR
BIT
TO
PROG
GND
5V
2546µS

2


5V
50µS
E2
GND
BIT
NO
PROG
GND
5V


5V
1mS
A0
GND
BIT
TO
PROG
GND
5V

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP	20.0	20.5	21.0	V	
	TPW	90	100	110	µs	
	TR	0.5	1.0	3.0	µs	
	TF					NA
	Reject		8		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.3	4.4	4.5	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	7.0	8.0	9.0	V	701-1655/TP4
	Low Load	7.0	8.0	9.0	V	701-1655/TP3
2ND PASS VERIFY	VCC	4.9	5.0	5.1	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	7.0	8.0	9.0	V	701-1655/TP4
	Low Load	7.0	8.0	9.0	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 01.*
2. *Load RAM with hex 01 for Family 02.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ	11/82
		ECN #4831		KH	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 01, 02

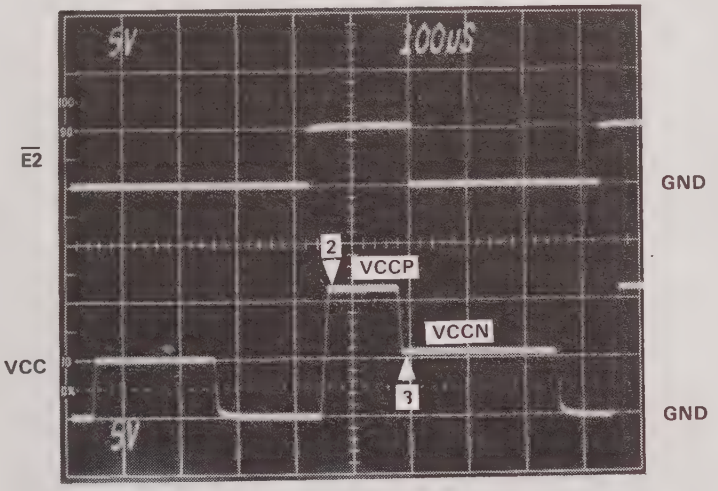
DRAWN BY: PAP

CHECKED BY:

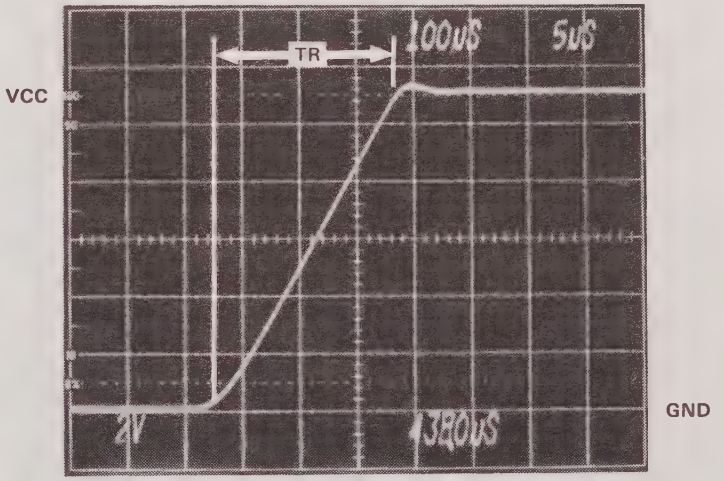
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

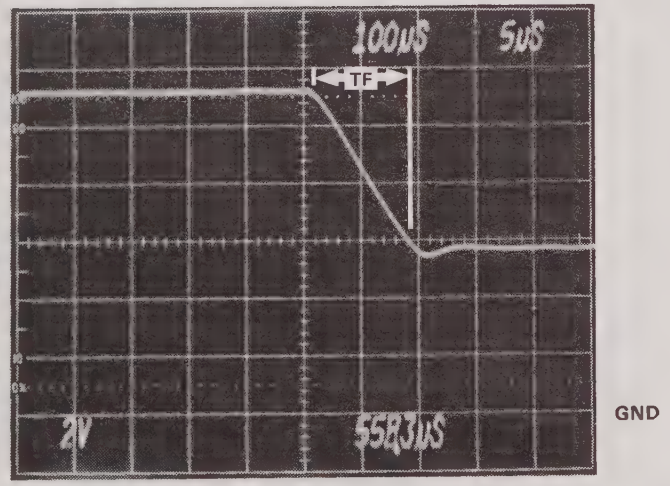
SHEET 1/1


5V
100uS
E2
GND
2
VCCP
VCCN
VCC
3
GND
5V

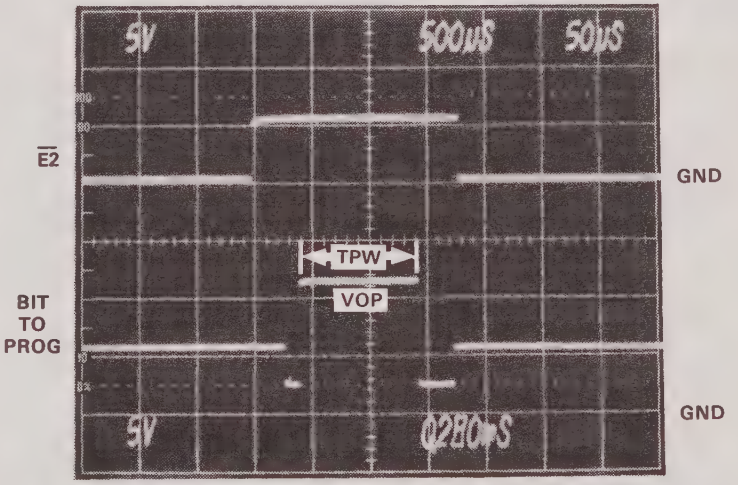
1


TR
100uS
5uS
VCC
GND
2V

2


100uS
5uS
TF
VCC
GND
2V

3


5V
500uS
50uS
E2
GND
TPW
VOP
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	10.8	11.0	11.2	V	
	VCCN	5.3	5.5	5.7	V	
	VOP	10.5	11.0	11.5	V	
	TPW	90	100	110	μs	
	TR	17		31	μs	See Note 3
	TF	8		18	μs	See Note 3
	Reject		8		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	HIGH LOAD	15.5	16.5	17.5	V	701-1655/TP4
	LOW LOAD	15.5	16.5	17.5	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	1.6	1.7	1.8	V	701-1655/TP2
	HIGH LOAD	12.5	13.5	14.5	V	701-1655/TP4
	LOW LOAD	12.5	13.5	14.5	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 05.*
2. *Load RAM with hex 01 for Family 06*
3. *Load VCC with a 100Ω, 2-watt resistor.*

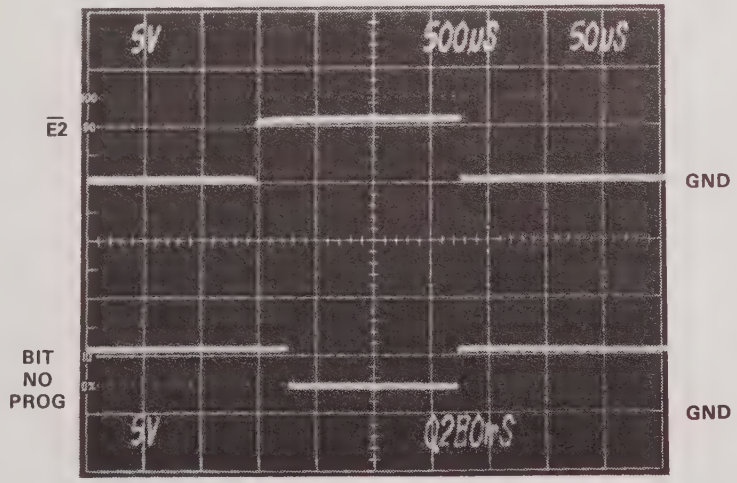
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

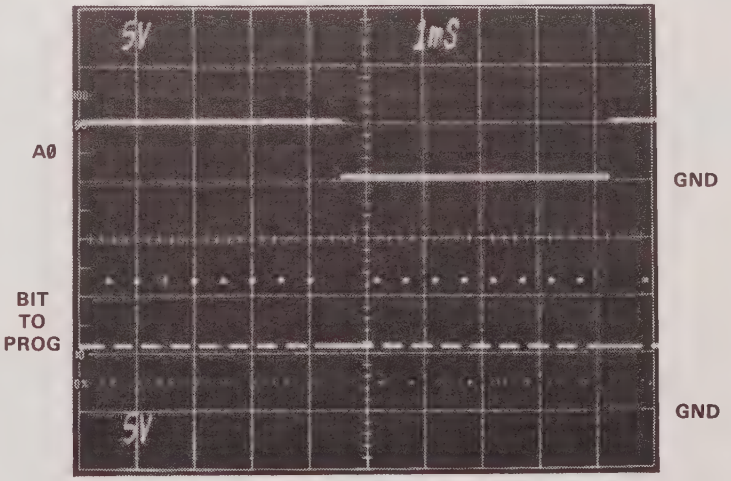
TIMING DIAGRAM

FAMILY CODES 05, 06

DATA I/O


5V
500uS
50uS
E2
GND
BIT
NO
PROG
5V
Q2BOmS
GND

5


5V
1mS
A0
GND
BIT
TO
PROG
5V
GND

6

REVISIONS

LTR	DESCRIPTION	P.E.	DATE

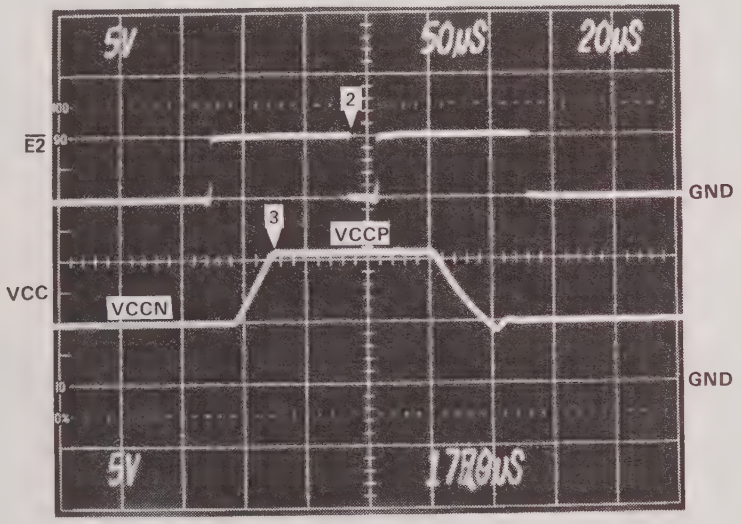
Sheet 2 of 2

TIMING DIAGRAM

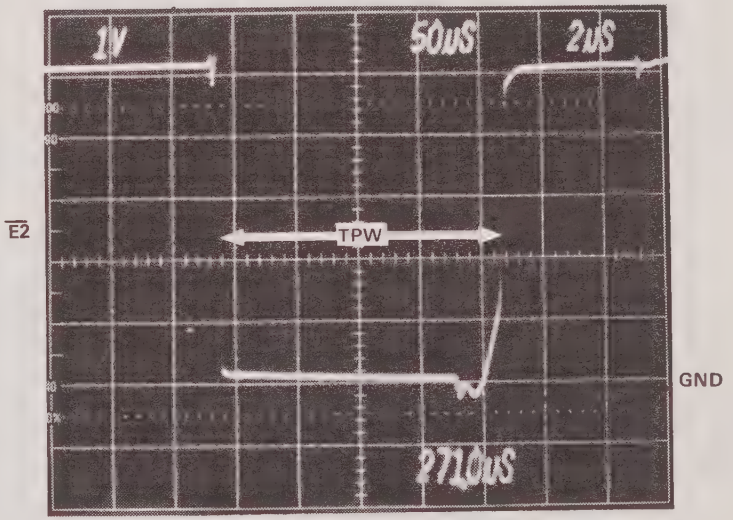
FAMILY CODES 05, 06

DATA I/O

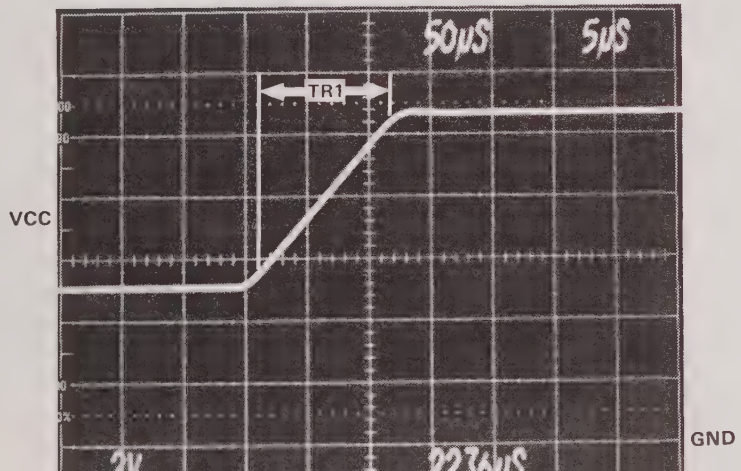
0526/1282

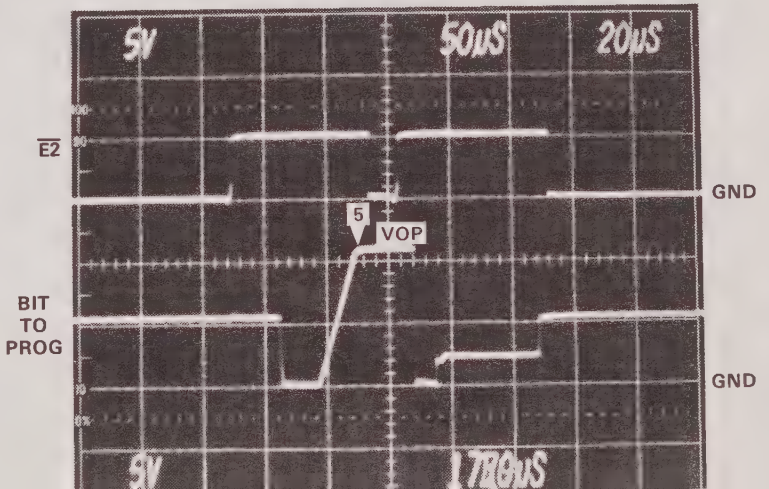

5V
50µS
20µS
2
E2
GND
3
VCCP
VCC
VCCN
GND
5V
1780µS

1


1V
50µS
2µS
E2
TPW
GND
2710µS

2


50µS
5µS
TR1
VCC
GND
2V
2236µS


5V
50µS
20µS
E2
GND
5
VOP
BIT
TO
PROG
GND
5V
1780µS

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	10.0	10.5	11.0	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	10.0	10.5	11.0	V	
	TPW	9.0	10.0	11.0	µs	
	TR1	1		25	µs	See note 3
	TR2	1		15	µs	
	TF					NA
	Reject		14		Pulses	
	Overprogram		5		Pulses	
1ST PASS VERIFY	VCC	3.9	4.0	4.1	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	6.9	7.9	8.9	V	701-1655/TP4
	Low Load	6.9	7.9	8.9	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	1.6	1.7	1.8	V	701-1655/TP2
	High Load	6.0	7.0	8.0	V	701-1655/TP4
	Low Load	6.0	7.0	8.0	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 07.*
2. *Load RAM with hex 01 for Family 08.*
3. *Load V_{CC} with a 330 Ω ½-watt resistor.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ	11/82
		ECN #4831		XH	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 07, 08

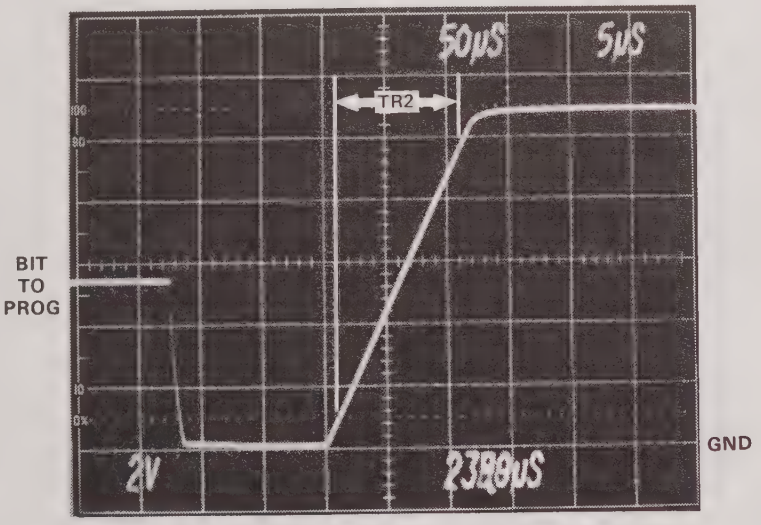
DRAWN BY: ES

CHECKED BY:

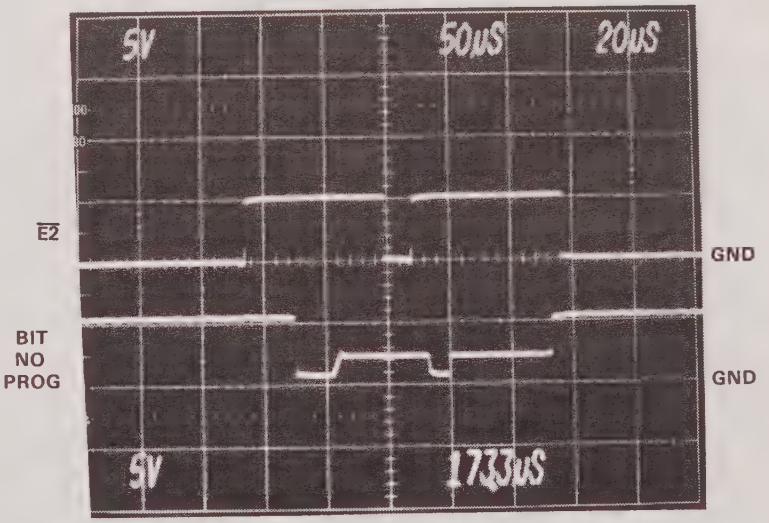
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

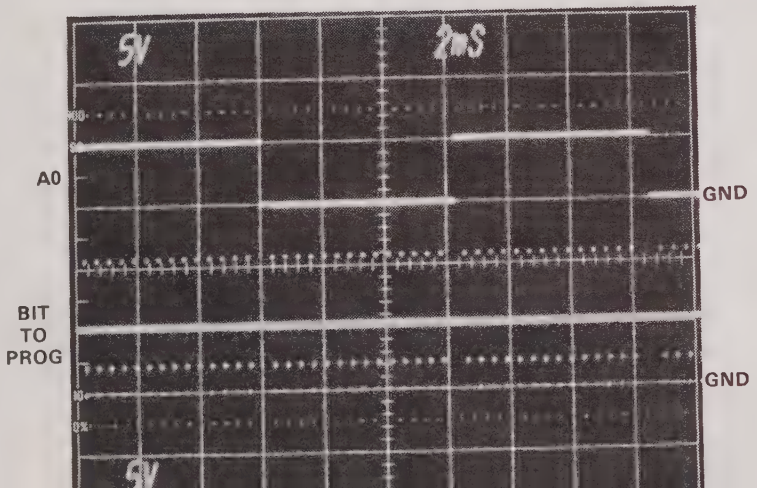
SHEET 1/2


50uS
5uS
TR2
BIT
TO
PROG
GND
2V
2380uS

5


5V
50uS
20uS
E2
GND
BIT
NO
PROG
GND
5V
1733uS

6

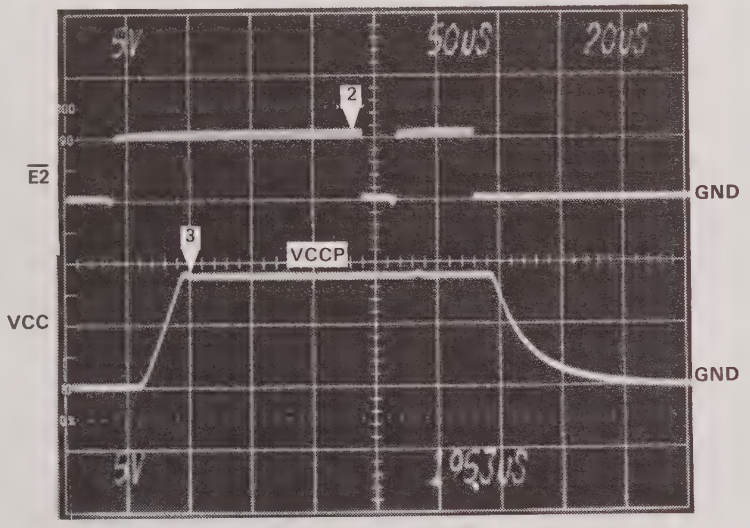

5V
2mS
A0
GND
BIT
TO
PROG
GND
5V

B-11
981-0001

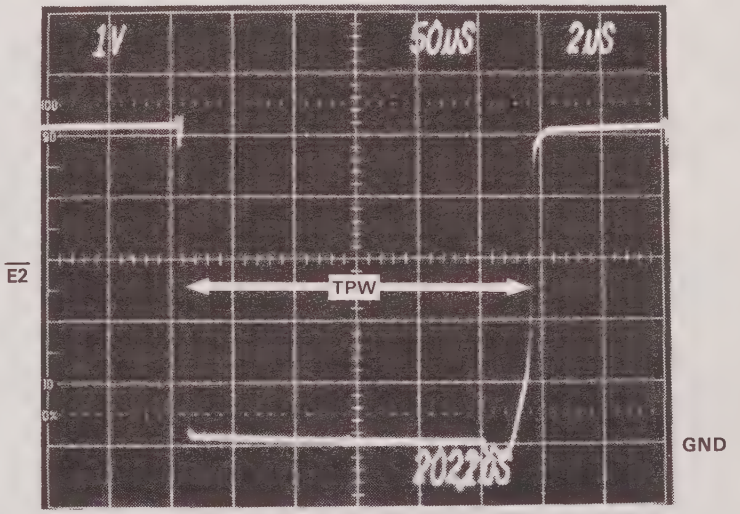
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.S.J.	11/82
		ECN #4831		[illegible]	5/83

DATA I/O ISSAQUAH, WA

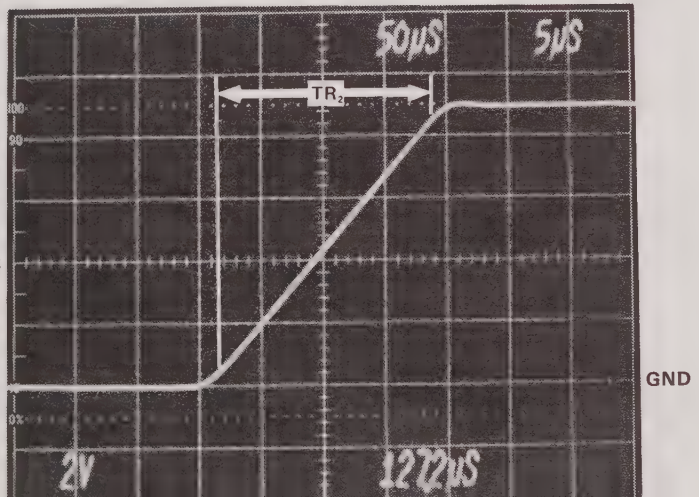
TITLE: TIMING DIAGRAM FAMILY CODES 07, 08			DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059	
SCALE:			SHEET 2/2

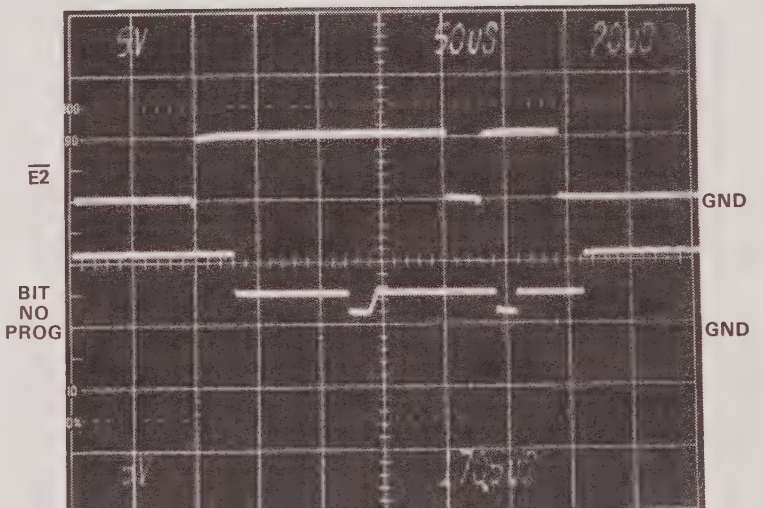

5V
50uS
20uS
2
E2
GND
3
VCCP
VCC
GND
5V

1


1V
50uS
2uS
E2
TPW
GND

2


50µS
5µS
TR2
VCC
GND
2V


5V
50uS
E2
GND
BIT
NO
PROG
GND

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	8.5		9.0	V	
	VOP	17.0	17.5	18.0	V	
	TPW	10		15	µs	
	TR1	15		30	µs	
	TR2	5		25	µs	See note 3
	TF	0.2		10	µs	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	1.4	1.5	1.6	V	701-1655/TP2
	High Load	0	0	0.4	V	701-1655/TP4
	Low Load	4.6	5.1	5.6	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	1.4	1.5	1.6	V	701-1655/TP2
	High Load	0	0	0.4	V	701-1655/TP4
	Low Load	4.6	5.1	5.6	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 09.*
2. *Load RAM with hex 01 for Family 10.*
3. *Load V_{CC} with a 330Ω, ½-watt resistor.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.J.	11/82
		ECN #4831		XX	5/83
		ECN #5023		CJJ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 09, 10

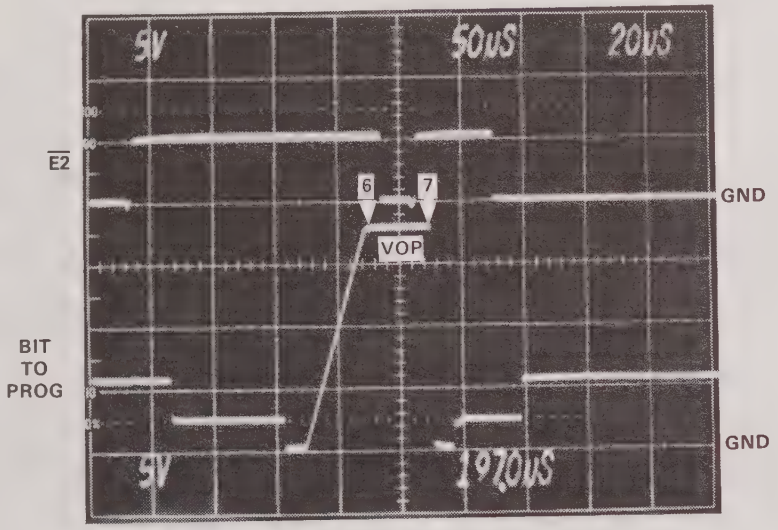
DRAWN BY: ES

CHECKED BY:

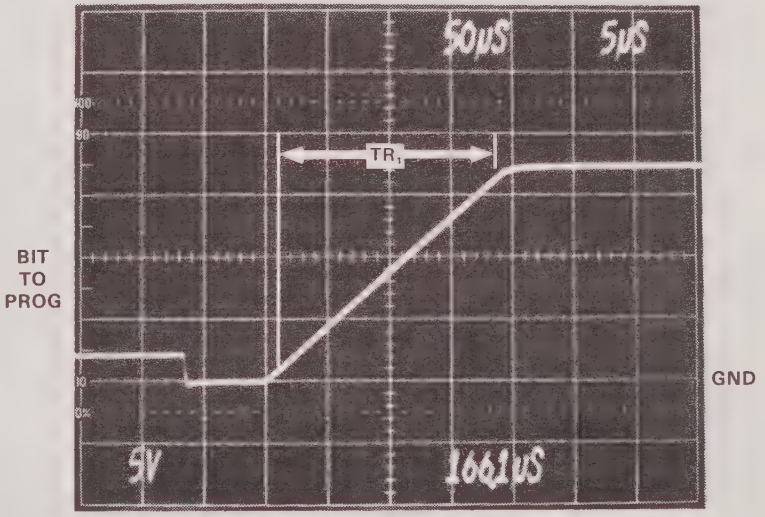
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

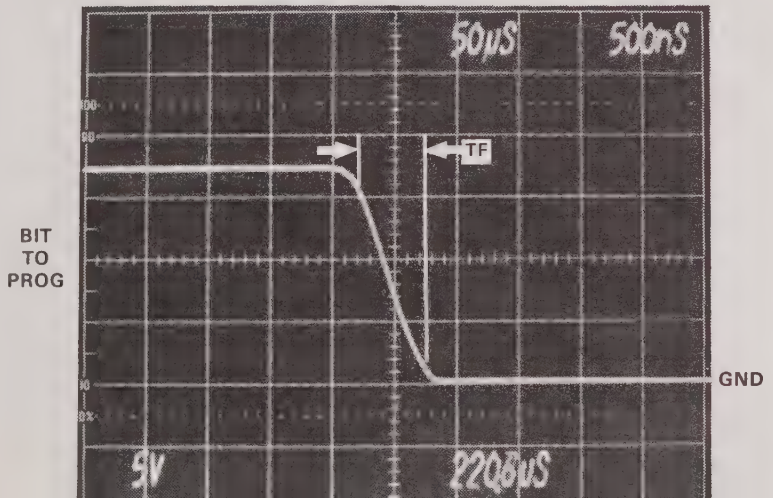
SHEET 1 of 2

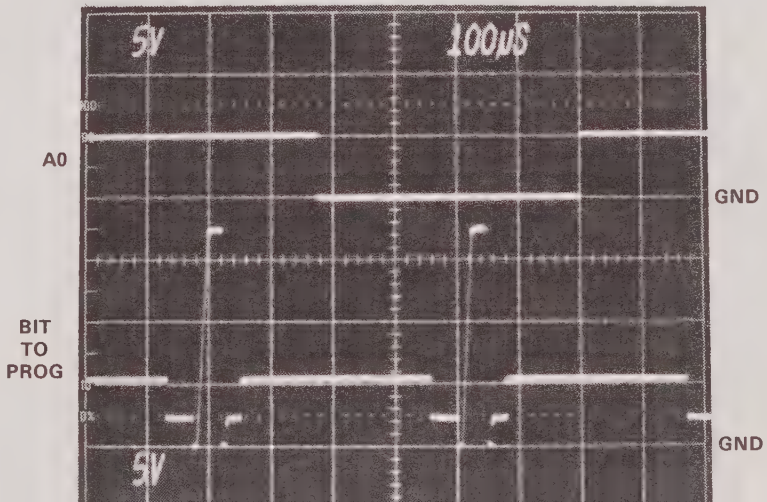

5V
50uS
20uS
E2
6
7
VOP
GND
BIT
TO
PROG
GND
5V
1970uS

5


50µS
5µS
TR1
BIT
TO
PROG
GND
5V
1661uS

6

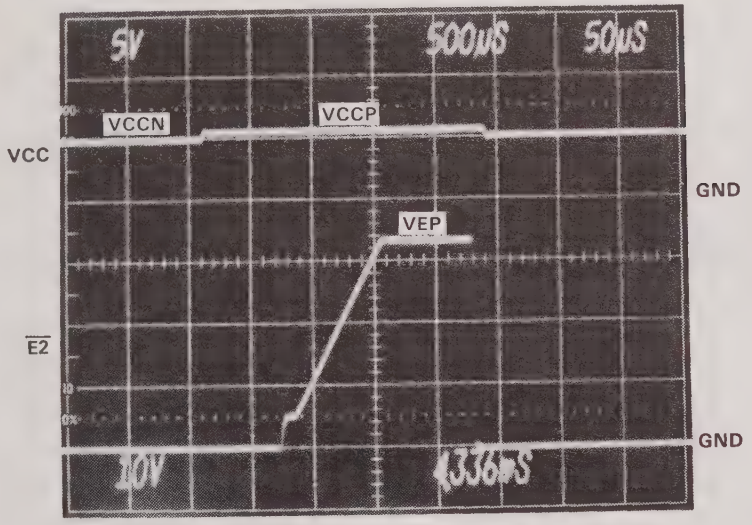

50µS
500nS
TF
BIT
TO
PROG
GND
5V
2208uS


5V
100µS
A0
GND
BIT
TO
PROG
GND
5V

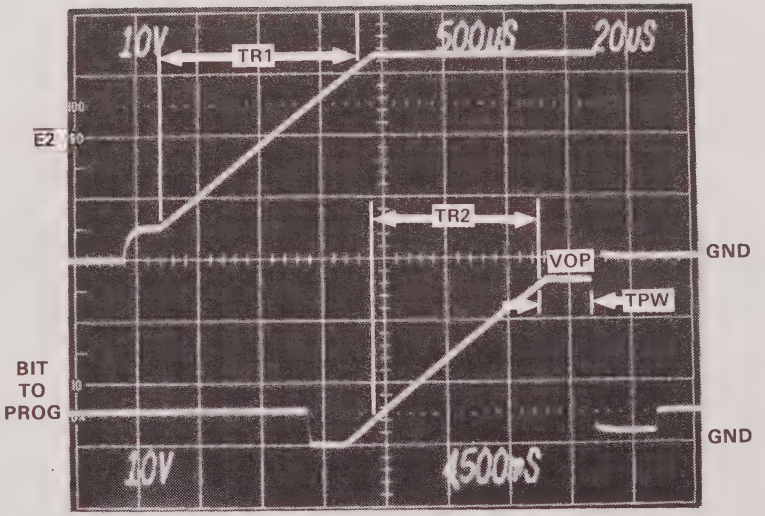
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		ZA	5/83

DATA I/O ISSAQUAH, WA

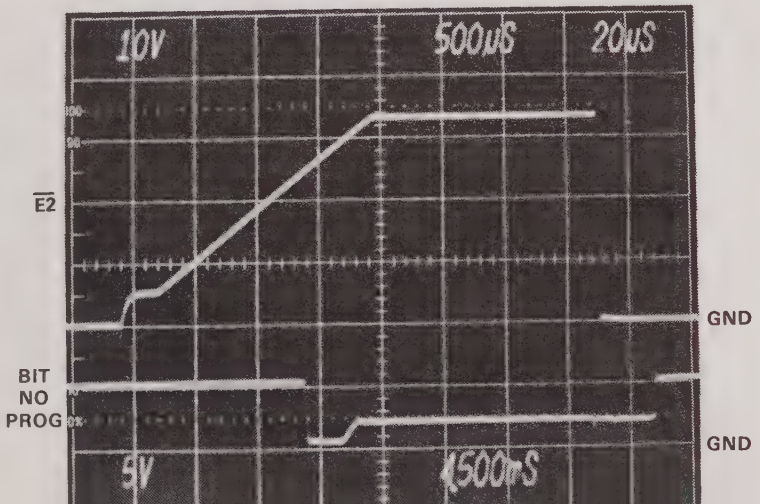
TITLE: TIMING DIAGRAM FAMILY CODES 09, 10		DRAWN BY: ES CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2

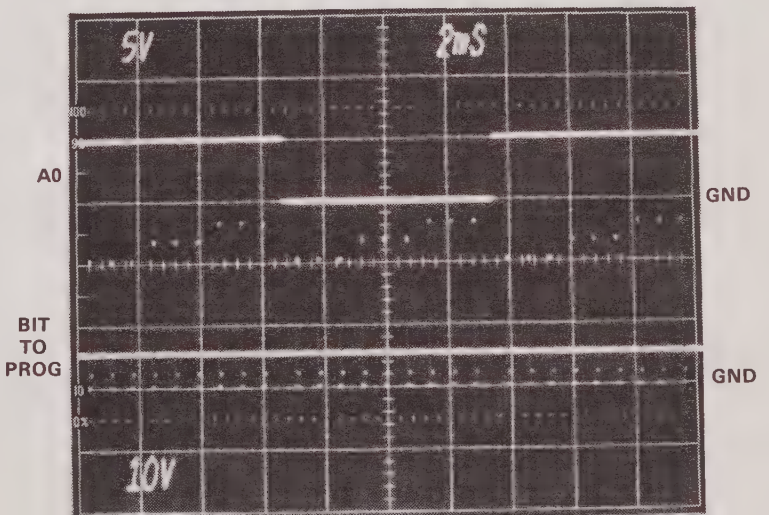

5V
500uS
50uS
VCCN
VCCP
VCC
GND
VEP
E2
GND
10V
1336mS

1


10V
TR1
500uS
20uS
E2
TR2
VOP
GND
TPW
BIT
TO
PROG
GND
10V
1500mS

2


10V
500uS
20uS
E2
GND
BIT
NO
PROG
GND
5V
1500mS


5V
2mS
A0
GND
BIT
TO
PROG
GND
10V

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.4	5.5	5.6	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	19	20	21	V	Pulses 1-3
		22	23	24	V	Pulses 4-6
		25	26	27	V	Pulses 7-9
	VEP	26	27	28	V	Pulses 1-3
		29	30	31	V	Pulses 4-6
		32	33	34	V	Pulses 7-9
	TPW	10		40	µs	See Note 3
	TR1	53	66	88	µs	See Note 4
	TR2	42	52	69	µs	See Note 4
	TF					NA
	Reject		9		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.1	4.2	4.3	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	17.9	18.9	19.9	V	701-1655/TP4
	Low Load	17.9	18.9	19.9	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	2.9	3.0	3.1	V	701-1655/TP2
	High Load	0	0	0.4	V	701-1655/TP4
	Low Load	4.6	5.6	6.6	V	701-1655/TP3

NOTES

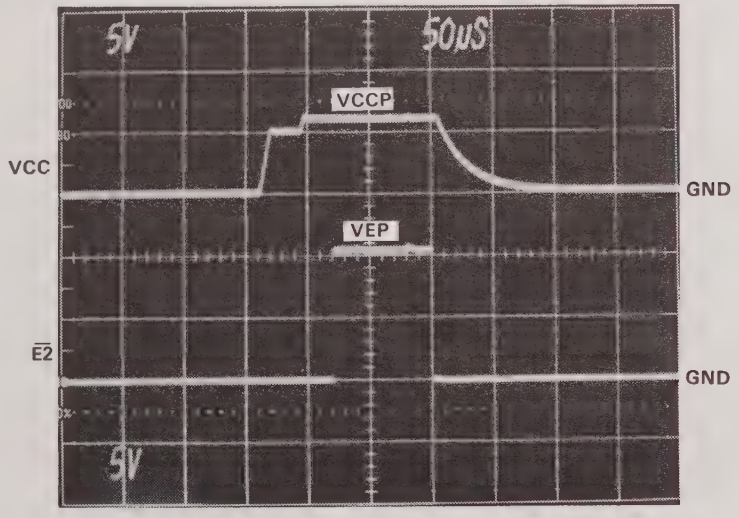
1. *Load RAM with hex FE for Family 11*
2. *Load RAM with hex 01 for Family 12.*
3. *This is measured at the 90% level of the pulse, and all three pulse levels must meet this specification.*
4. *This is measured from 10% to 90% on the tallest pulse.*

REVISIONS

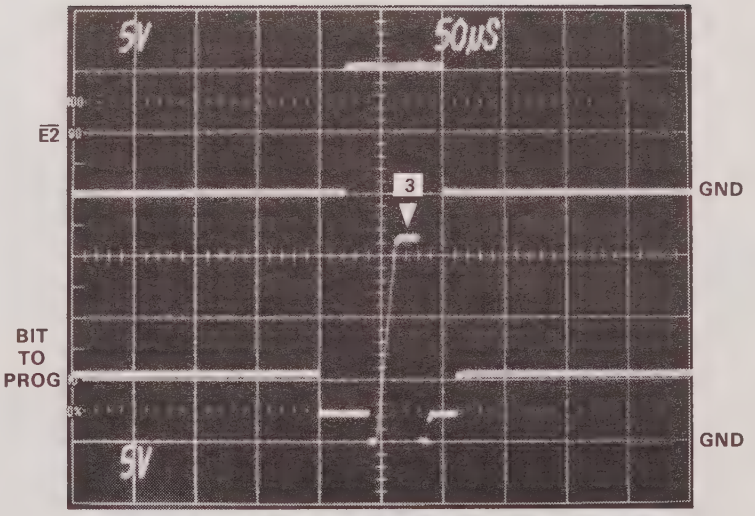
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		ZH	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

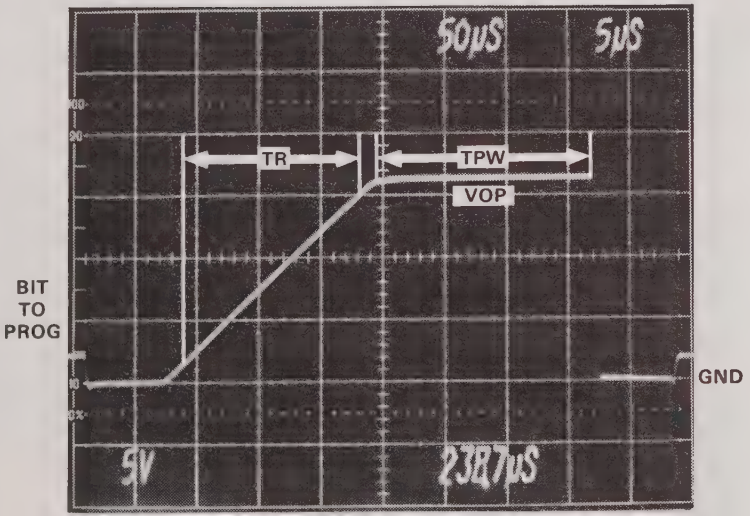
TITLE: TIMING DIAGRAM		DRAWN BY: ES
FAMILY CODES 11, 12		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/1

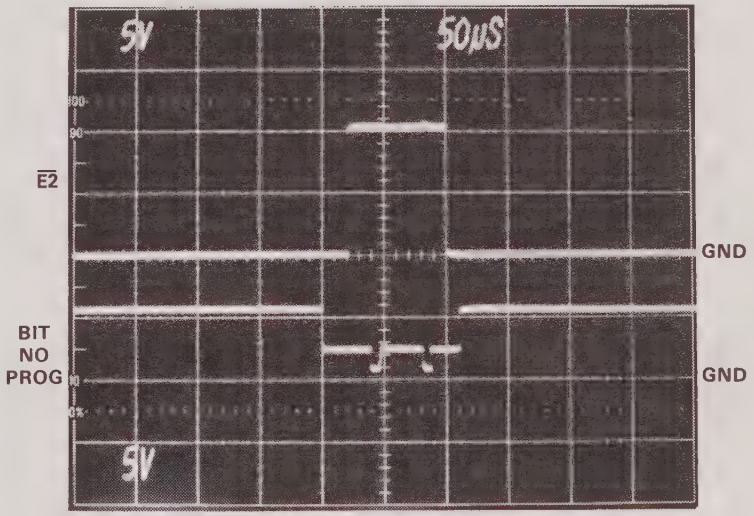

5V
50µS
VCCP
VCC
GND
VEP
E2
GND
5V

1


5V
50µS
E2
3
GND
BIT
TO
PROG
GND
5V

2


50µS
5µS
TR
TPW
VOP
BIT
TO
PROG
GND
5V
2387µS


5V
50µS
E2
GND
BIT
NO
PROG
GND
5V

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.0	6.25	V	
	VOP	15.75	16	16.25	V	
	VEP	9.75	10	11.0	V	
	TPW	15		20	µs	
	TR	10	15	20	µs	
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	0.9	1.0	1.1	V	701-1655/TP2
	High Load	16.3	17.3	18.3	V	701-1655/TP4
	Low Load	16.3	17.3	18.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	2.9	3.0	3.1	V	701-1655/TP2
	High Load	0	0	0.4	V	701-1655/TP4
	Low Load	12.6	13.6	14.6	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 13.*
2. *Load RAM with hex 01 for Family 14.*
3. *Photo 6 is for registered devices.*
4. *Load V_{CC} with a 330 Ω, ½-watt resistor.*

REVISIONS

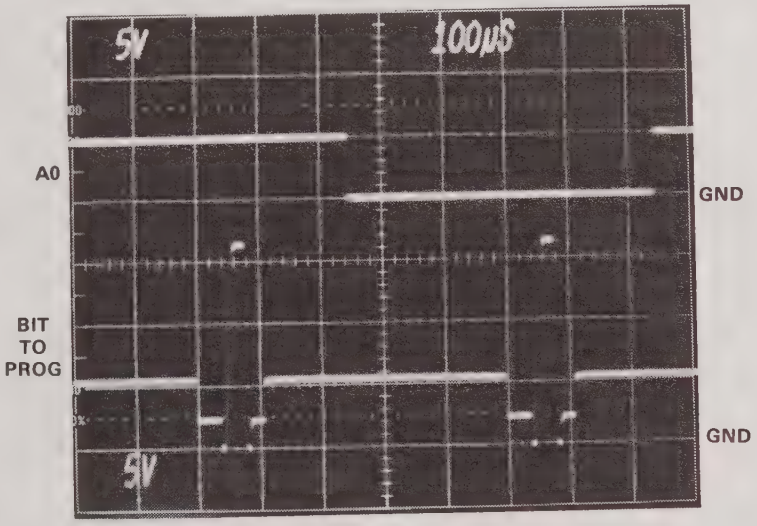
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ	11/82
		ECN #4831		JZ	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

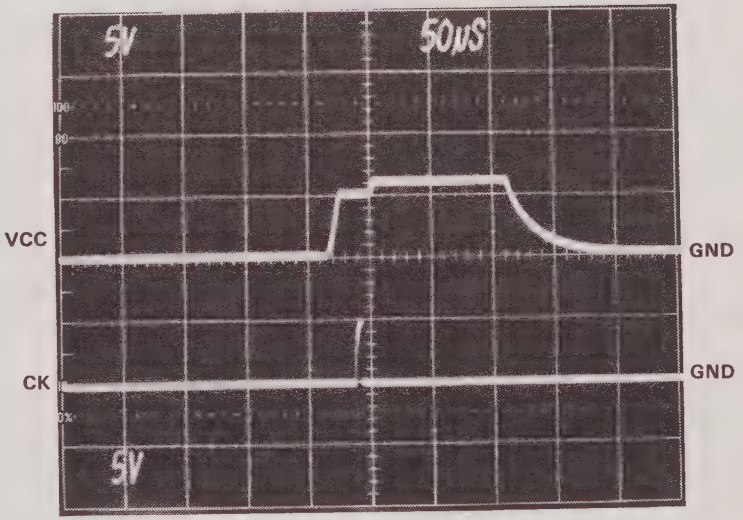
TITLE: TIMING DIAGRAM	DRAWN BY:
FAMILY CODES 13, 14	CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE | SHEET 1/2



5

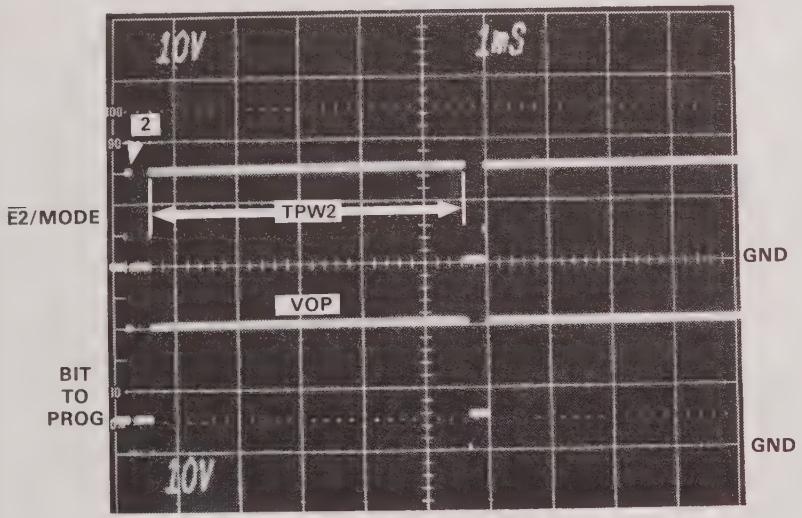


6

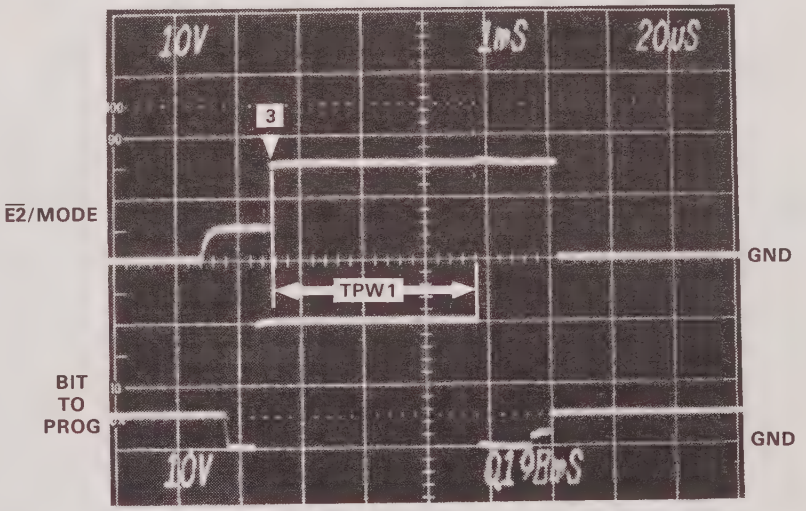
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.J.	11/82
		ECN #4831		XX	5/83

DATA I/O ISSAQUAH, WA

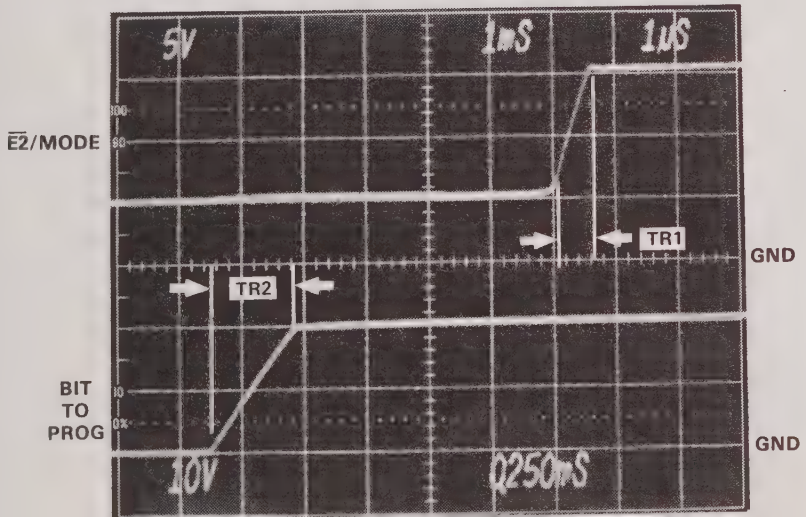
TITLE: TIMING DIAGRAM FAMILY CODES 13, 14		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2

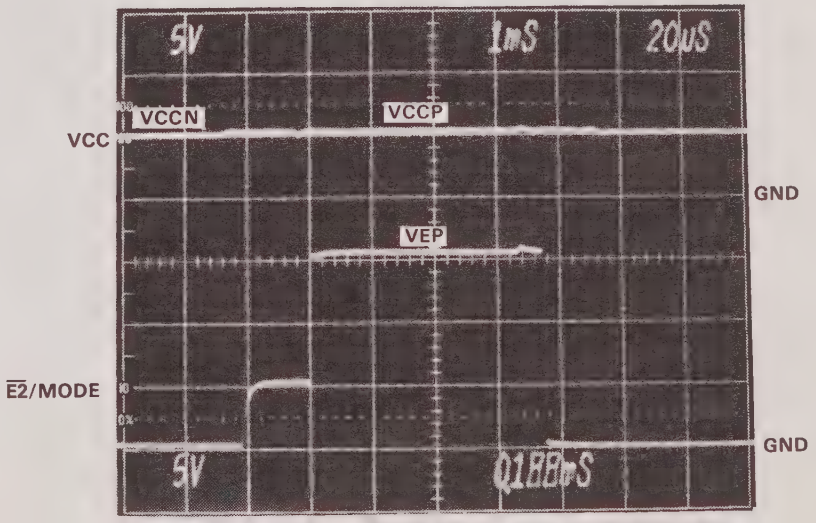

10V
1mS
2
E2/MODE
TPW2
GND
VOP
BIT
TO
PROG
GND
10V

1


10V
1mS
20uS
3
E2/MODE
GND
TPW1
BIT
TO
PROG
GND
10V

2


5V
1mS
1uS
E2/MODE
TR1
GND
TR2
BIT
TO
PROG
GND
10V
Q250mS


5V
1mS
20uS
VCCN
VCCP
VCC
GND
VEP
E2/MODE
GND
5V
Q1BBmS

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.0	5.25	5.5	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	19.5	20.0	20.5	V	
	VEP	14.5	15.0	15.5	V	
	TPW1	50		100	µs	Pulse 1
	TPW2	5		15	ms	Pulses 2-80
	TR1	0.2		0.7	µs	See Note 3
	TR2	0.6		1.4	µs	See Note 3
	TF					NA
	Reject		80		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.6	4.7	4.8	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	24.3	25.3	26.3	V	701-1655/TP4
	Low Load	24.3	25.3	26.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.3	2.4	2.5	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	18.0	19.0	20.0	V	701-1655/TP3

NOTES

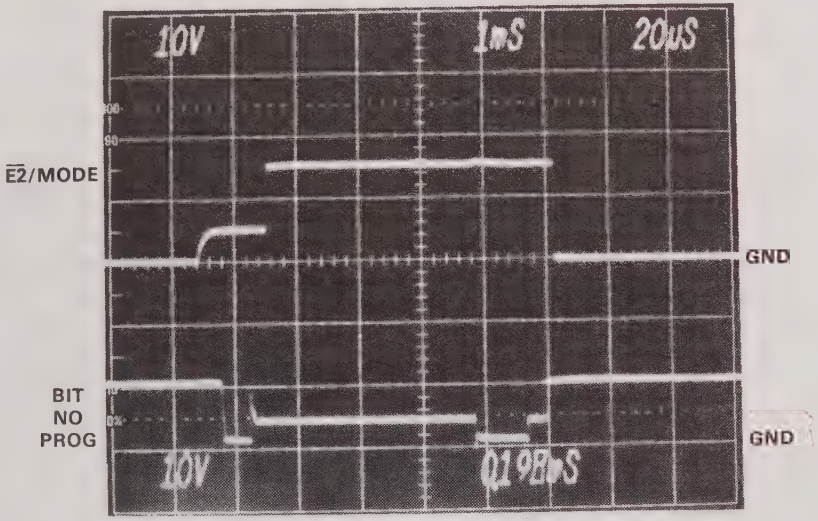
1. *Load RAM with hex FE for Family 15*
2. *Load RAM with hex 01 for Family 16.*
3. *Measured from 10% to 90%.*

REVISIONS

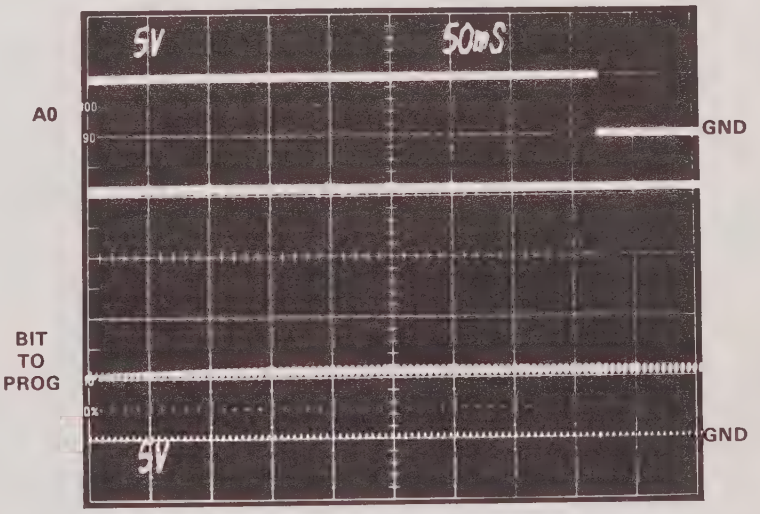
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.B.	11/82
		ECN #4772		XX	1/83
		ECN #4831		XX	5/83
		ECN #5023		CJB	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 15, 16		DRAWN BY: EE CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2


10V
1mS
20uS
$\overline{E2}$/MODE
GND
BIT
NO
PROG
GND
10V

5

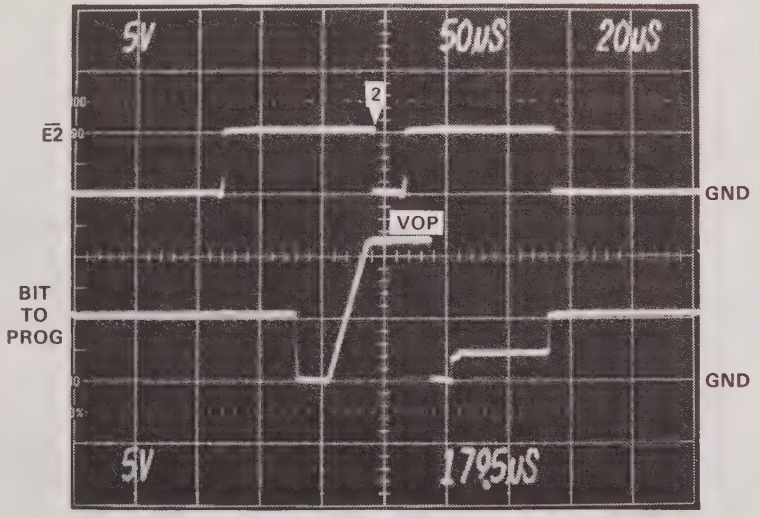

5V
50mS
A0
GND
BIT
TO
PROG
GND
5V

6

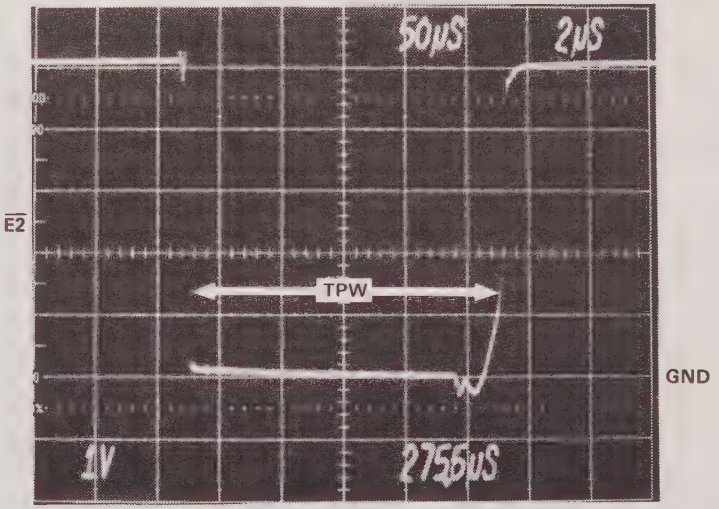
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ	11/82
		ECN #4831		JLH	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

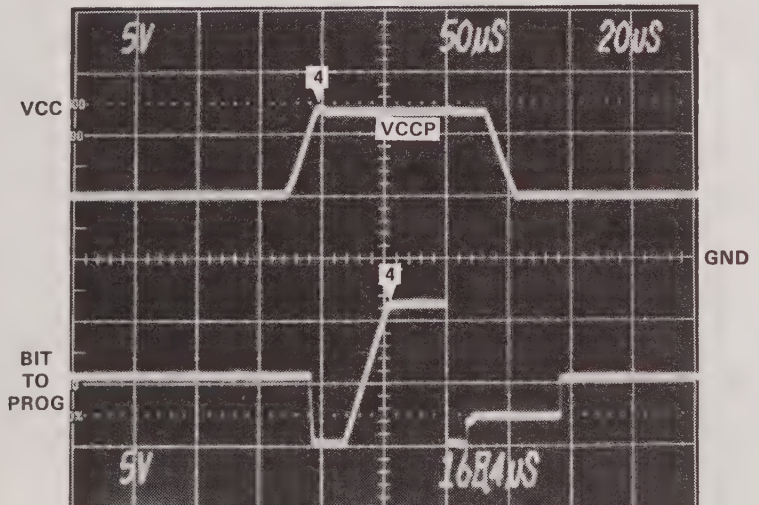
TITLE: TIMING DIAGRAM FAMILY CODES 15, 16		DRAWN BY: EE CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2

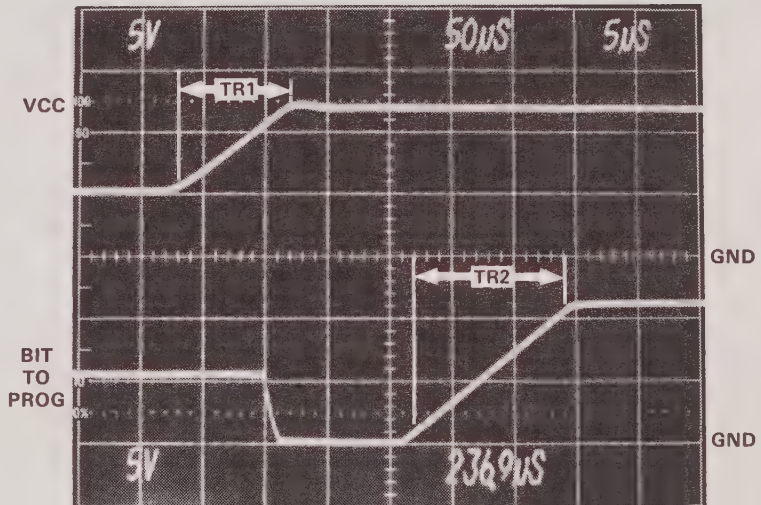

5V
50µS
20µS
2
E2
GND
VOP
BIT
TO
PROG
GND
5V
1795µS

1


50µS
2µS
E2
TPW
GND
1V
2756µS

2


5V
50µS
20µS
4
VCC
VCCP
GND
4
BIT
TO
PROG
5V
1684µS


5V
50µS
5µS
TR1
VCC
GND
TR2
BIT
TO
PROG
GND
5V
2369µS

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	11.5	11.7	12.0	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	10.5	11.0	11.5	V	
	TPW	9.0	10.0	11.0	µs	
	TR1	1.0		20.0	µs	See note 3
	TR2	1.0		15.0	µs	
	TF					NA
	Reject		10		Pulses	
	Overprogram		5		Pulses	
1ST PASS VERIFY	VCC	4.2	4.3	4.4	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	7.0	8.0	9.0	V	701-1655/TP4
	Low Load	7.0	8.0	9.0	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	2.9	3.0	3.1	V	701-1655/TP2
	High Load	7.8	8.8	9.8	V	701-1655/TP4
	Low Load	7.8	8.8	9.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 17.*
2. *Load RAM with hex 01 for Family 18.*
3. *Load V_{CC} with a 330 Ω ½-watt resistor.*

REVISIONS

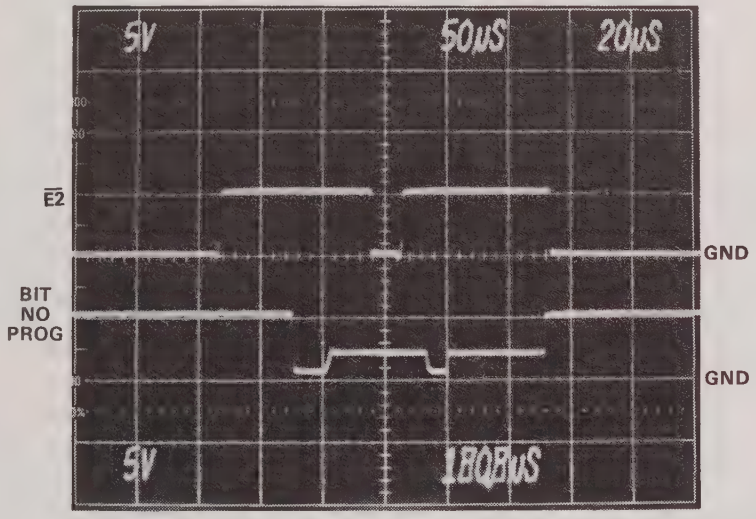
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		ZH	5/83
		ECN #5023		CTZ	3/84

DATA I/O ISSAQUAH, WA

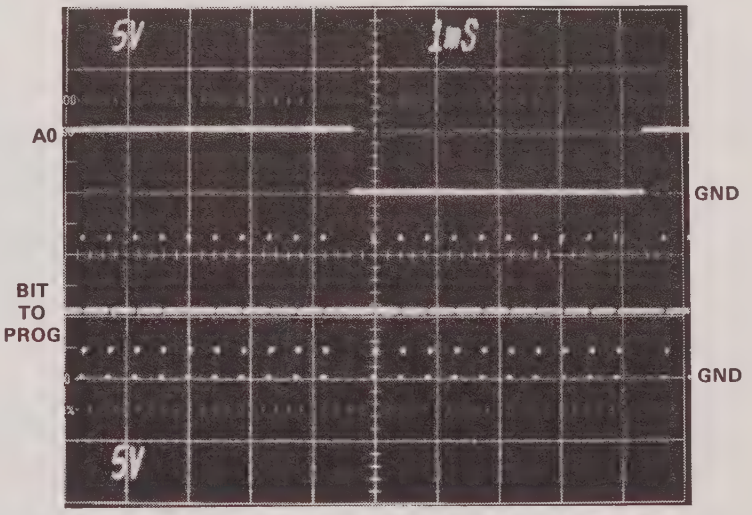
TITLE: TIMING DIAGRAM FAMILY CODES 17, 18	DRAWN BY: EE
	CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE | SHEET 1/2


5V
50uS
20uS
E2
GND
BIT
NO
PROG
GND
5V
180uS

5


5V
1mS
A0
GND
BIT
TO
PROG
GND
5V

6

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.S.J.	11/82
		ECN #4831		XXX	5/83

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 17, 18

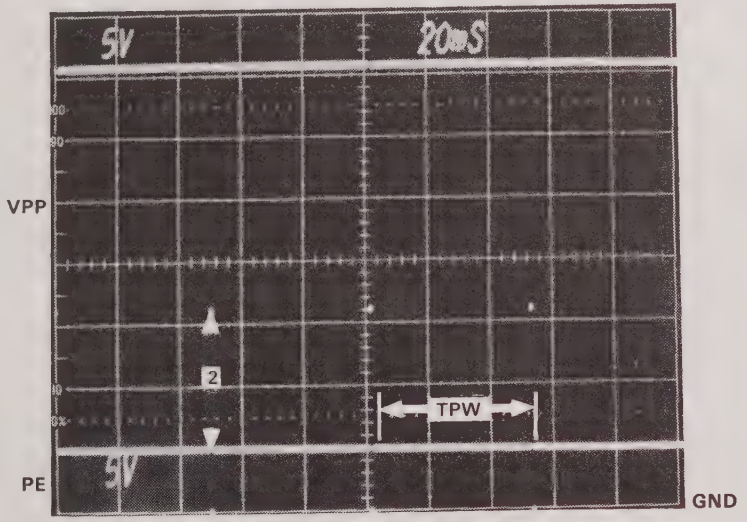
DRAWN BY: EE

CHECKED BY:

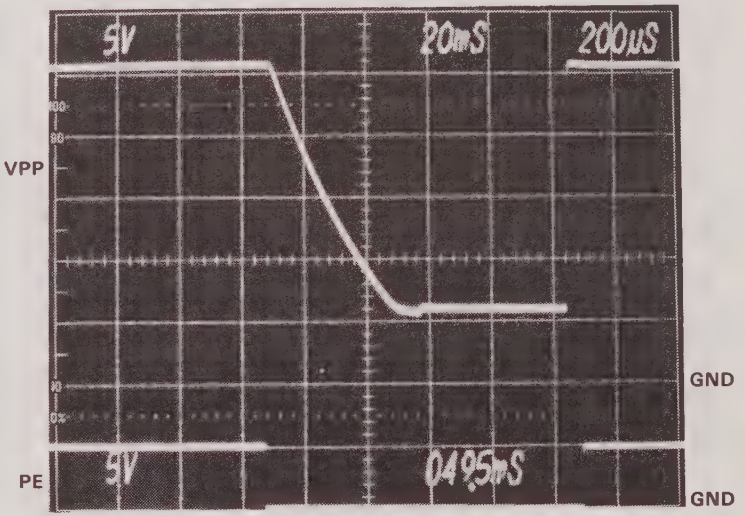
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

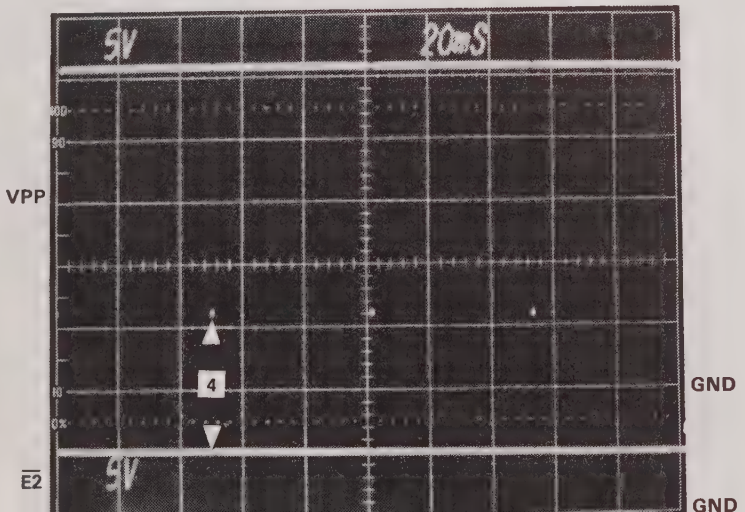
SHEET 2/2

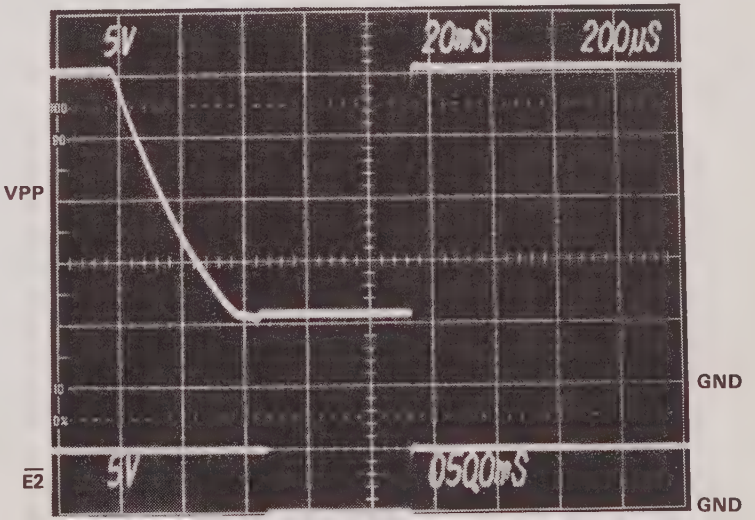

5V
20mS
VPP
2
TPW
PE
5V
GND

1


5V
20mS
200µS
VPP
GND
PE
5V
04,95mS
GND

2


5V
20mS
VPP
4
GND
E2
5V
GND


5V
20mS
200µS
VPP
GND
E2
5V
050,0mS
GND

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP	3.8	5.0	6.0	V	
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.00	5.25	V	
	VPPV	0.0	0.0	0.8	V	Pinout 24
	TPW	48	50	52	ms	
	T_R	50			ns	
	T_F	50			ns	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

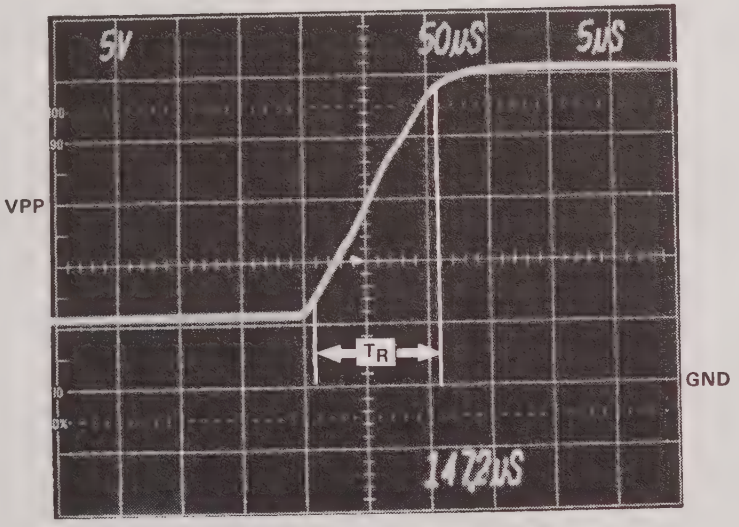
1. *Load RAM with hex FE for Family 19.*
2. *Load RAM with hex 01 for Family 20, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photos 11 and 12 are for Pinout 24.*
4. *Photos 13 and 14 are for Pinout 25.*
5. *Photo 15 is for Pinout 49, using the same setup as photo 12.*
6. *Photo 16 is for Pinout 50, using the same setup as photo 14.*

REVISIONS

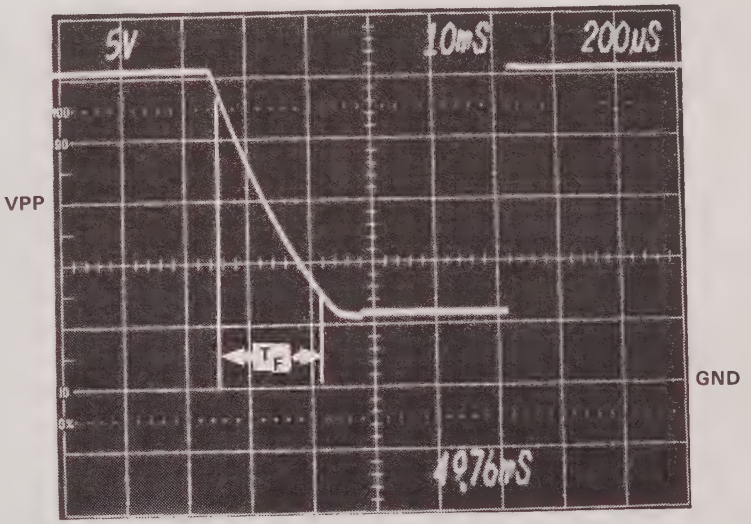
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.J.	11/82
		ECN #4831		XX	5/83
		ECN #5023		CTJ	3/84

DATA I/O ISSAQUAH, WA

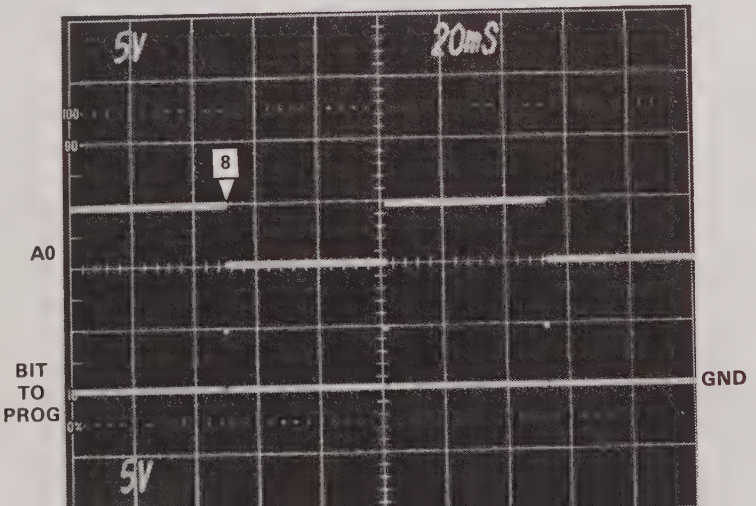
TITLE: TIMING DIAGRAM FAMILY CODES 19, 20	DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193
DRAWING NO.: 33-950-0059	
SCALE	SHEET 1/3

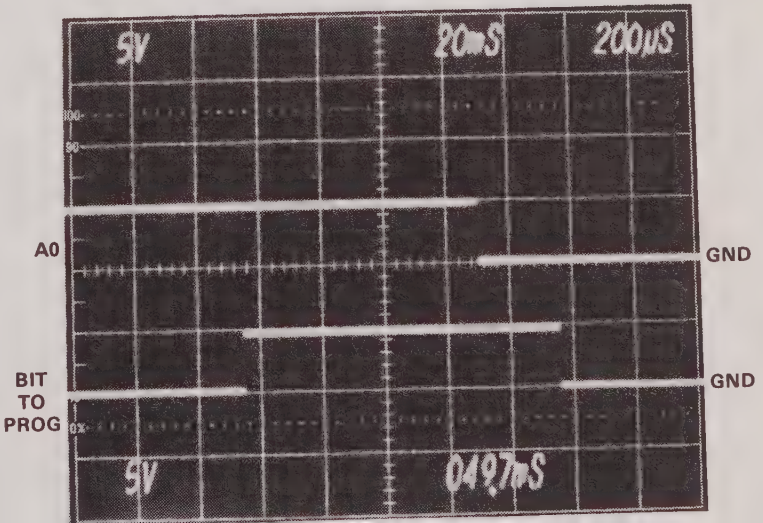

5V
50uS
5uS
VPP
T_R
GND
14.2uS

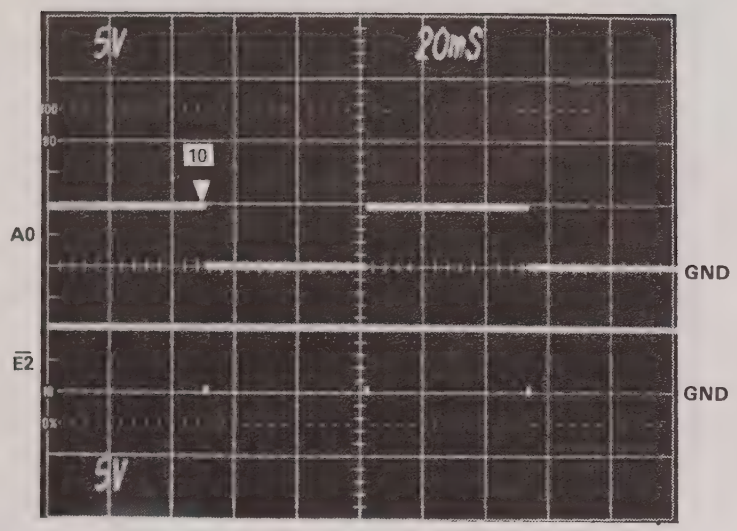
5


5V
10mS
200uS
VPP
T_F
GND
4.76mS

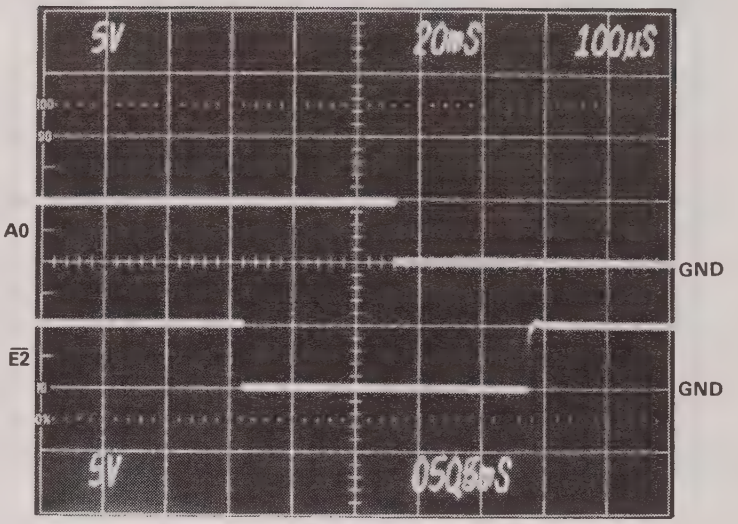
6


5V
20mS
8
A0
BIT
TO
PROG
GND
5V


5V
20mS
200uS
A0
GND
BIT
TO
PROG
GND
5V
04.7mS



9

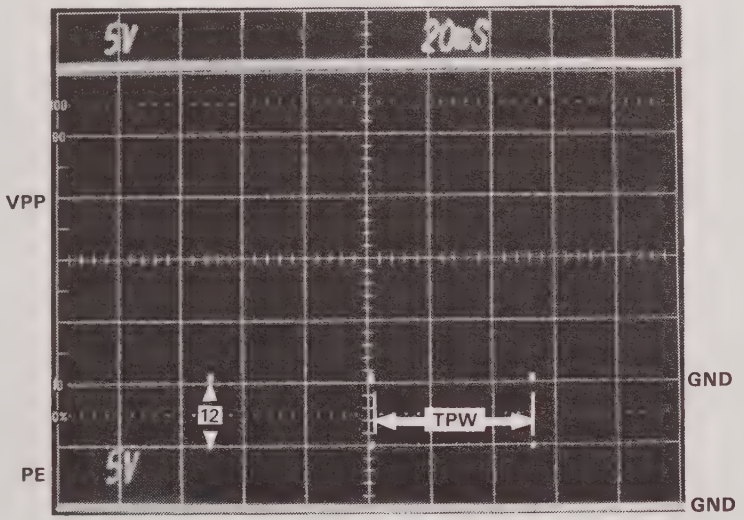


10

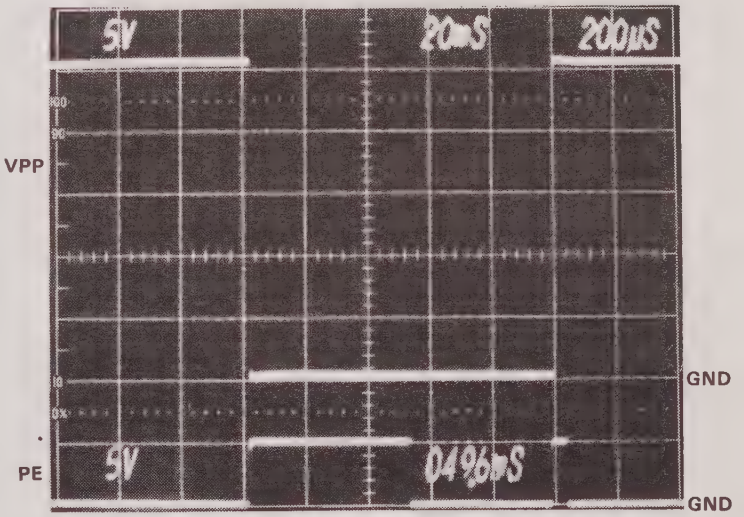
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ.	11/82
		ECN #4831		TH	5/83

DATA I/O ISSAQUAH, WA

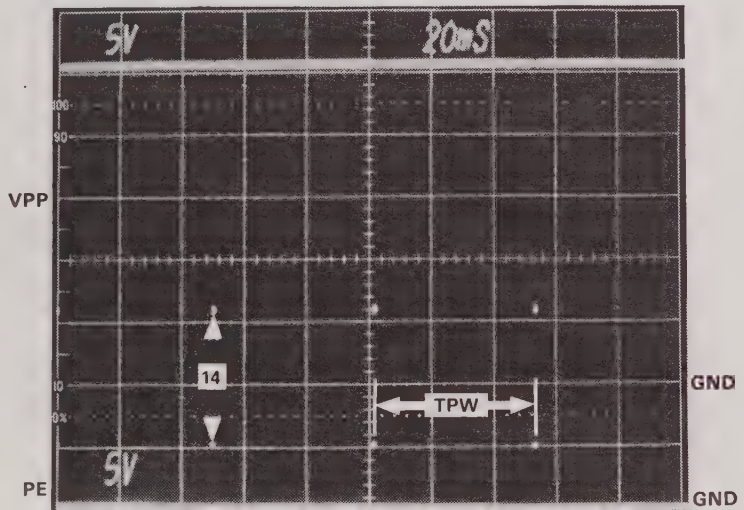
TITLE: TIMING DIAGRAM FAMILY CODES 19, 20		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/3

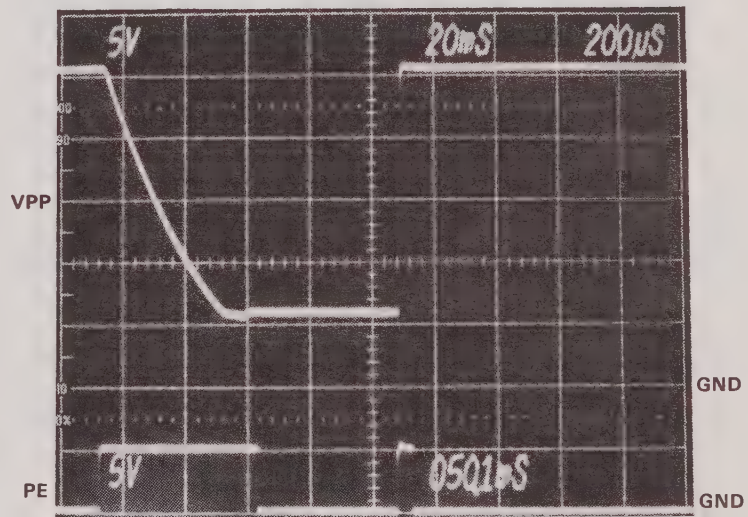

5V
20mS
VPP
12
TPW
GND
PE
5V
GND

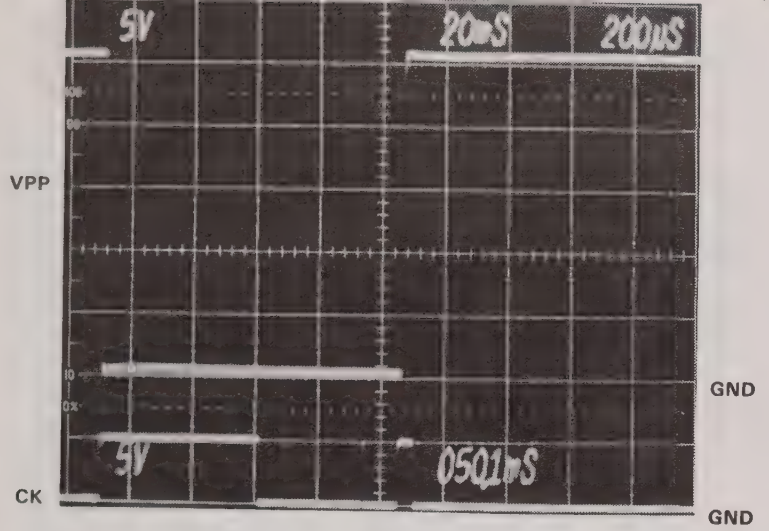
11


5V
20mS
200µS
VPP
GND
PE
5V
GND

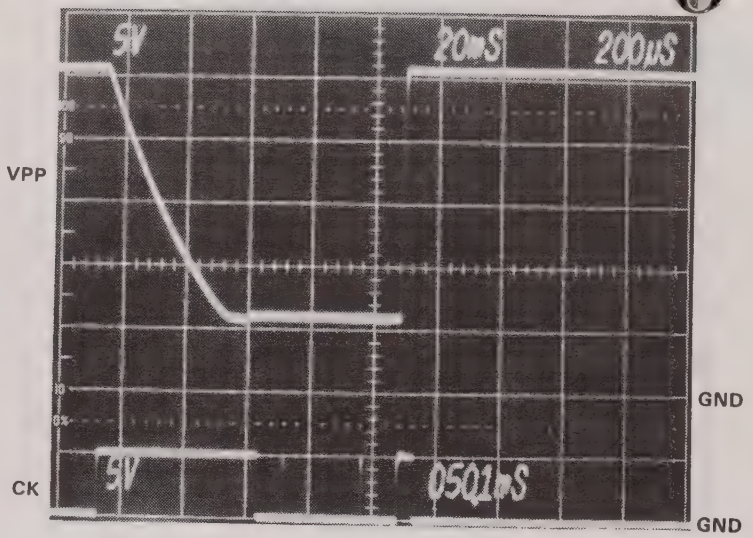
12


5V
20mS
VPP
14
TPW
GND
PE
5V
GND


5V
20mS
200µS
VPP
GND
PE
5V
GND



15



16

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		[illegible]	5/83

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 19, 20

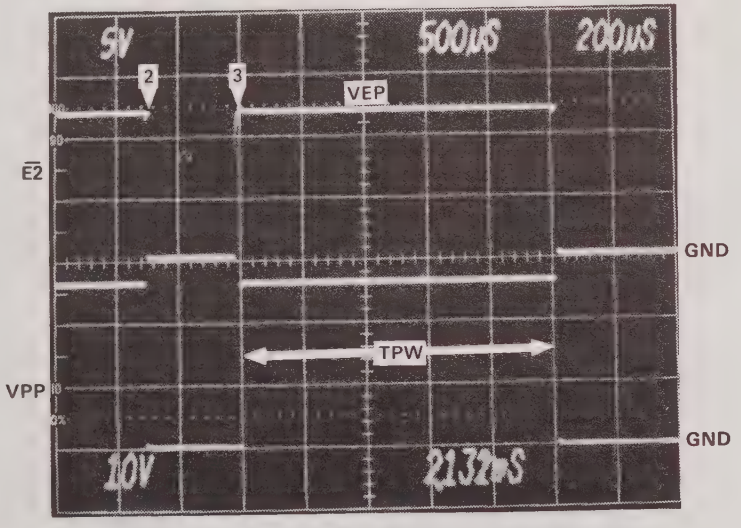
DRAWN BY:

CHECKED BY:

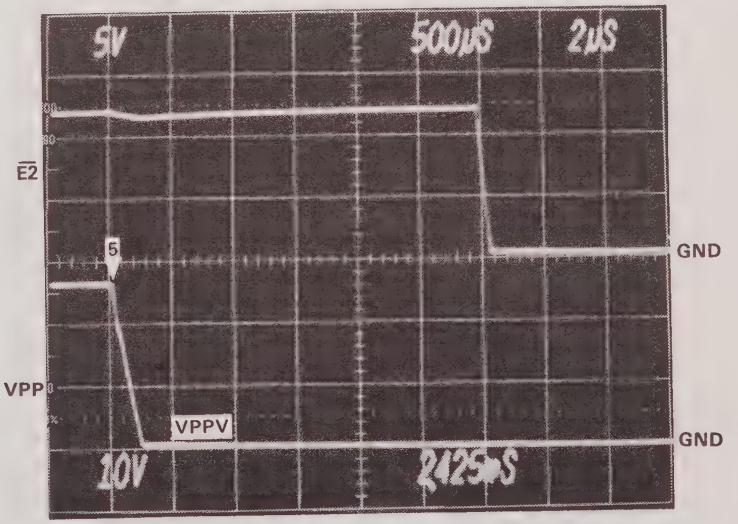
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

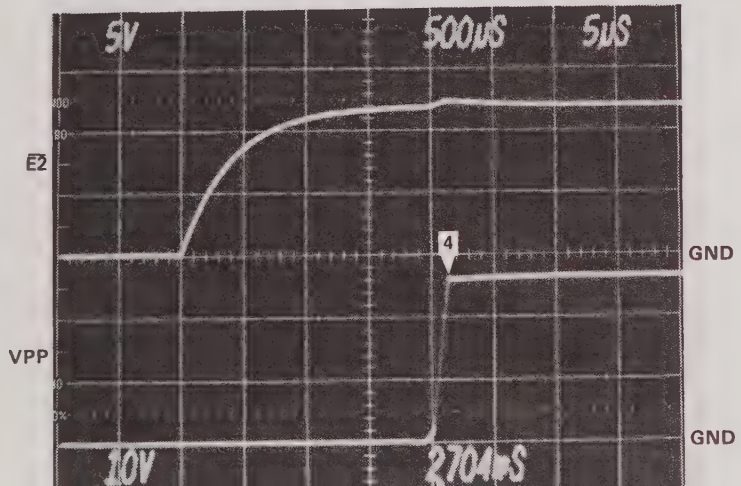
SHEET 3/3

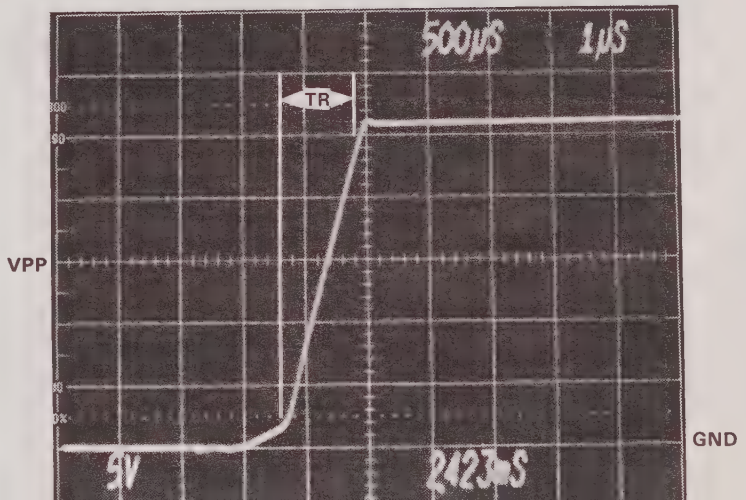

5V
500µS
200µS
2
3
VEP
E2
GND
TPW
VPP
GND
10V
2132mS

1


5V
500µS
2µS
E2
GND
5
VPP
VPPV
GND
10V
2425mS

2


5V
500µS
5µS
E2
4
GND
VPP
GND
10V
2704mS


500µS
1µS
TR
VPP
GND
5V
2423mS

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP	3.8	5.0	6.0	V	
	VPP	25.0	26.0	27.0	V	
	VPPV	0.0	0.0	1.0	V	
	VEP	11.4	12.0	12.6	V	
	VBB	-5.25	-5.00	-4.75	V	Not Shown
	VDD	11.4	12.0	12.6	V	Not Shown
	TPW	0.8	1.0	1.2	ms	
	TR	0.5	1.0	2.0	µs	
	TF	0.5	1.0	2.0	µs	
	Reject		100		Loops	See Note 3
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	16.3	17.3	18.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

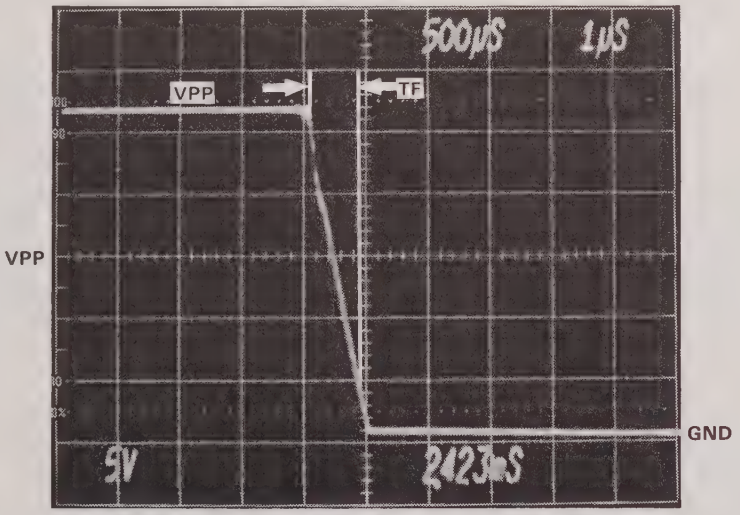
1. *Load RAM with hex FE for Family 21.*
2. *Load RAM with hex 01 for Family 22, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *A loop is defined as a complete pass from Address 0 to maximum device address, applying one pulse at each address.*

REVISIONS

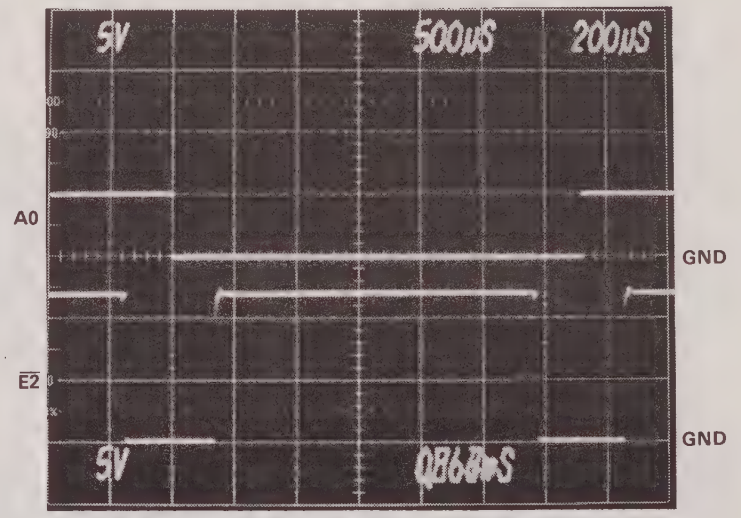
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		[illegible]	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

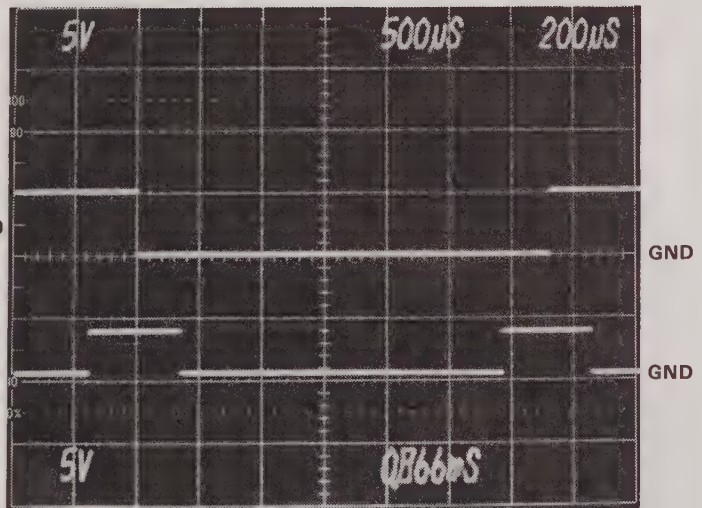
TITLE: TIMING DIAGRAM FAMILY CODES 21, 22	DRAWN BY: EE	
	CHECKED BY:	
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2

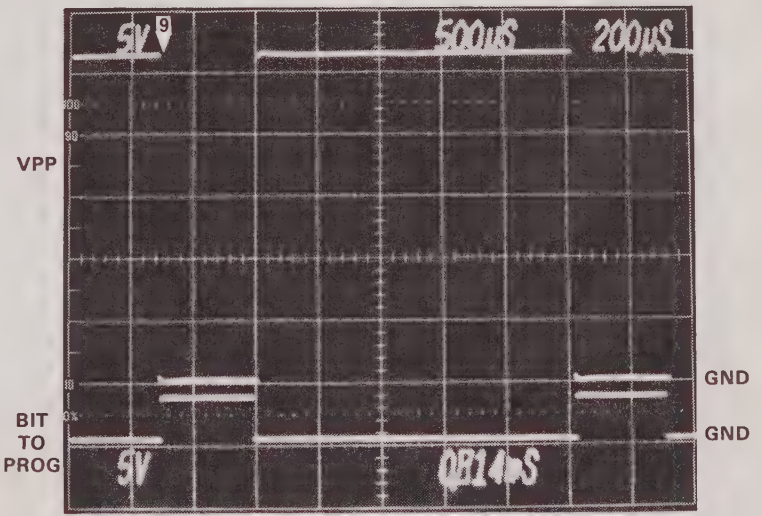

500µS
1µS
VPP
TF
VPP
GND
5V

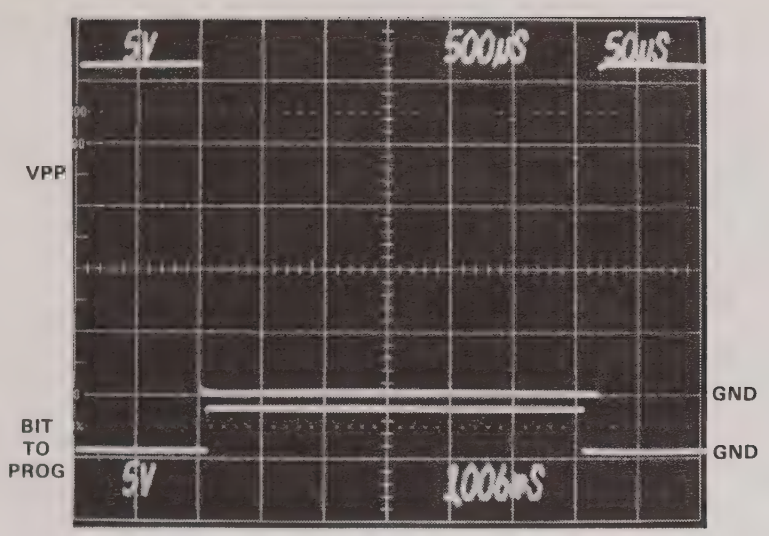
5


5V
500µS
200µS
A0
GND
E2
GND
5V

6


5V
500µS
200µS
A0
GND
BIT
TO
PROG
GND
5V


5V
500µS
200µS
VPP
GND
BIT
TO
PROG
GND
5V



9

B-39
981-0001

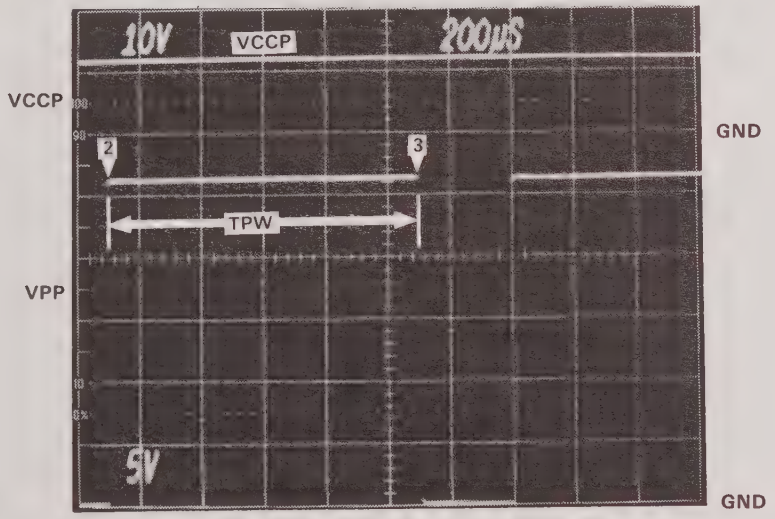
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.J.	11/82
		ECN #4831		XA	5/83

DATA I/O ISSAQUAH, WA

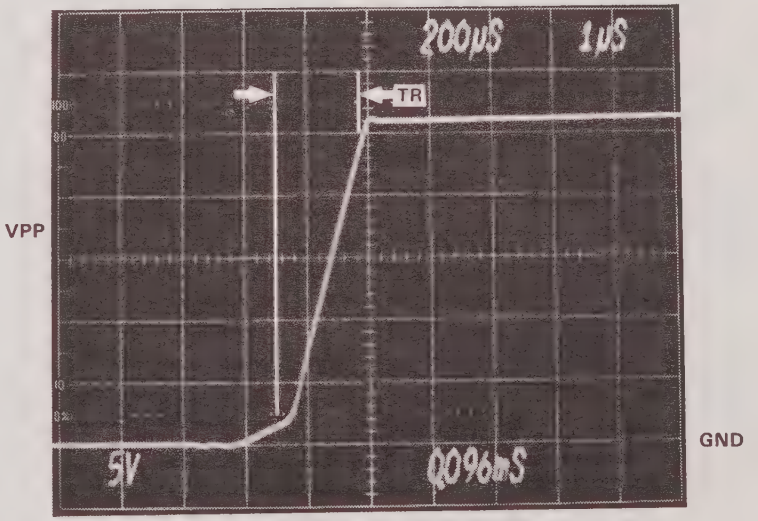
TITLE: TIMING DIAGRAM FAMILY CODES 21, 22	DRAWN BY: ES CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

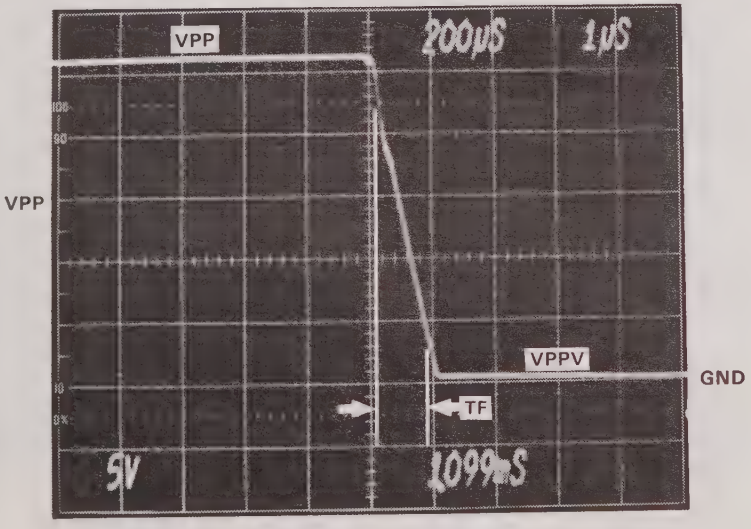
SCALE | SHEET 2/2


10V
VCCP
200µS
VCCP
GND
2
3
TPW
VPP
5V
GND

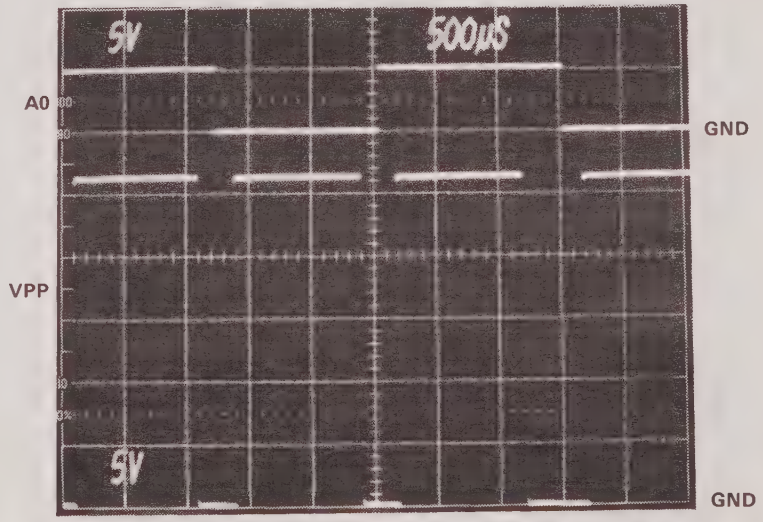
1


200µS
1µS
TR
VPP
GND
5V
0096mS

2


VPP
200µS
1µS
VPP
VPPV
GND
TF
5V
1099mS

3


5V
500µS
A0
GND
VPP
5V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	11.4	12.0	12.6	V	
	VOP					NA
	VPP	25.0	26.0	27.0	V	
	VPPV	0.0		1.0	V	
	VBB	-5.25	-5.0	-4.75	V	Not Shown
	VDD	11.4	12.0	12.4	V	Not Shown
	TPW	0.8	1.0	1.2	ms	
	TR	0.5		2.0	µs	
	TF	0.5		2.0	µs	
	Reject		100		Loops	See Note 3
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	16.3	17.3	18.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 23.*
2. *Load RAM with hex 01 for Family 24, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *A loop is defined as a complete pass from Address 0 to maximum device address applying one pulse at each address. All 100 loops are performed, and the device is read and verified after all 100 loops.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.T.Z.	11/82
		ECN #4831		XA	5/83
		ECN #5023		CTZ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

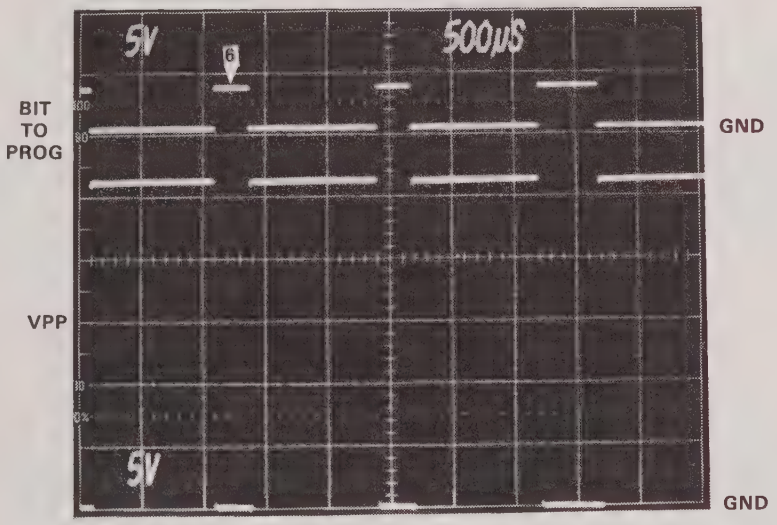
FAMILY CODES 23, 24

DRAWN BY:

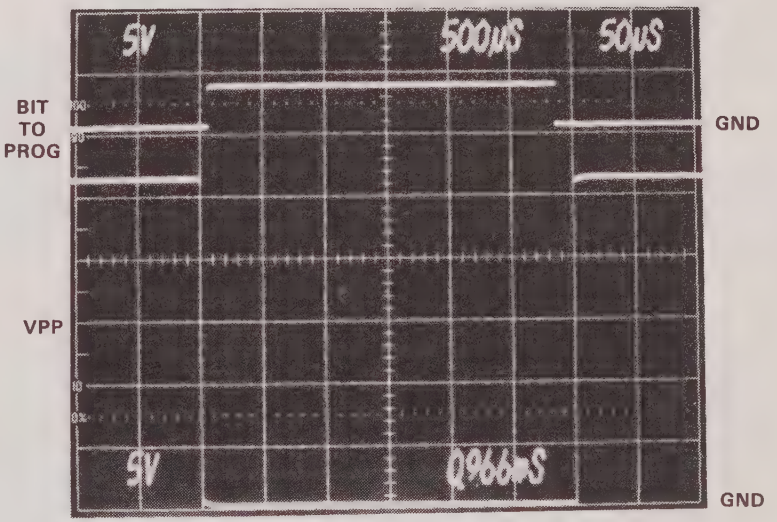
CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE | SHEET 1/2


5V
6
500µS
BIT
TO
PROG
GND
VPP
5V
GND

5

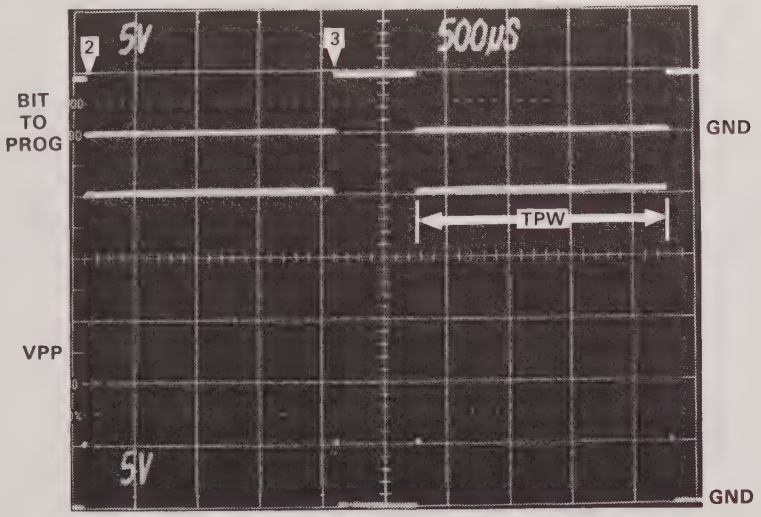

5V
500µS
50µS
BIT
TO
PROG
GND
VPP
5V
GND

6

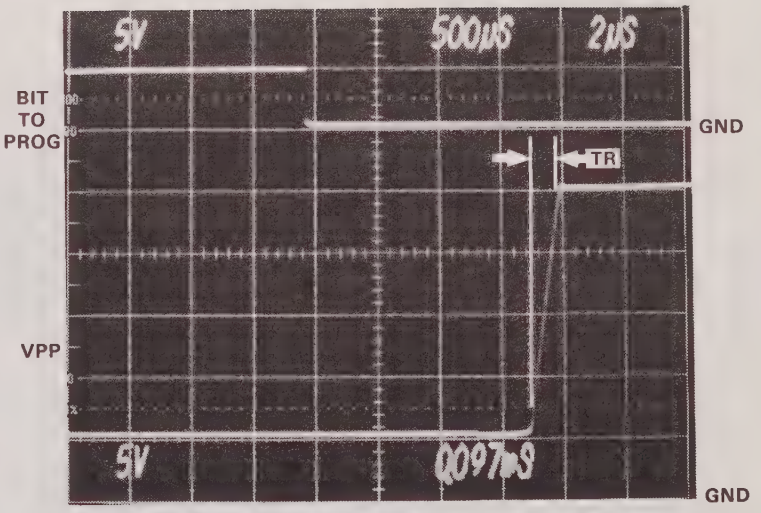
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.J.	11/82
		ECN #4831		JCH	5/83

DATA I/O ISSAQUAH, WA

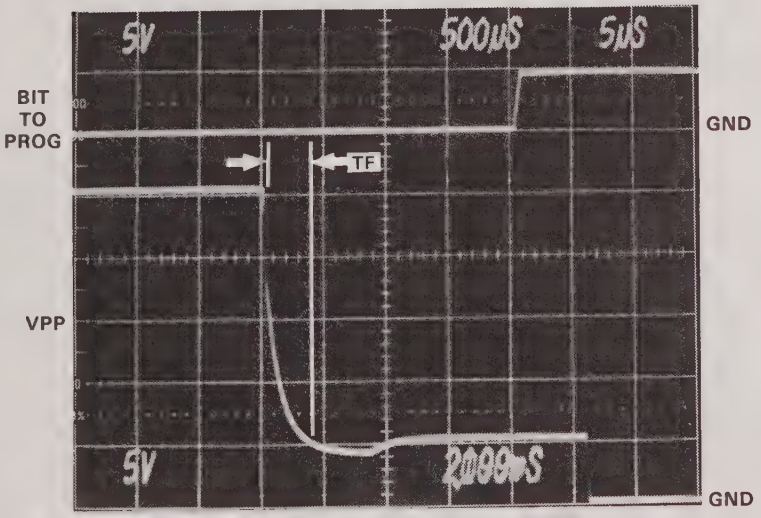
TITLE: TIMING DIAGRAM FAMILY CODES 23, 24		DRAWN BY: kac CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE:		SHEET 2/2

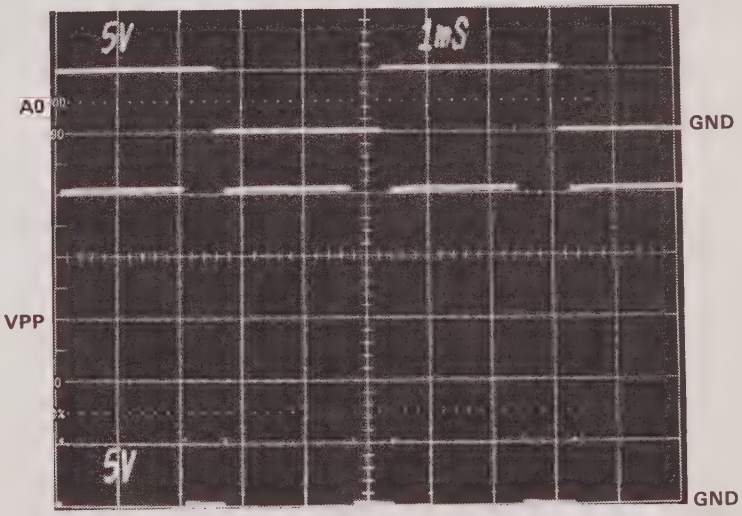

2
5V
3
500µS
BIT
TO
PROG
GND
TPW
VPP
5V
GND

1


5V
500µS
2µS
BIT
TO
PROG
GND
TR
VPP
5V
.0097mS
GND

2


5V
500µS
5µS
BIT
TO
PROG
GND
TF
VPP
5V
.2099mS
GND


5V
1mS
A0
GND
VPP
5V
GND

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	1.9	2.0	2.1	ms	
	TR	0.5		2.0	µs	
	TF	0.5		5.0	µs	
	Reject		20		Loops	See Note 3
	Overprogram		5		Loops	See Note 3
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 25.*
2. *Load RAM with hex 01 for Family 26, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *A loop is defined as one complete pass from Address 0 to maximum device address applying one pulse at each address. A read and verify is done after each loop, and when the device verifies, five more loops are applied.*

REVISIONS

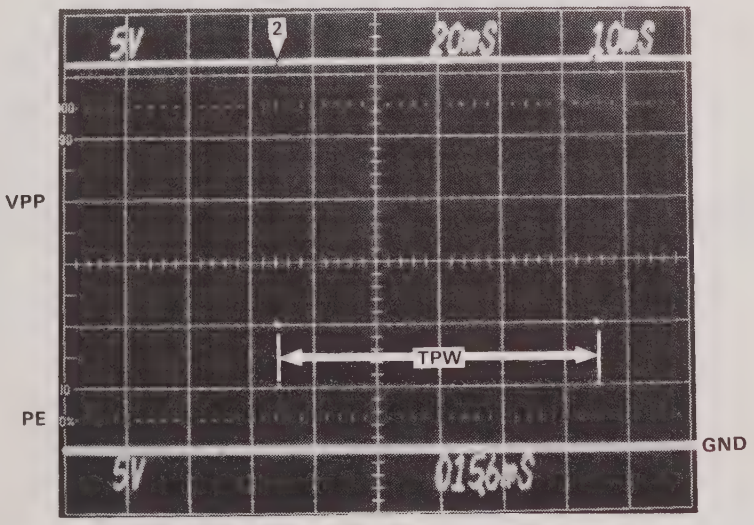
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		KA	5/83
		ECN #5023		CTZ	3/84

DATA I/O ISSAQUAH, WA

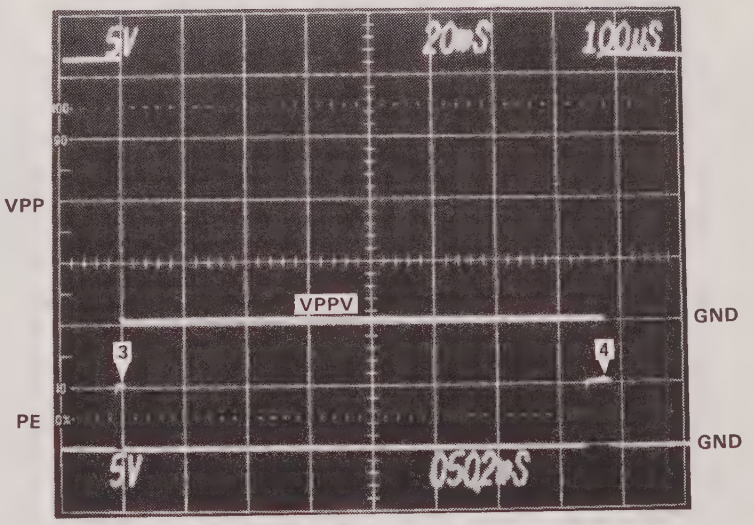
TITLE: TIMING DIAGRAM FAMILY CODES 25, 26	DRAWN BY: EE CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

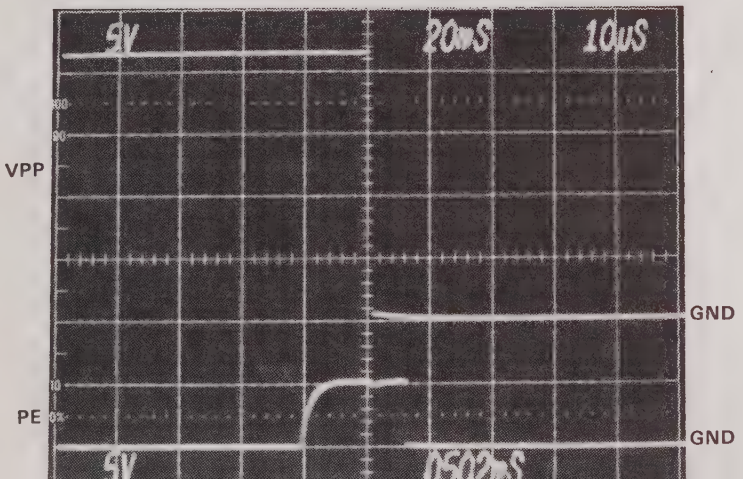
SCALE | SHEET 1/1

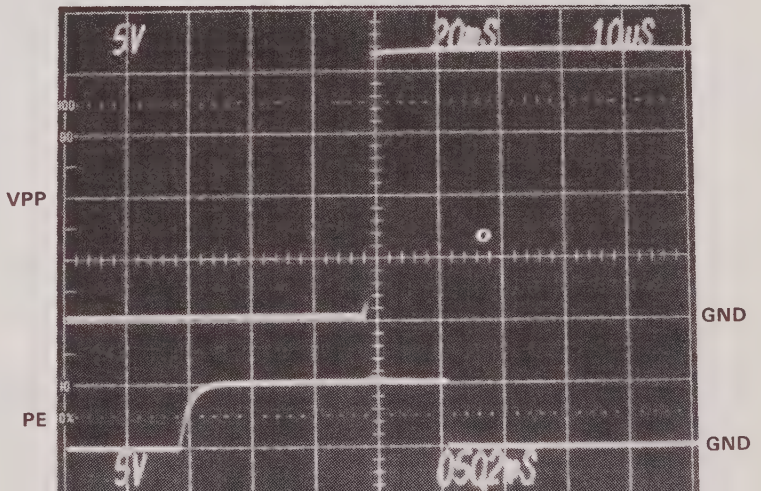

5V
2
20mS
10mS
VPP
TPW
PE
GND
5V
0156mS

1


5V
20mS
100uS
VPP
VPPV
GND
3
4
PE
GND
5V
0502mS

2


5V
20mS
10uS
VPP
GND
PE
GND
5V
0502mS


5V
20mS
10uS
VPP
GND
PE
GND
5V
0502mS

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP	3.8	5.00	6.00	V	
	VPP	20.5	21.0	21.5	V	
	VPPV	0.0	0.0	0.8	V	
	TPW	48	50	52	ms	
	TR	50			ns	
	TF					NA
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

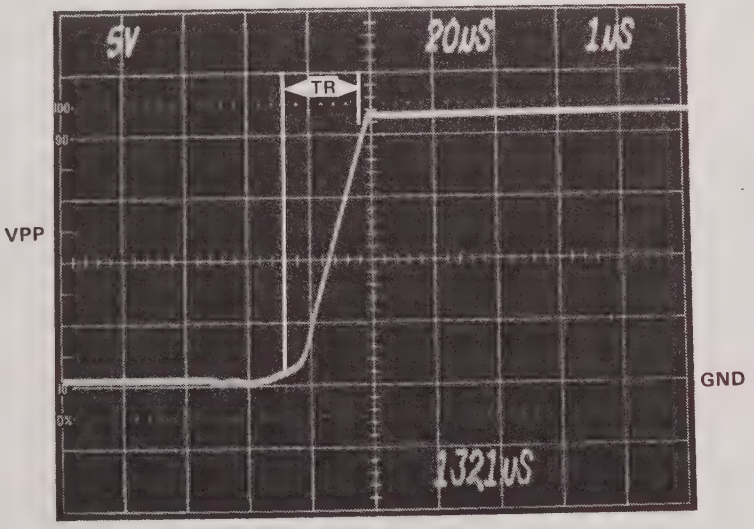
1. *Load RAM with hex FE for Family 27.*
2. *Load RAM with hex 01 for Family 28, and bit-to-prog waveform becomes bit-no-prog waveform.*

REVISIONS

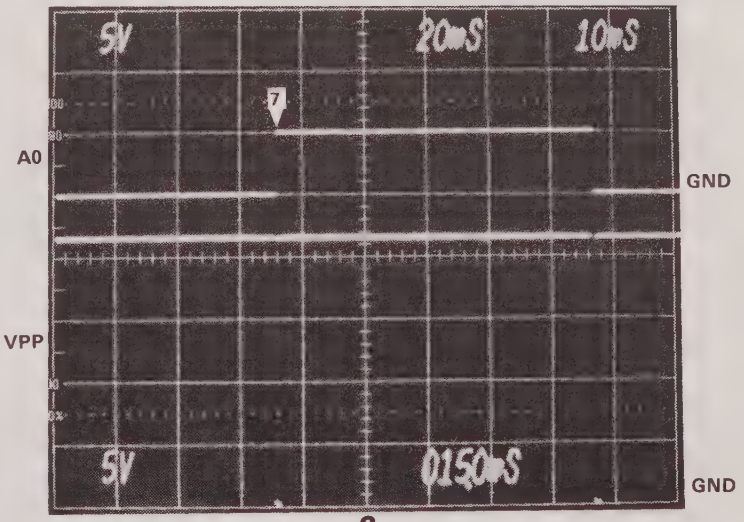
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJJ	11/82
		ECN #4831		XH	5/83
		ECN #5023		CJJ	3/84

DATA I/O ISSAQUAH, WA

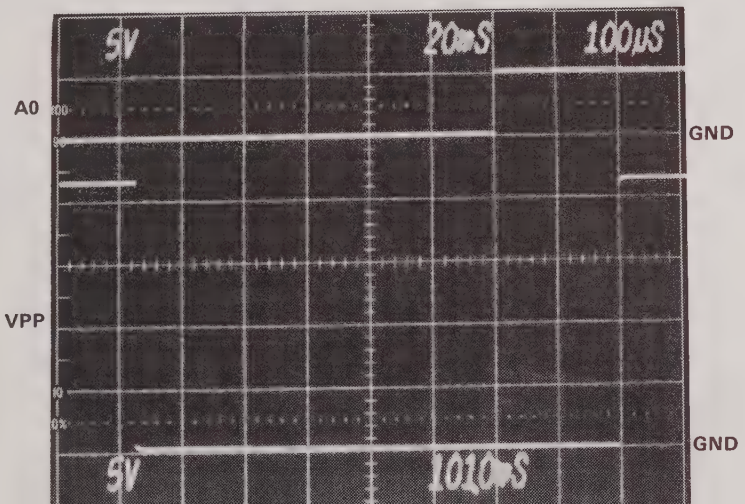
TITLE: TIMING DIAGRAM FAMILY CODES 27, 28	DRAWN BY: ES CHECKED BY:	
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2

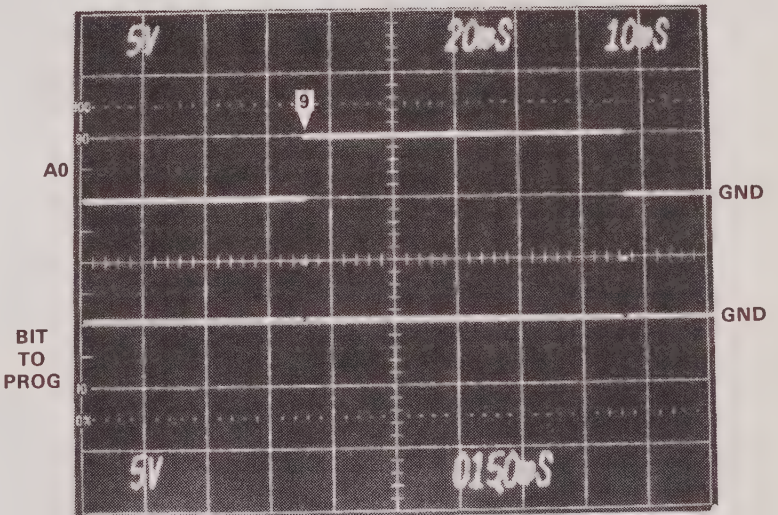

5V
20µS
1µS
TR
VPP
GND
1321µS

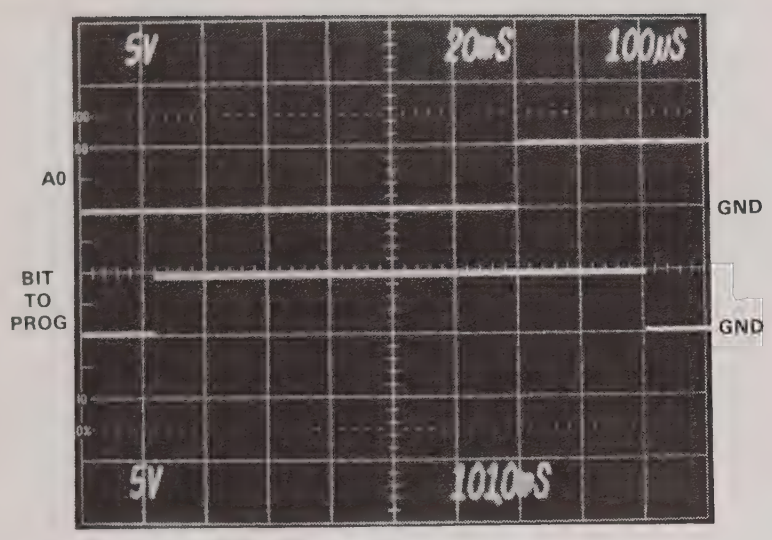
5


5V
20mS
10mS
7
A0
GND
VPP
5V
0150mS
GND

6


5V
20mS
100µS
A0
GND
VPP
GND
5V
1010mS


5V
20mS
10µS
9
A0
GND
GND
BIT
TO
PROG
5V
0150µS



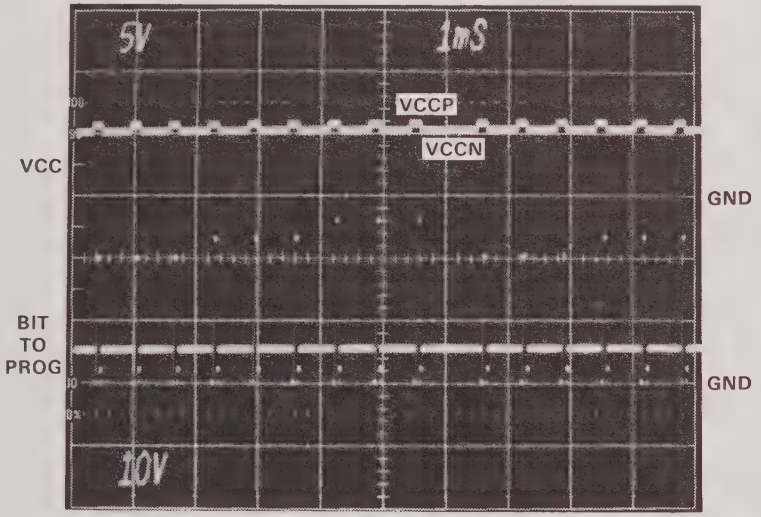
9

B-49
981-0001

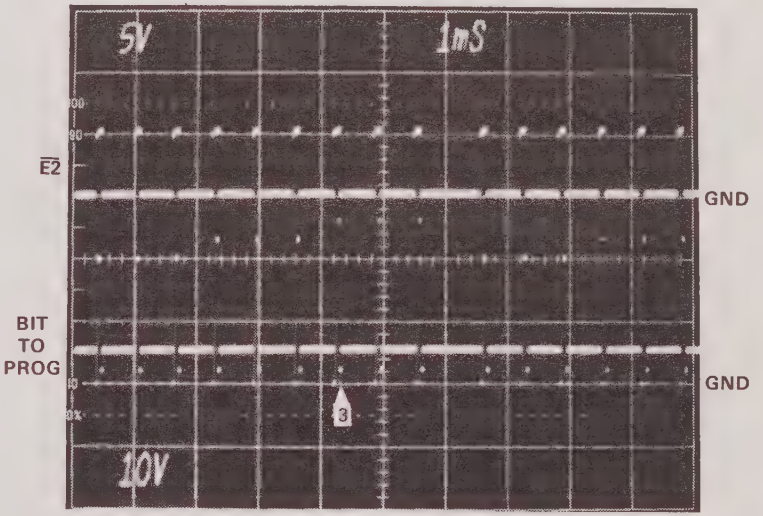
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		XA	5/83

DATA I/O ISSAQUAH, WA

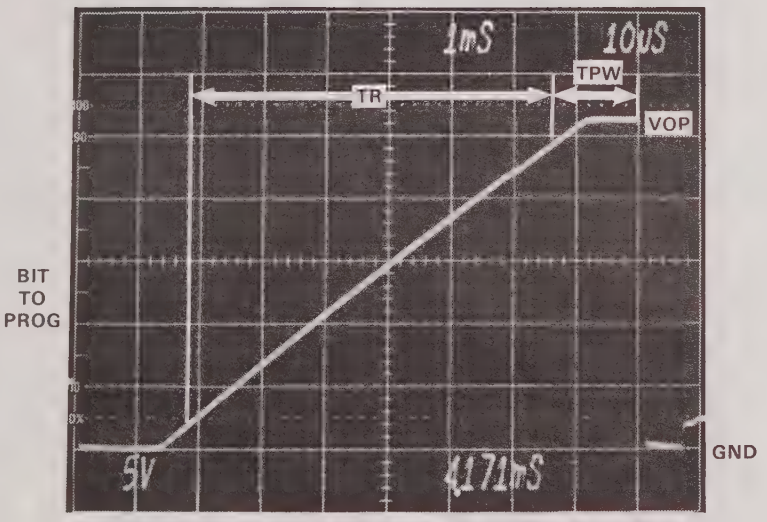
TITLE: TIMING DIAGRAM FAMILY CODES 27, 28	DRAWN BY: ES CHECKED BY:	
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2

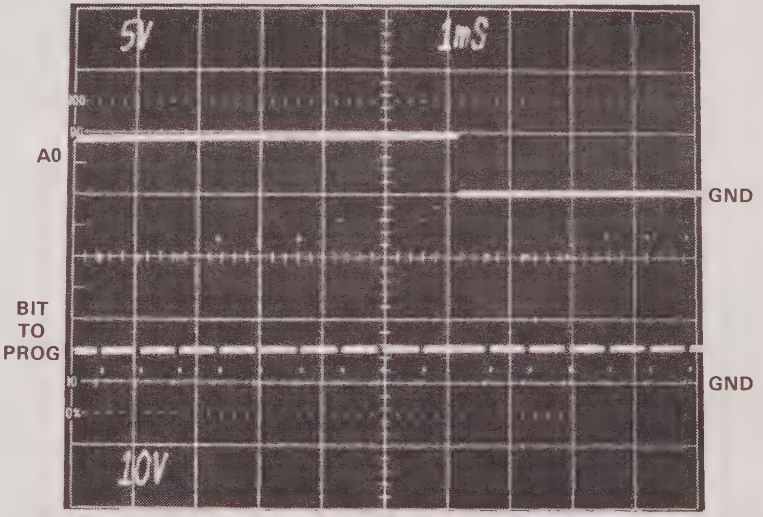

5V
1mS
VCCP
VCCN
VCC
GND
BIT
TO
PROG
GND
10V

1


5V
1mS
E2
GND
BIT
TO
PROG
GND
3
10V

2


1mS
10uS
TR
TPW
VOP
BIT
TO
PROG
GND
5V
4.171mS


5V
1mS
A0
GND
BIT
TO
PROG
GND
10V

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.4	5.5	5.6	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	19	20	21	V	Pulses 1-3
		22	23	24	V	Pulses 4-6
		25	26	27	V	Pulses 7-9
	TPW	10		40	µs	See note 3
	TR	42	52	69	µs	See note 4
	Reject		9		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.1	4.2	4.3	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	17.9	18.9	19.9	V	701-1655/TP4
	Low Load	17.9	18.9	19.9	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	2.9	3.0	3.1	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	4.6	5.6	6.6	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 29.*
2. *Load RAM with hex 01 for Family 30.*
3. *This is measured at the 90% level of the pulse, and all three pulses must meet this specification.*
4. *This is measured from 10% to 90% on the 26V pulses.*

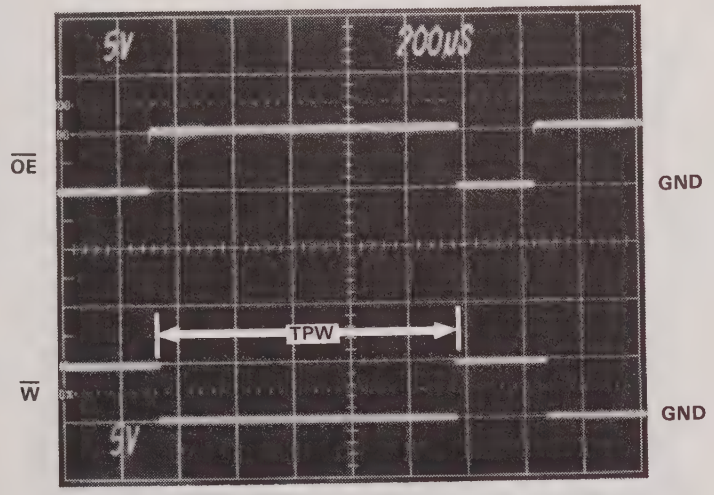
B-51
9811-0001

REVISIONS

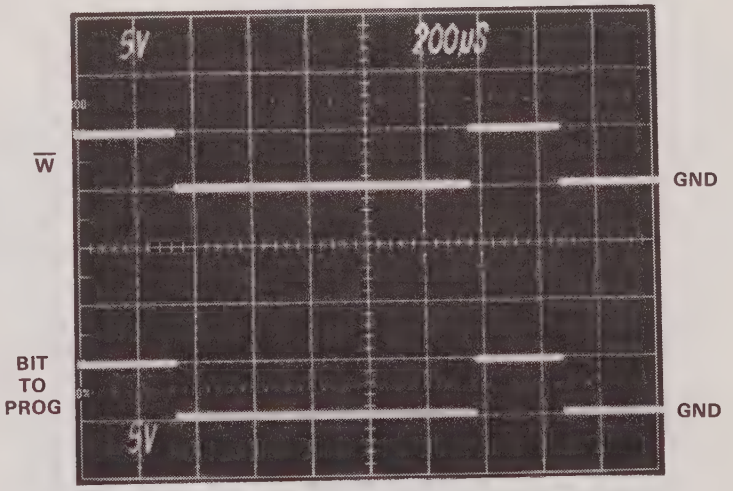
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ	11/82
		ECN #4831		XR	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

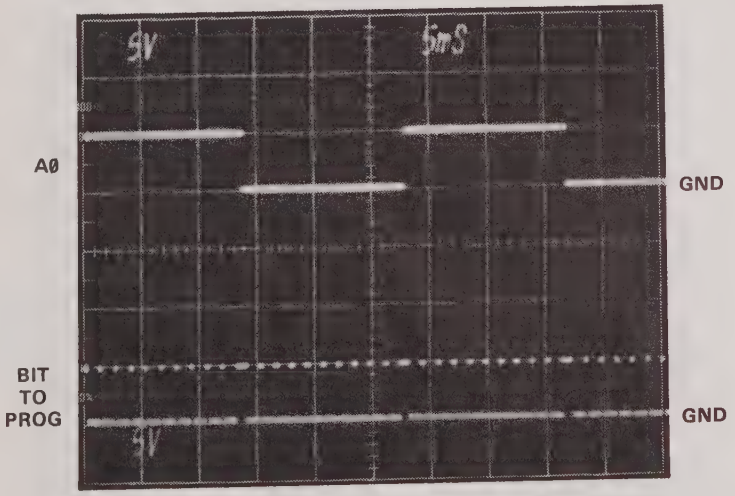
TITLE: TIMING DIAGRAM FAMILY CODES 29, 30		DRAWN BY: DG CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE:		SHEET 1/1


5V
200uS
OE
GND
TPW
W
GND
5V

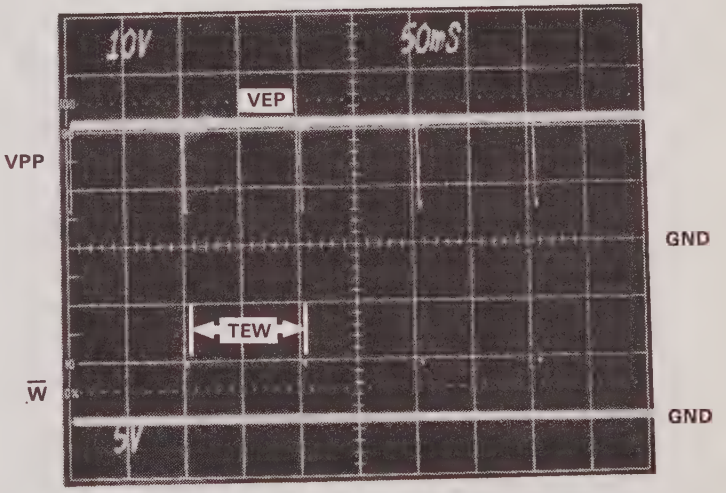
1


5V
200uS
W
GND
BIT
TO
PROG
GND
5V

2


5V
5mS
A0
GND
BIT
TO
PROG
GND
5V

3


10V
50mS
VEP
VPP
GND
TEW
W
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VEP	19.5	20.0	20.5	V	
	VEE	19.5	20.0	20.5	V	
	TPW	1.0		10.0	ms	
	TEW	99	100	101	ms	
	Reject		10		Pulses	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.3	5.3	6.3	V	701-1655/TP4
	LOW LOAD	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 2D.*
2. *Load RAM with hex 01 for Family 2E*
3. *Photos 4 and 5 show erase pulse.*

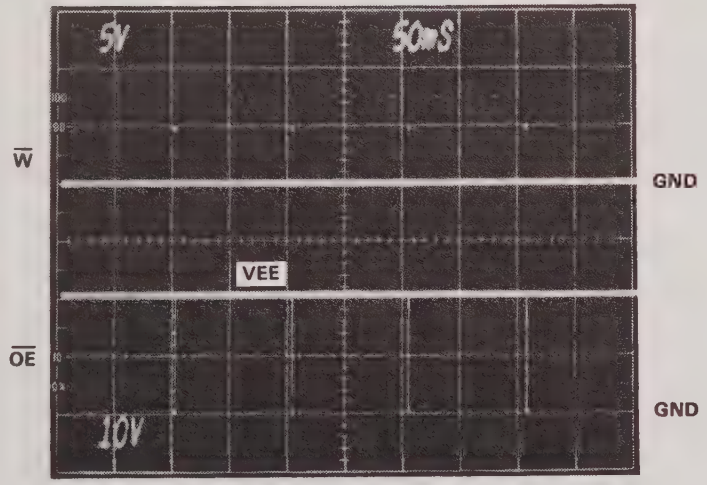
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

TIMING DIAGRAM

FAMILY CODES 2D, 2E

DATA I/O



5

B-55
981-0001

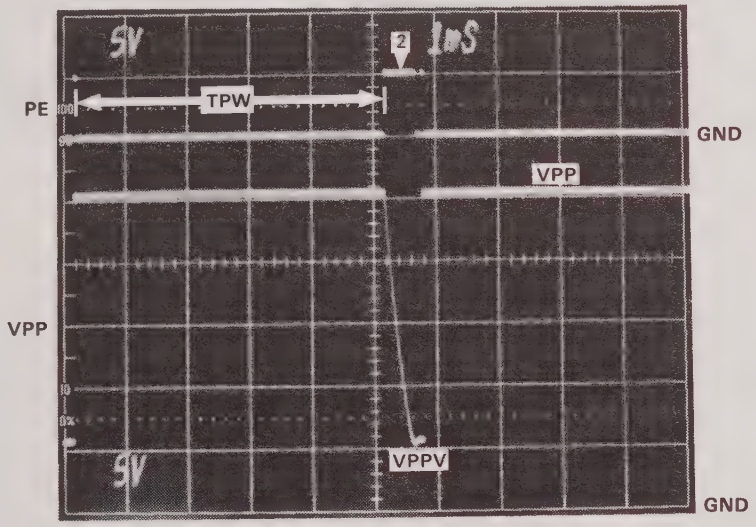
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

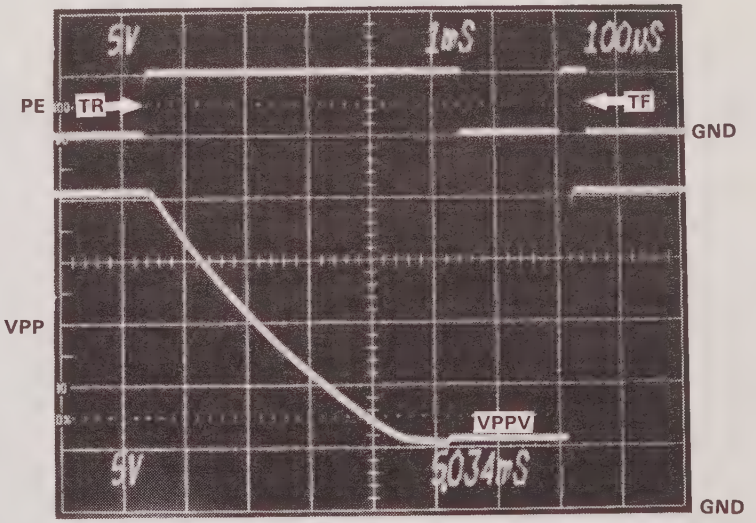
TIMING DIAGRAM

FAMILY CODES 2D, 2E

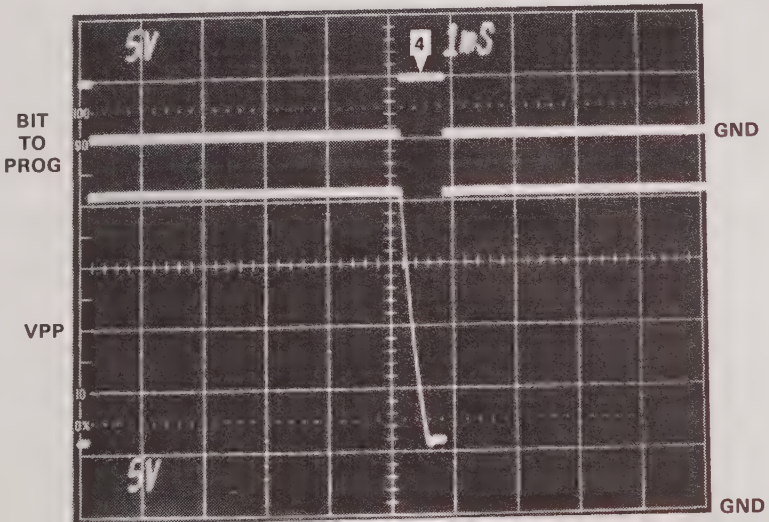
DATA I/O

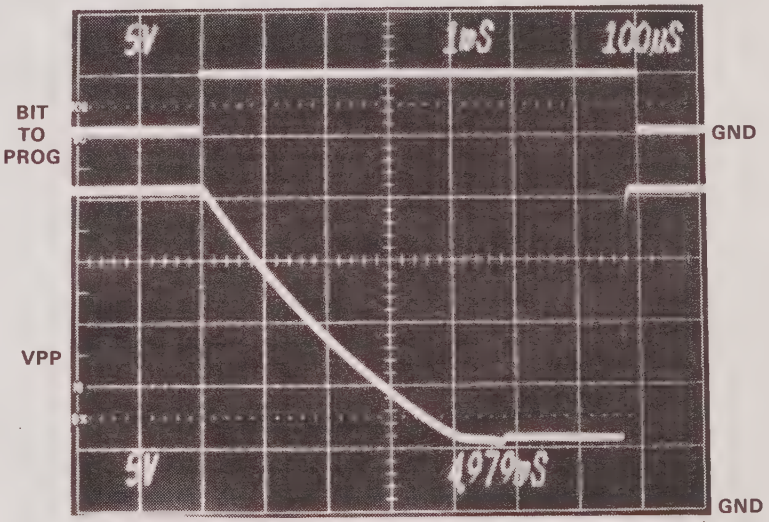

5V
2
1mS
PE
TPW
GND
VPP
VPP
VPPV
5V
GND

1


5V
1mS
100uS
PE
TR
TF
GND
VPP
VPPV
5V
5034mS
GND

2


5V
4
1mS
BIT
TO
PROG
GND
VPP
5V
GND


5V
1mS
100uS
BIT
TO
PROG
GND
VPP
5V
4979mS
GND

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	4.9	5.0	5.1	ms	
	TR	5			ns	
	TF	5			ns	
	Reject		5		Pulses	
	Overprogram		x		Pulses	See Note 3
1ST PASS	VCC	4.7	4.8	4.9	V	
VERIFY	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS	VCC	5.1	5.2	5.3	V	
VERIFY	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 31.*
2. *Load RAM with hex 01 for Family 32, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The number of overprogram pulses is equal to the greatest number of reject pulses applied to any address.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CSJ	11/82
		ECN #4831		JK	5/83
		ECN #5023		CTJ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 31, 32

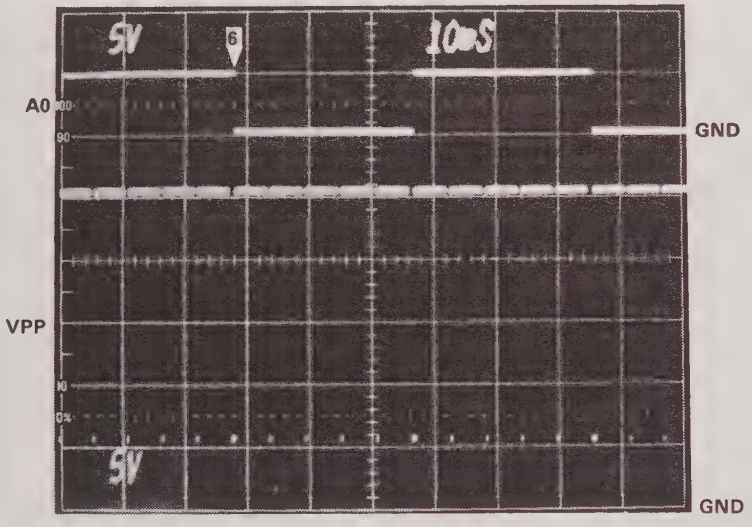
DRAWN BY:

CHECKED BY:

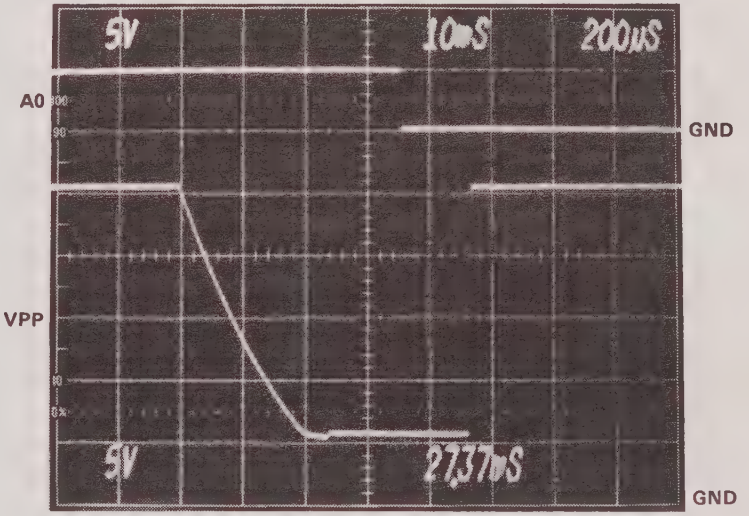
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 1/2


5V
6
10mS
A0
GND
VPP
5V
GND

5


5V
10mS
200uS
A0
GND
VPP
5V
27.37mS
GND

6

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		I.H	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 31, 32

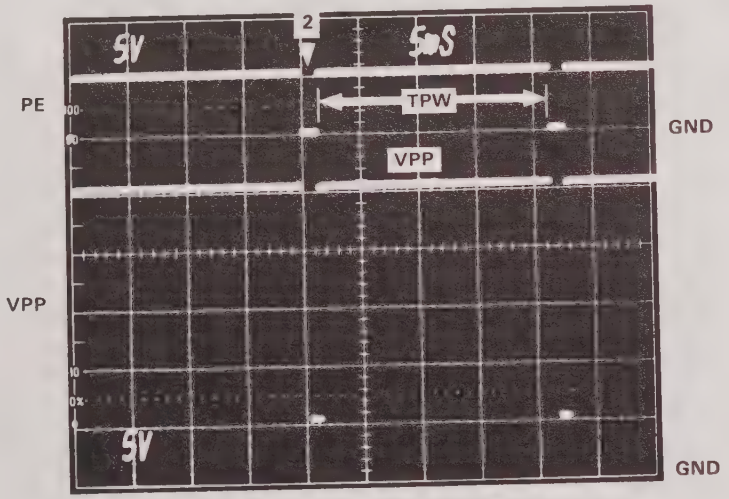
DRAWN BY:

CHECKED BY:

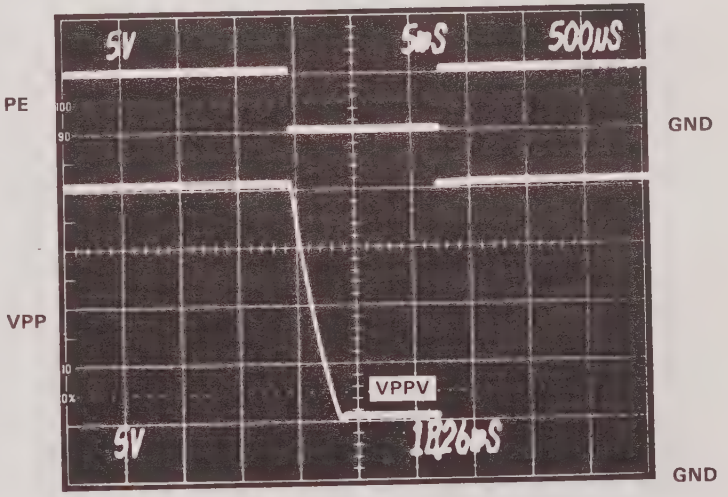
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

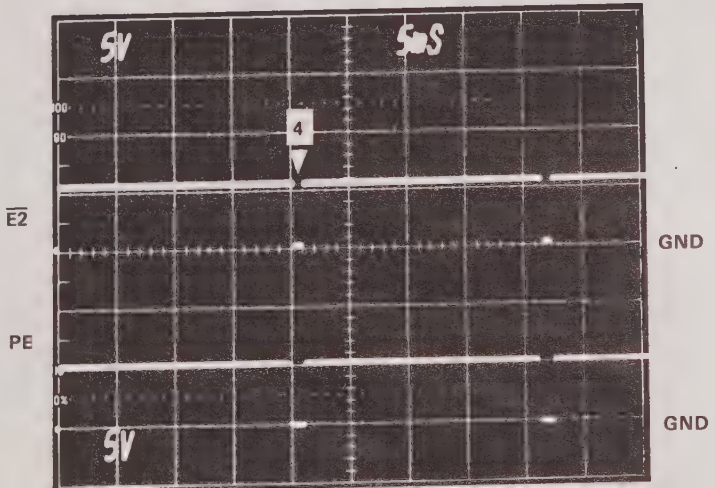
SHEET 2/2

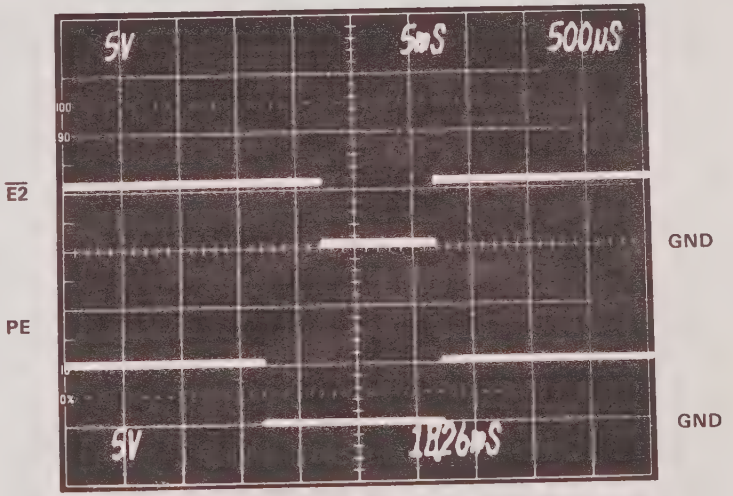

5V
2
5mS
PE
TPW
VPP
GND
VPP
5V
GND

1


5V
5mS
500uS
PE
GND
VPP
VPPV
5V
1826mS
GND

2


5V
5mS
4
E2
GND
PE
5V
GND


5V
5mS
500uS
E2
GND
PE
5V
1826mS
GND

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	19.8	20.0	20.2	ms	
	TR					NA
	TEW	200			ms	
	TF					NA
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 33.*
2. *Load RAM with hex 01 for Family 34, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photo 9 is the erase waveform.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		[illegible]	[illegible]
		ECN #5023		C.J.Z.	3/84

DATA I/O ISSAQUAH, WA

TITLE: **TIMING DIAGRAM**

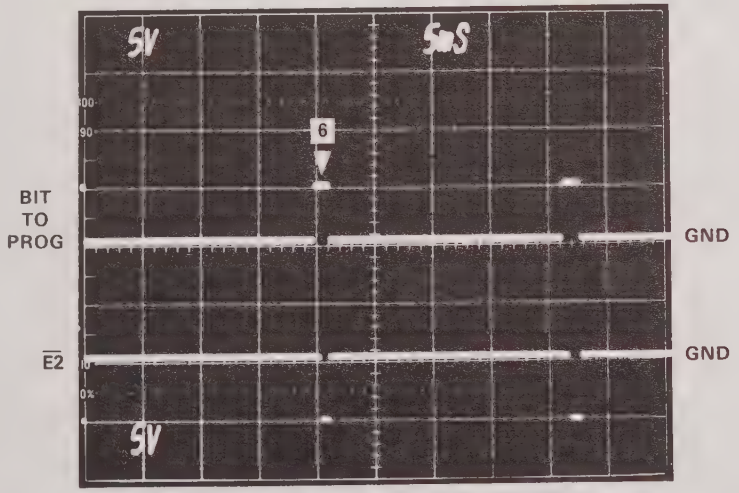
FAMILY CODES 33, 34

DRAWN BY:

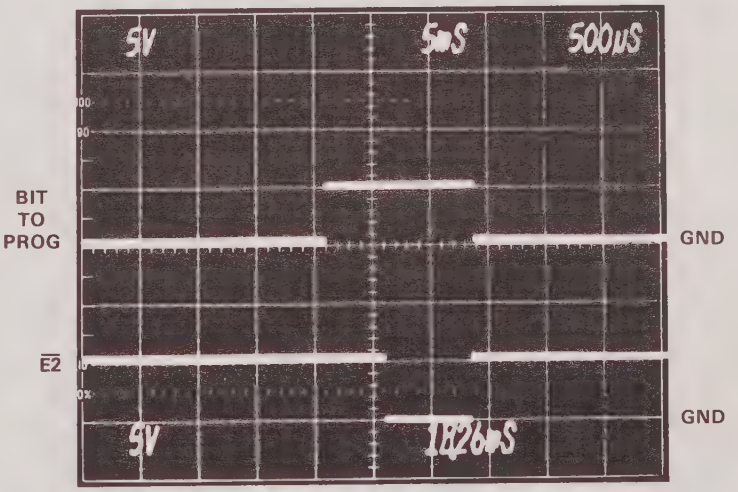
CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

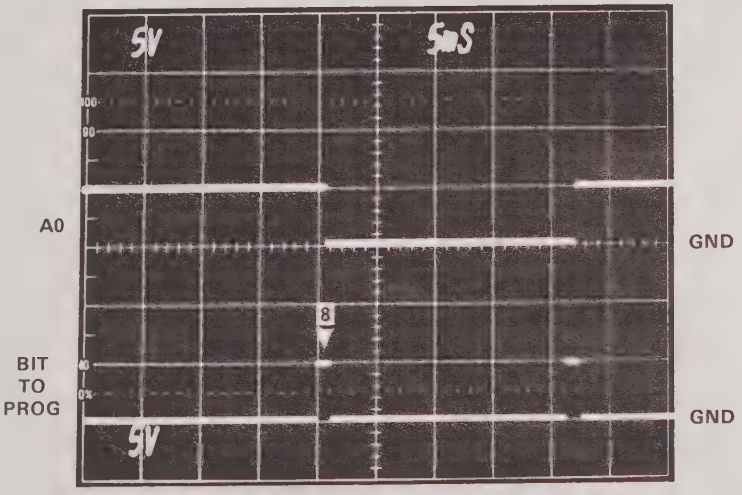
SCALE | SHEET 1/2

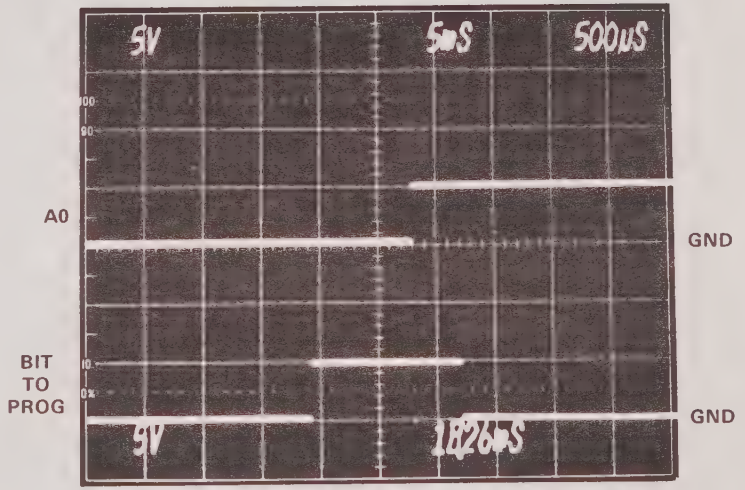

5V
5mS
6
BIT
TO
PROG
GND
E2
GND
5V

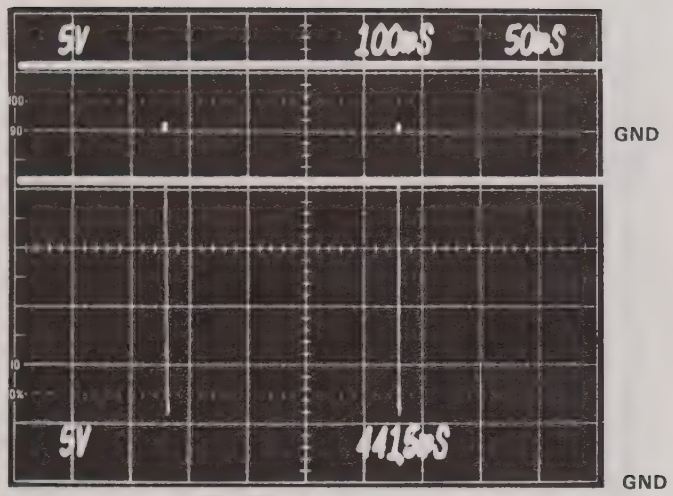
5


5V
5mS
500uS
BIT
TO
PROG
GND
E2
GND
5V
1.026mS

6


5V
5mS
A0
GND
8
BIT
TO
PROG
GND
5V


5V
5mS
500uS
A0
GND
BIT
TO
PROG
GND
5V
1.026mS



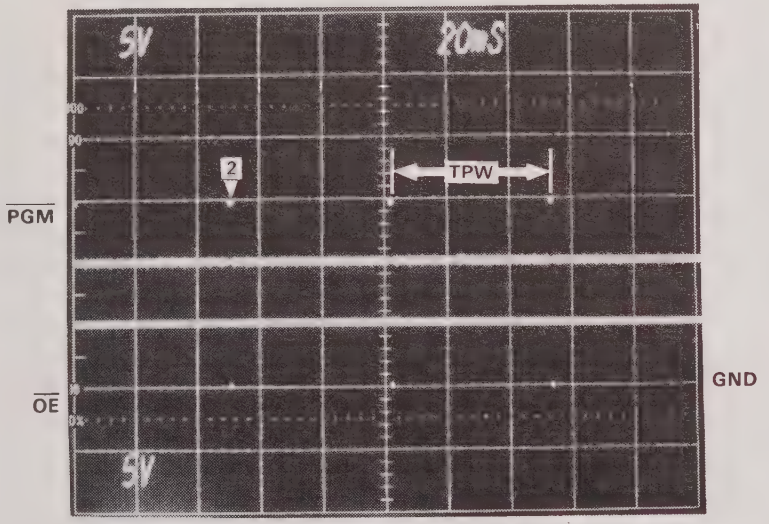
9

B-63
981-0001

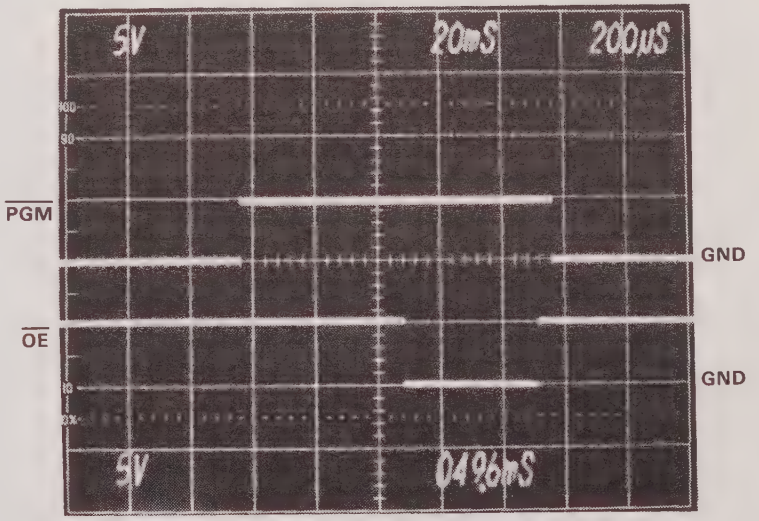
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.J.	11/82
		ECN #4831		[illegible]	[illegible]
		ECN #5023		C7J	3/84

DATA I/O ISSAQUAH, WA

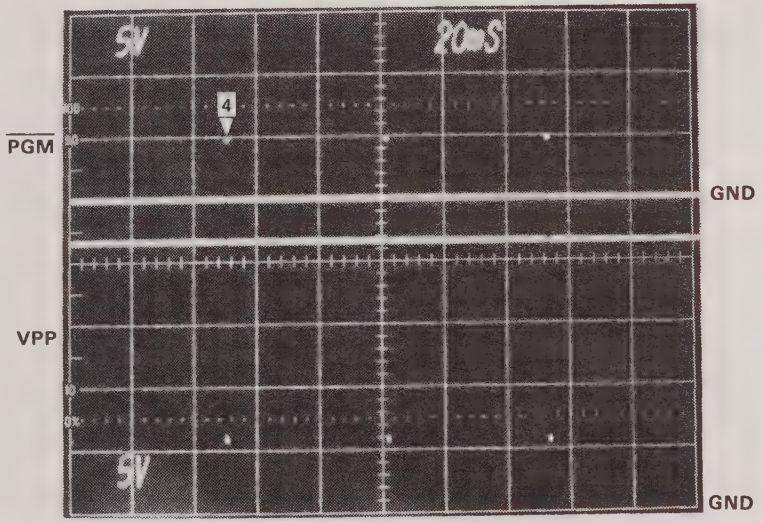
TITLE: TIMING DIAGRAM		DRAWN BY:
FAMILY CODES 33, 34		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2


5V
20mS
2
TPW
PGM
OE
GND
5V

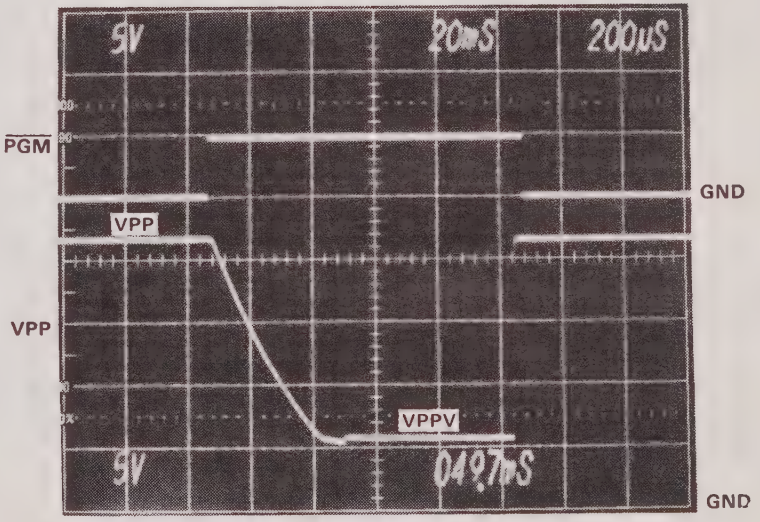
1


5V
20mS
200uS
PGM
GND
OE
GND
5V
04.96mS

2


5V
20mS
4
PGM
GND
VPP
5V
GND

3


5V
20mS
200uS
PGM
GND
VPP
VPP
VPPV
5V
04.97mS
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP	3.8	5.0	6.0	V	
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.00	5.25	V	
	TPW	48	50	52	ms	
	TR					NA
	TF					NA
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

GND

NOTES

1. *Load RAM with hex FE for Family 35.*
2. *Load RAM with hex 01 for Family 36, and bit-to-prog waveform becomes bit-no-prog waveform.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		[illegible]	11/82
		ECN #4831		TA	1/83
		ECN #5023		CTJ	3/84

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 35, 36

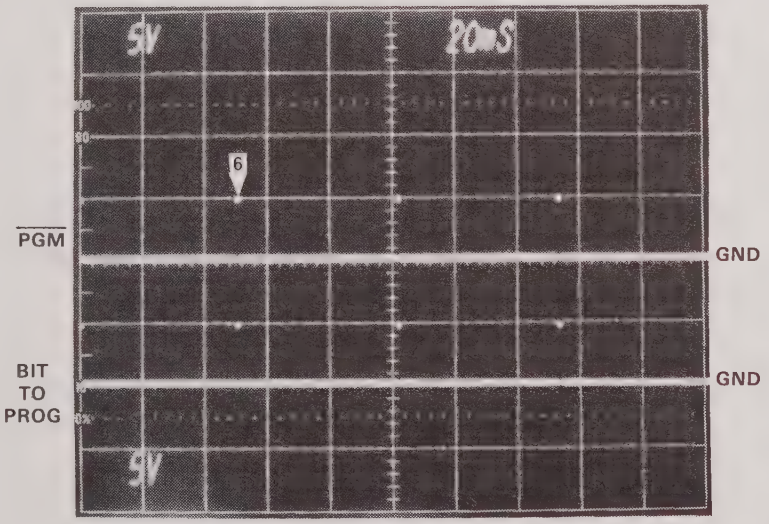
DRAWN BY: BG

CHECKED BY:

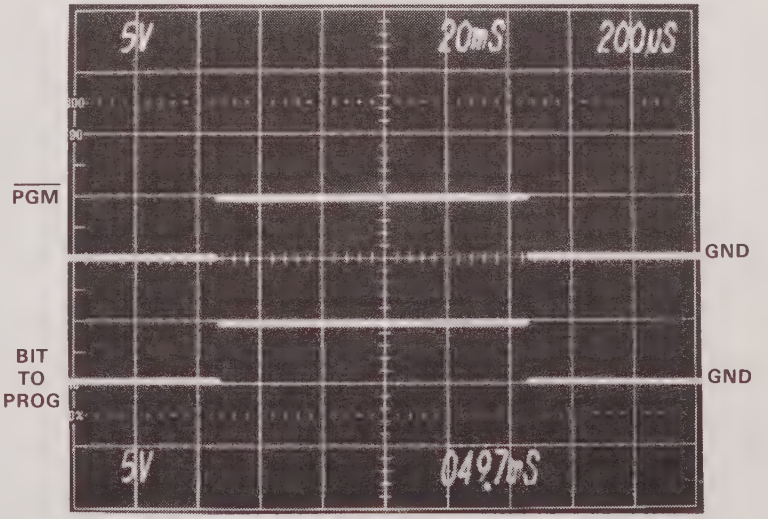
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

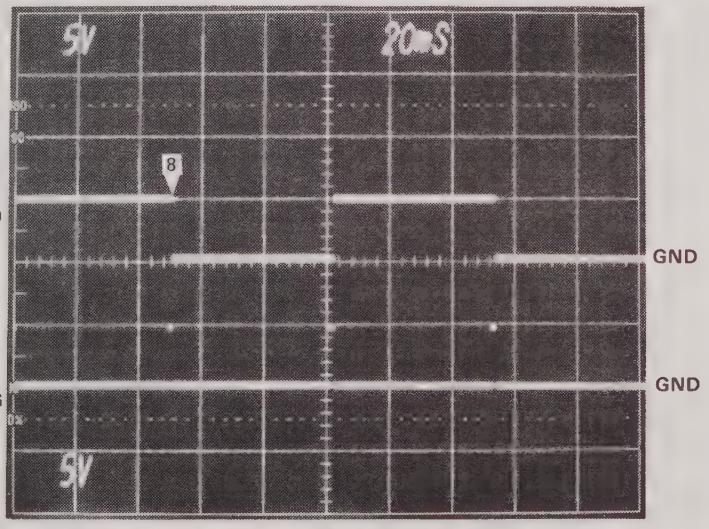
SHEET 1/2


5V
20mS
6
PGM
GND
BIT
TO
PROG
GND
5V

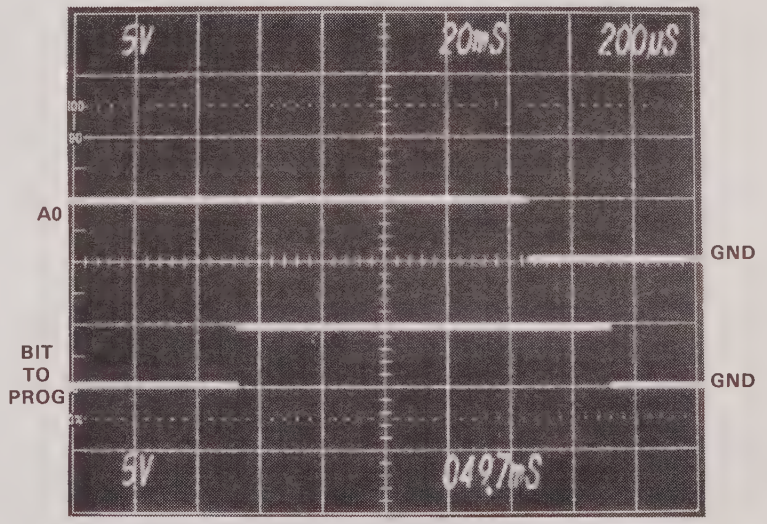
5


5V
20mS
200uS
PGM
GND
BIT
TO
PROG
GND
5V
049.7mS

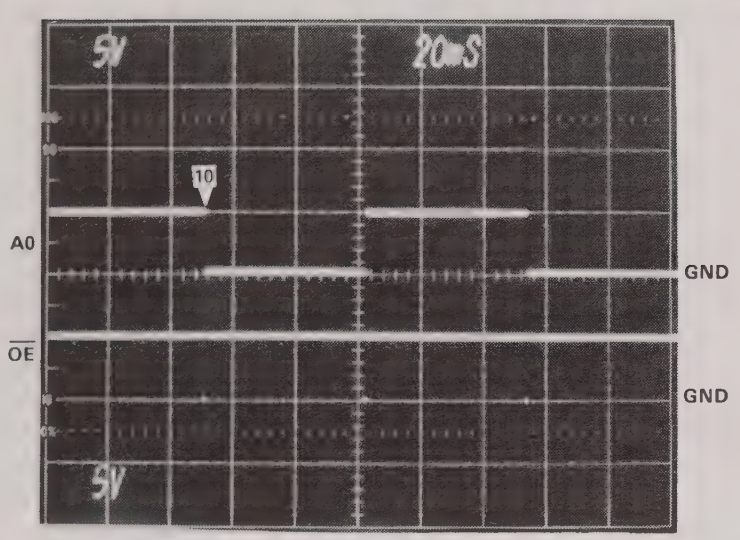
6


5V
20mS
8
A0
GND
BIT
TO
PROG
GND
5V

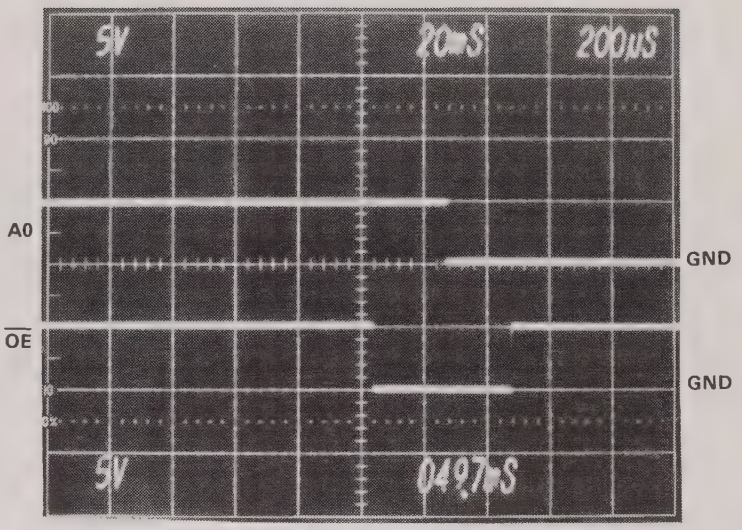
7


5V
20mS
200uS
A0
GND
BIT
TO
PROG
GND
5V
049.7mS

8



9

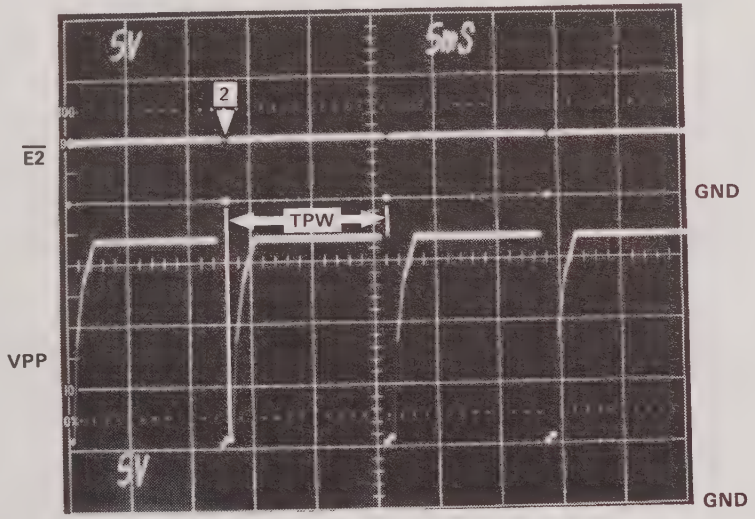


10

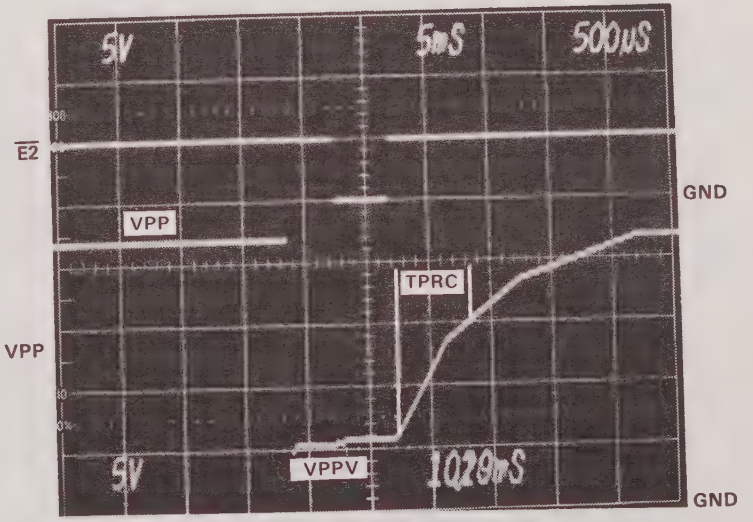
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		22	[illegible]

DATA I/O ISSAQUAH, WA

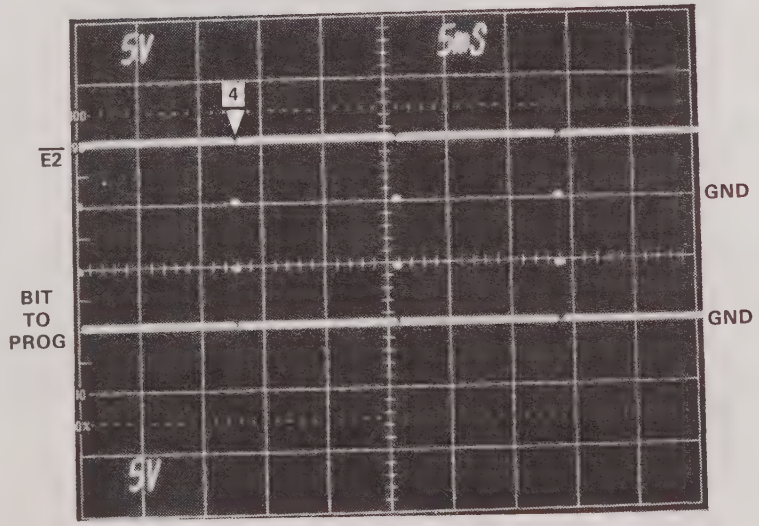
TITLE: TIMING DIAGRAM FAMILY CODES 35, 36		DRAWN BY: BG CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2


5V
5mS
2
E2
GND
TPW
VPP
5V
GND

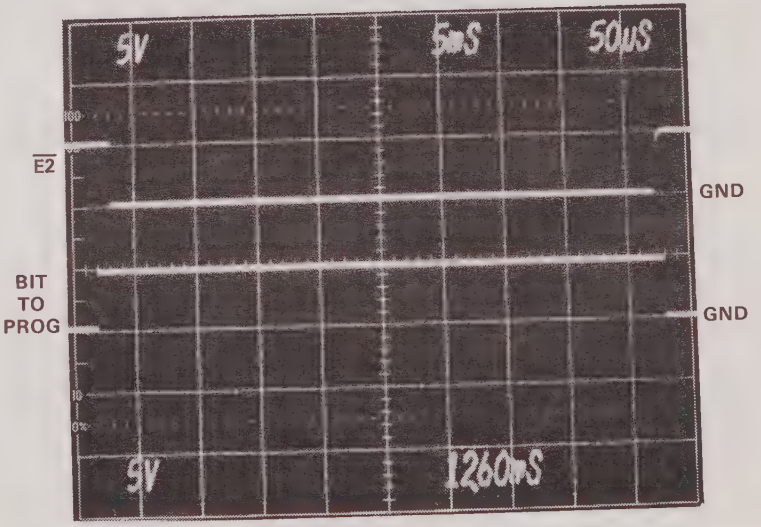
1


5V
5mS
500uS
E2
GND
VPP
TPRC
VPP
VPPV
5V
1029mS
GND

2


5V
5mS
4
E2
GND
BIT
TO
PROG
GND
5V

3


5V
5mS
50uS
E2
GND
BIT
TO
PROG
GND
5V
1260mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VPP	20.0	21.0	22.0	V	
	VPPV	4.0	5.0	6.0	V	
	VOE	9.0	12.0	15.0	V	
	TPW	9.0	10.0	15.0	ms	
	TPRC	450	600	750	µs	See Note 3
	TF			100	µs	
	Reject		2		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 37.*
2. *Load RAM with hex 01 for Family 38, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *TPRC is measured from 6V to 15.5V.*
4. *Photos 10 and 11 are erase waveforms.*

REVISIONS

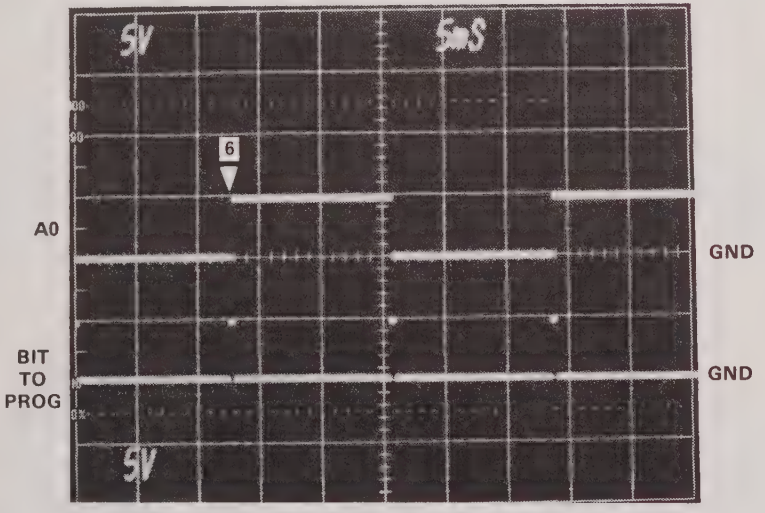
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		KA	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

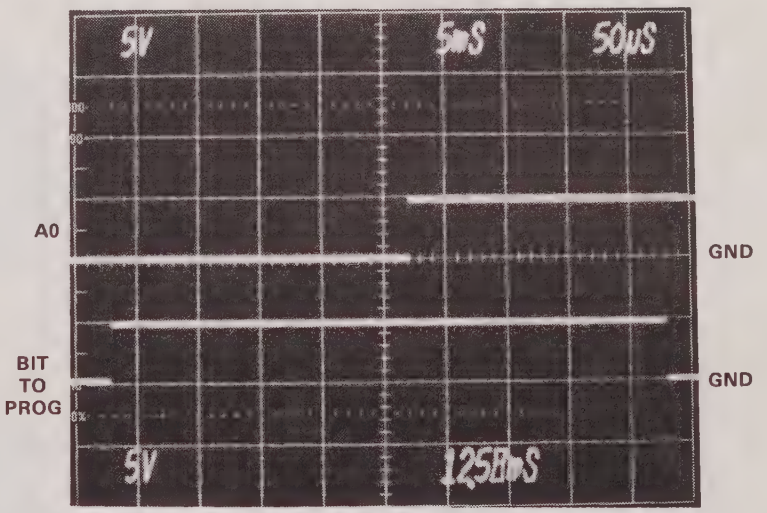
TITLE: TIMING DIAGRAM	DRAWN BY: KEV
FAMILY CODES 37, 38	CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

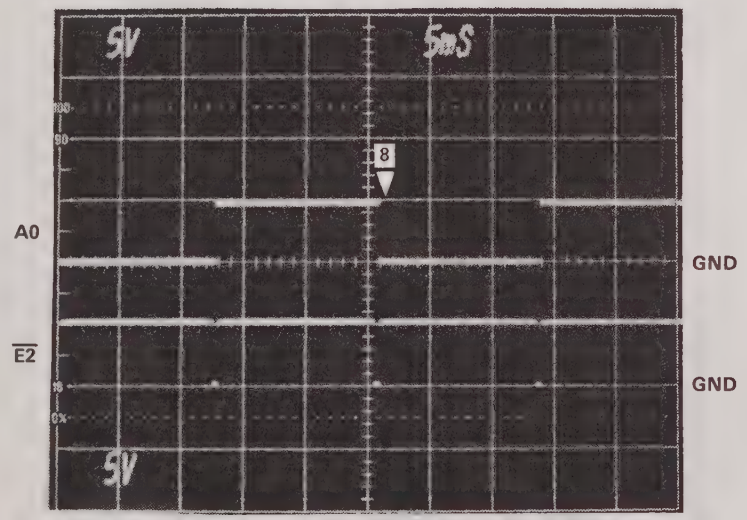
SCALE | SHEET 1/3

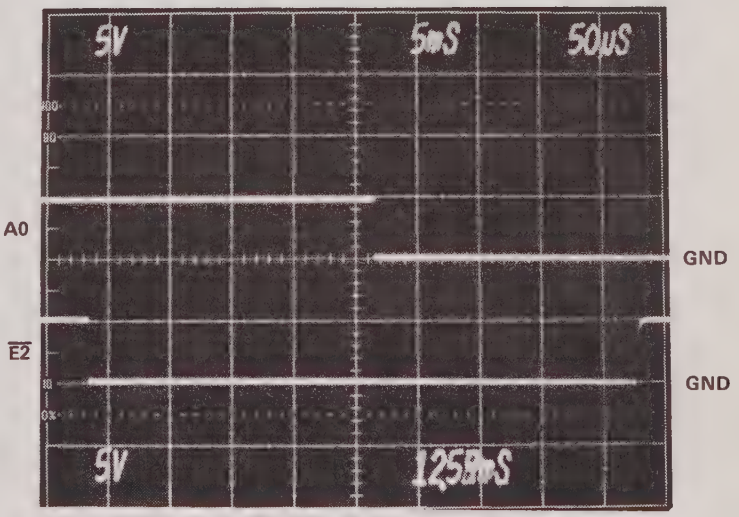

5V
5mS
6
A0
GND
BIT
TO
PROG
GND
5V

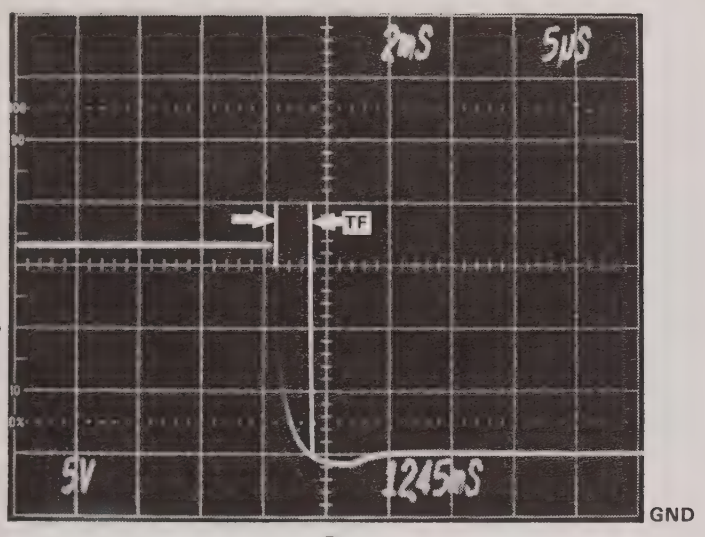
5


5V
5mS
50µS
A0
GND
BIT
TO
PROG
GND
5V
125mS

6


5V
5mS
8
A0
GND
E2
GND
5V


5V
5mS
50µS
A0
GND
E2
GND
5V
125mS



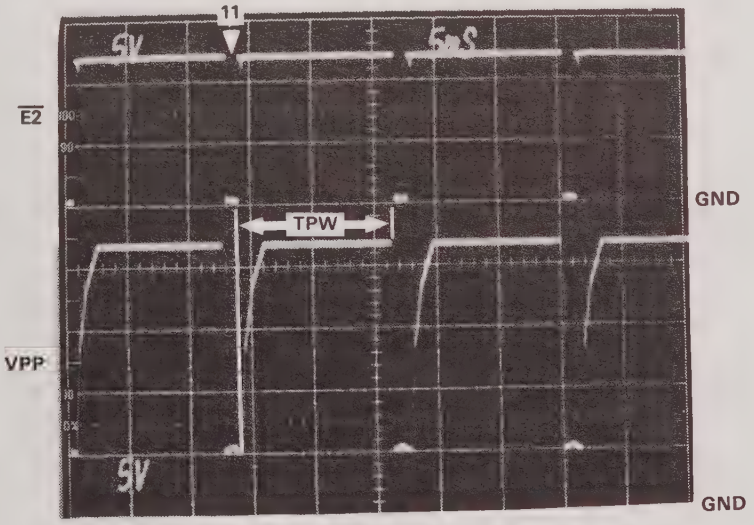
9

B-71
981-0001

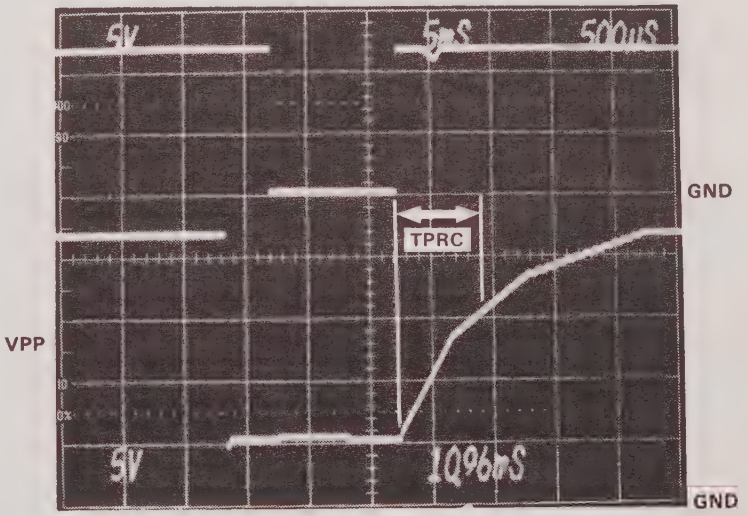
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ	11/82
		ECN #4831		KF	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM		DRAWN BY: KEV
FAMILY CODES 37, 38		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/3


11
5V
5μS
E2
GND
TPW
VPP
5V
GND

10


5V
5μS
500μS
GND
TPRC
VPP
5V
1Q96μS
GND

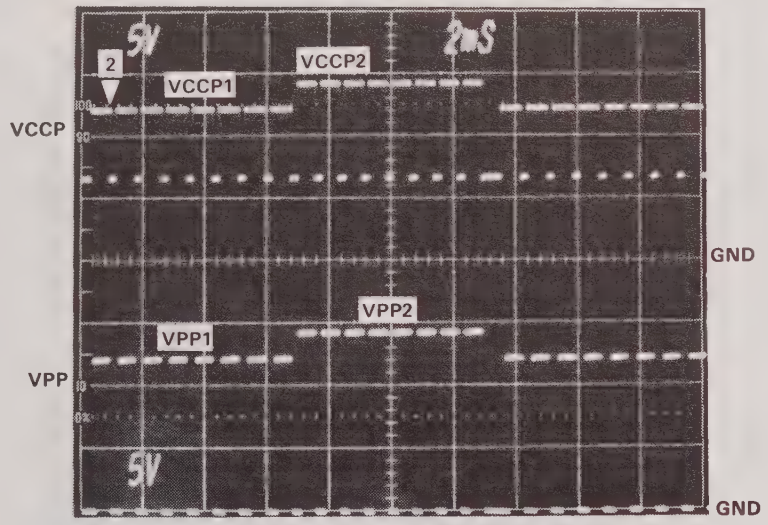
11

B-73
981-0001

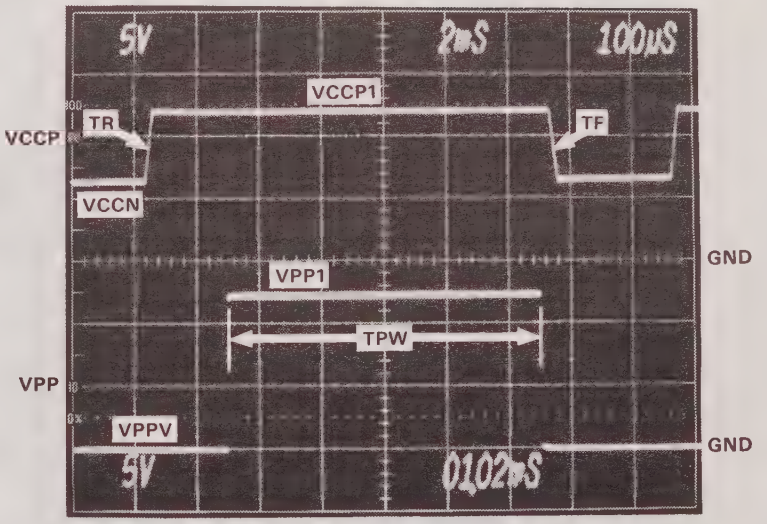
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		JH	5/83

DATA I/O ISSAQUAH, WA

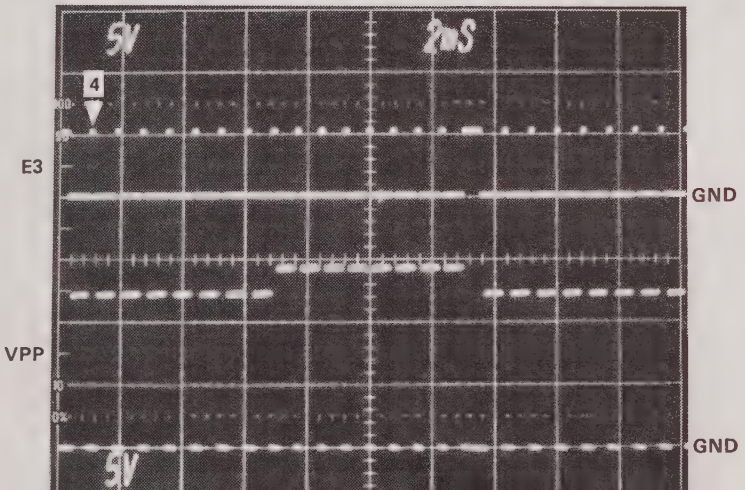
TITLE: TIMING DIAGRAM FAMILY CODES 37, 38		DRAWN BY: KEV CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 3/3

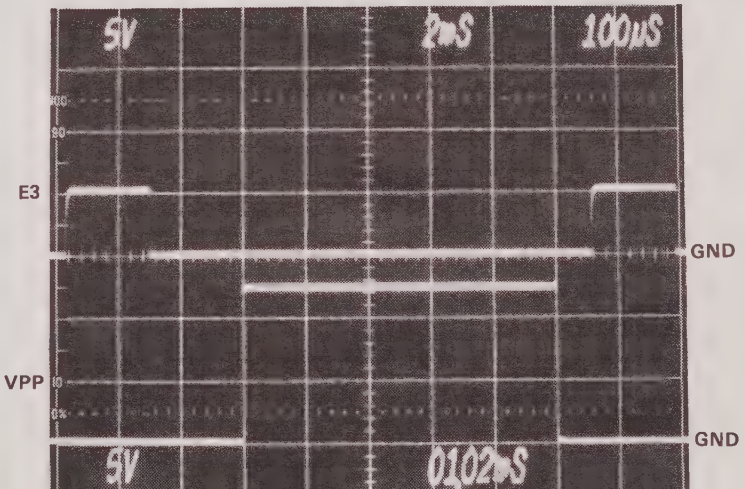

5V
2mS
2
VCCP1
VCCP2
VCCP
GND
VPP2
VPP1
VPP
5V
GND

1


5V
2mS
100µS
VCCP1
VCCP
TR
TF
VCCN
GND
VPP1
TPW
VPP
VPPV
GND
5V
0102mS

2


5V
2mS
4
E3
GND
VPP
GND
5V


5V
2mS
100µS
E3
GND
VPP
GND
5V
0102mS

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCN	6.0	6.5	7.0	V	
	VCCP1	11.5	12.0	12.5	V	Pulses 1-8
	VCCP2	13.5	14.0	14.5	V	Pulses 9-16
	VPP1	11.5	12.0	12.5	V	Pulses 1-8
	VPP2	13.5	14.0	14.5	V	Pulses 9-16
	VPPV	0.0		1.0	V	
	VOP1	11.5	12.0	12.5	V	Pulses 1-8
	VOP2	13.5	14.0	14.5	V	Pulses 9-16
	TPW	450	500	550	µs	
	T_R	1.0			µs	
	T_F	1.0			µs	
	Reject		16		Pulses	
	Overprogram		2		Pulses	
1ST PASS	VCC	3.9	4.0	4.1	V	
VERIFY	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	6.1	7.1	8.1	V	701-1655/TP4
	Low Load	6.1	7.1	8.1	V	701-1655/TP3
2ND PASS	VCC	5.9	6.0	6.1	V	
VERIFY	VREF	4.0	4.1	4.2	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	8.7	9.7	10.7	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 39.*
2. *Load RAM with hex 01 for Family 40.*
3. *V_{CC} is loaded with a 100 Ω, 2-watt resistor.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.T.Z.	11/82
		ECN #4831		XP	5/8
		ECN #5023		CTZ	3/87

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 39, 40

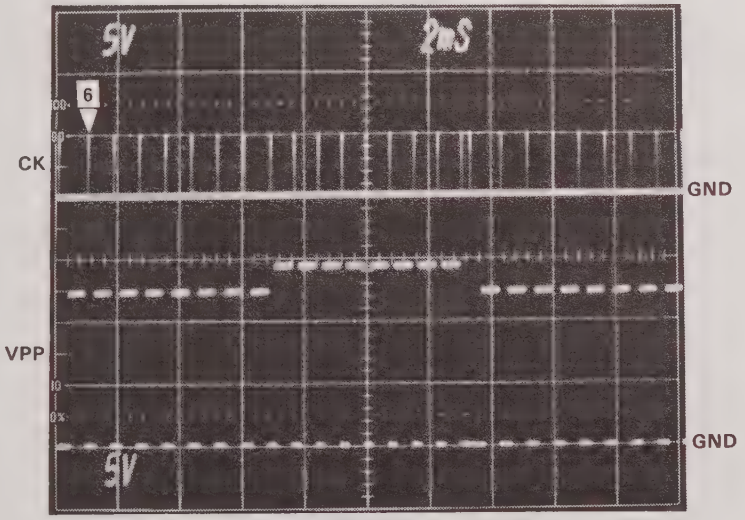
DRAWN BY:

CHECKED BY:

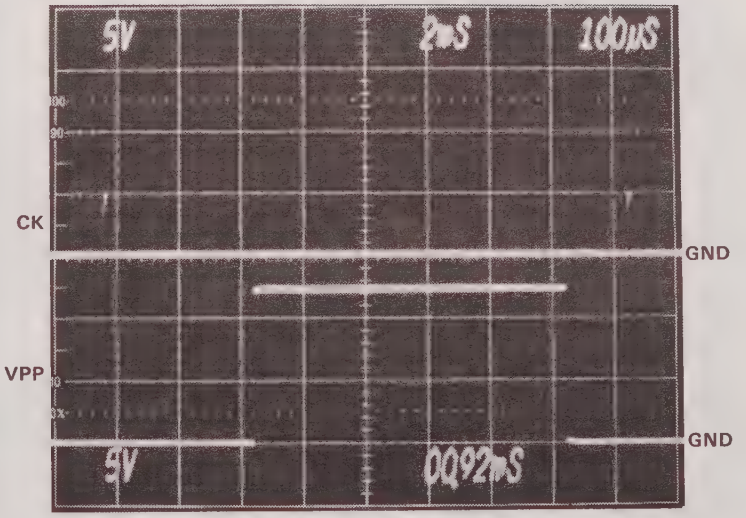
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

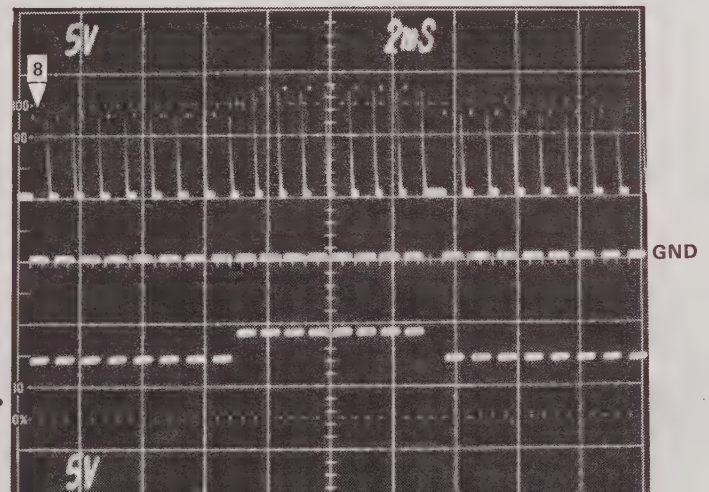
SHEET 1/3

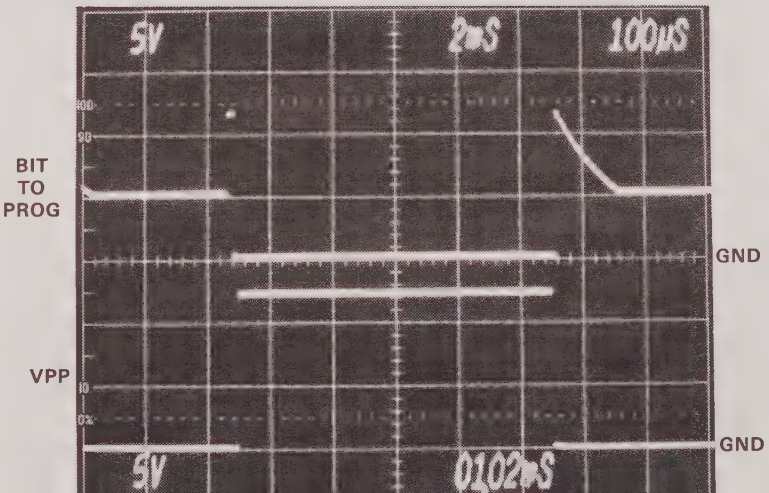

5V
2mS
6
CK
GND
VPP
GND
5V

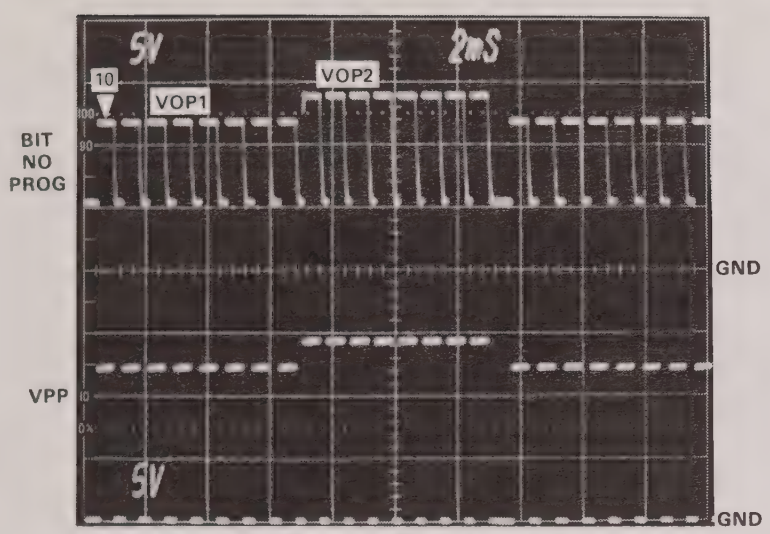
5


5V
2mS
100µS
CK
GND
VPP
GND
5V
0092mS

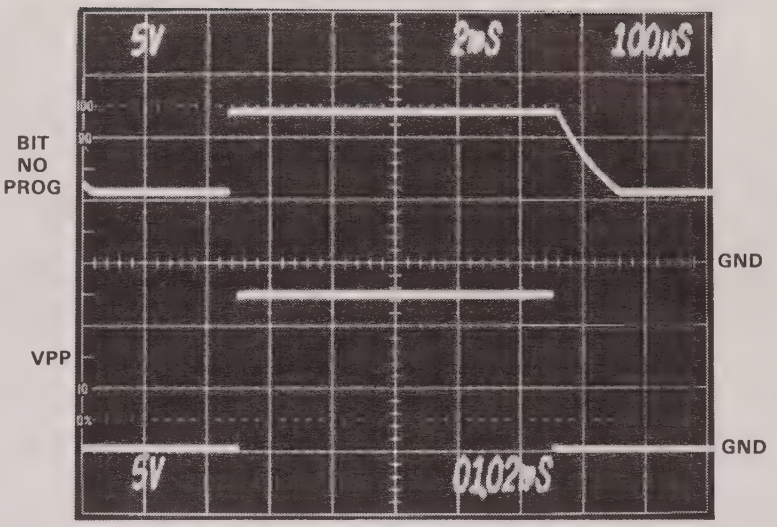
6


5V
2mS
8
BIT
TO
PROG
GND
VPP
5V


5V
2mS
100µS
BIT
TO
PROG
GND
VPP
GND
5V
0102mS



9

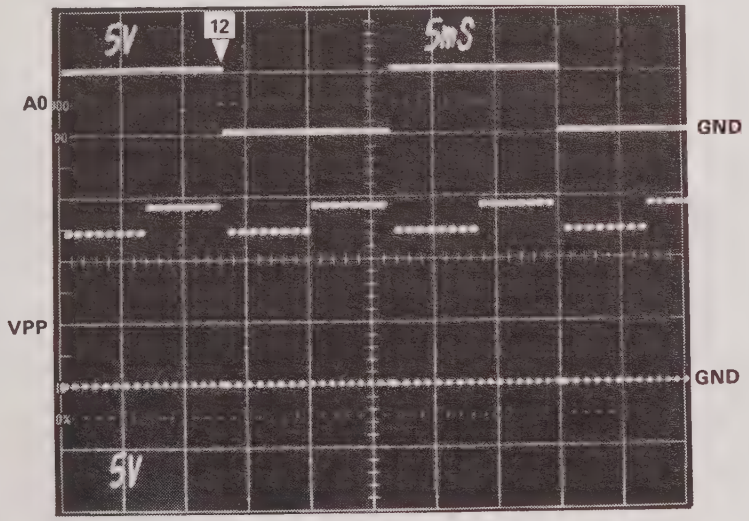


1C

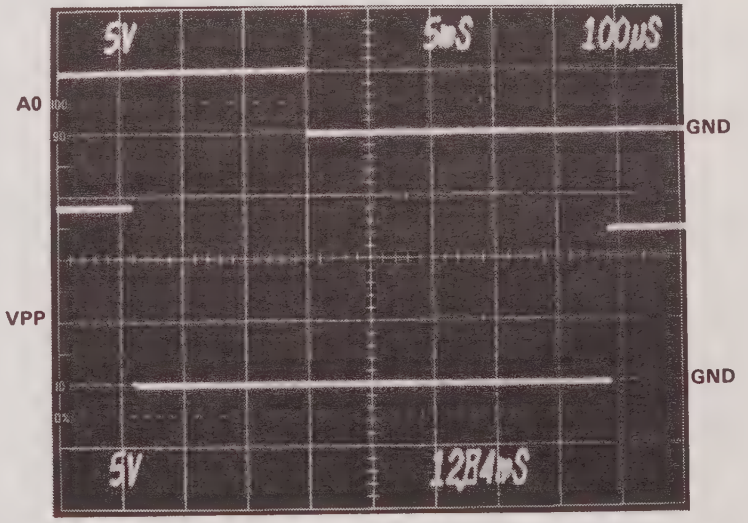
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		J.K	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 39, 40		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/3



11

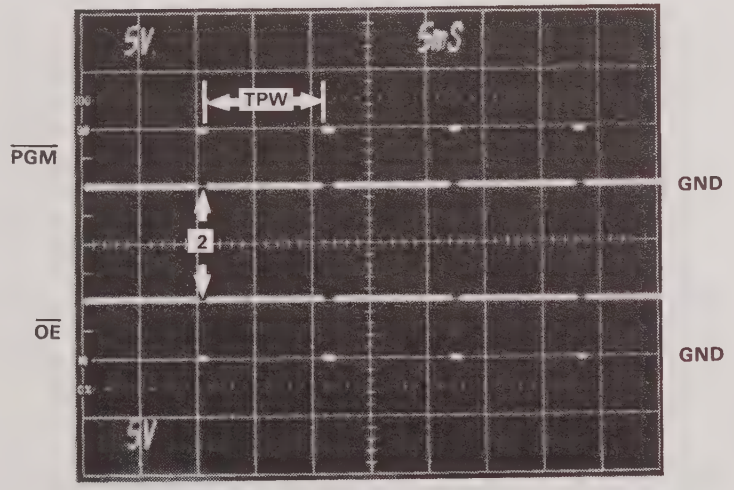


12

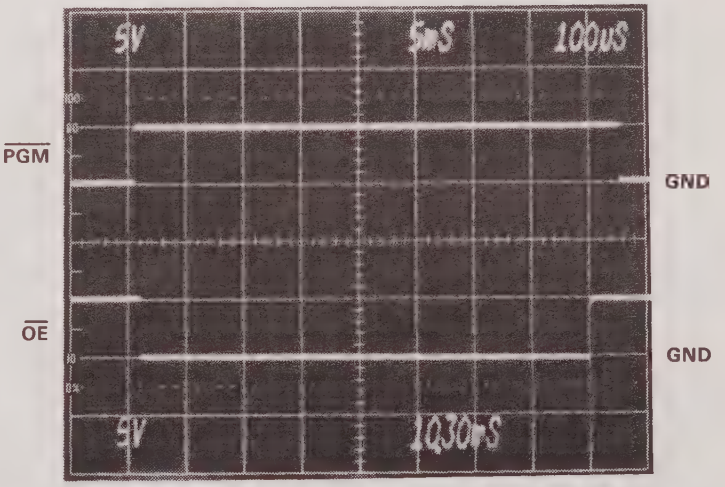
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.T.J.	11/82
		ECN #4831		XX	5/83

DATA I/O ISSAQUAH, WA

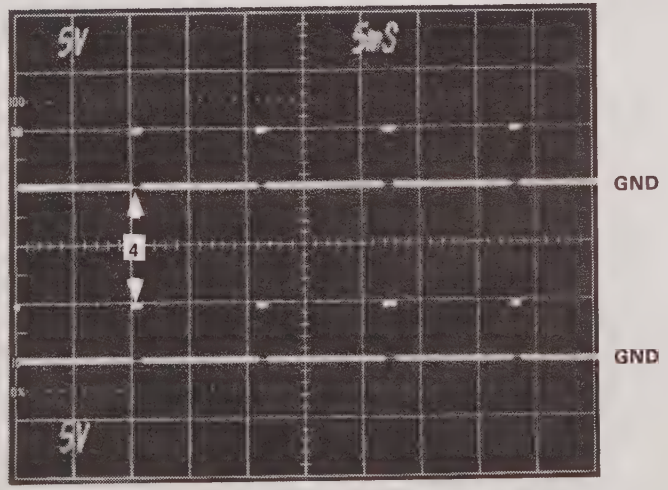
TITLE: TIMING DIAGRAM FAMILY CODES 39, 40		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0099
SCALE		SHEET 3/3


5V
5mS
TPW
PGM
GND
2
OE
GND
5V

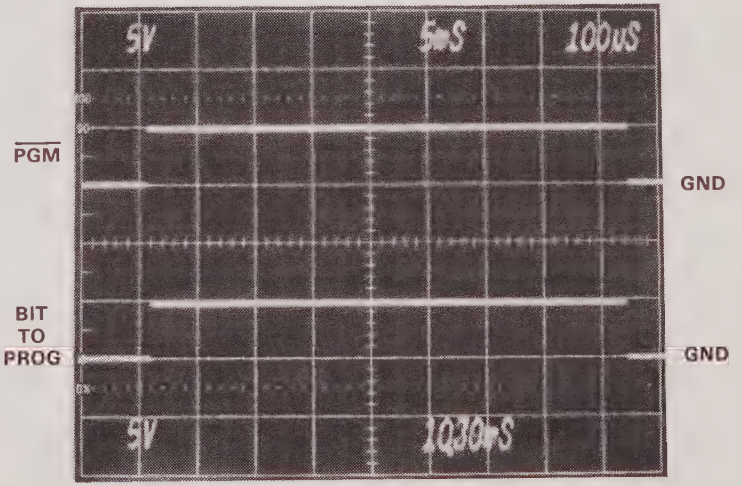
1


5V
5mS
100uS
PGM
GND
OE
GND
5V
1Q30mS

2


5V
5mS
PGM
GND
4
BIT
TO
PROG
GND
5V

3


5V
5mS
100uS
PGM
GND
BIT
TO
PROG
GND
5V
1Q30mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VPP	12.0	12.5	13.0	V	Not Shown
	TPW	9.5	10.0	10.5	ms	
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.3	5.3	6.3	V	701-1655/TP4
	LOW LOAD	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 3B.*
2. *Load RAM with hex 01 for Family 3C*

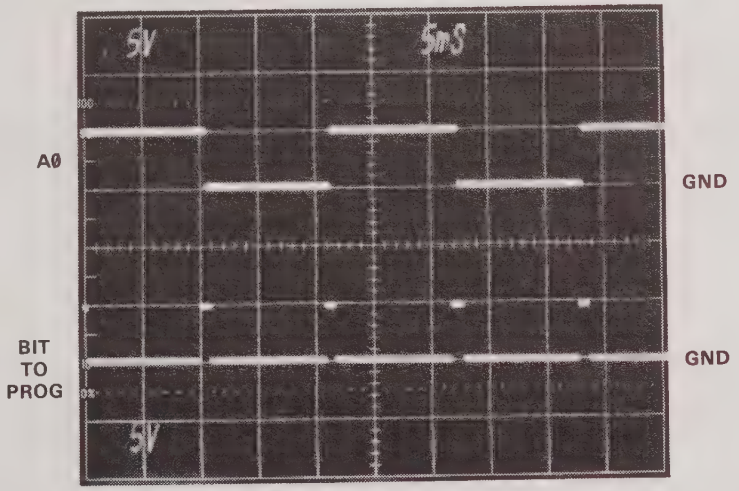
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

TIMING DIAGRAM

FAMILY CODES 3B, 3C

DATA I/O



5

B-83
981-0001

REVISIONS

LTR	DESCRIPTION	P.E.	DATE

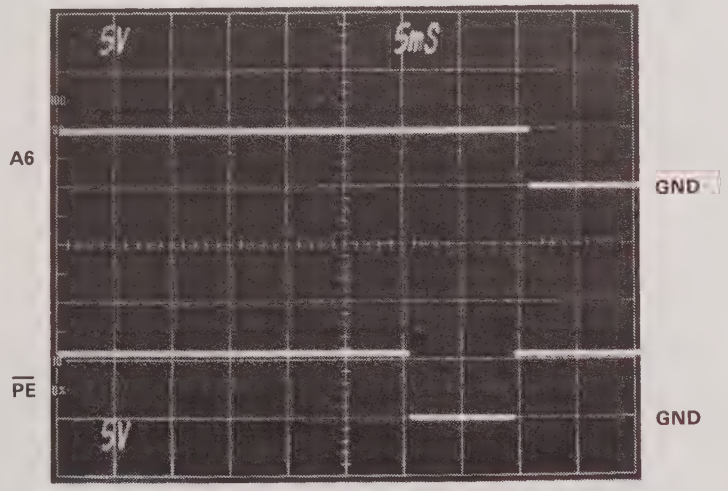
Sheet 2 of 2

TIMING DIAGRAM

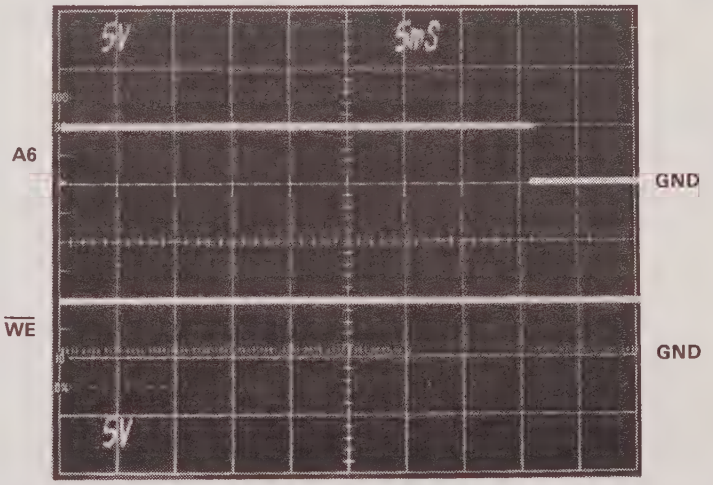
FAMILY CODES 3B, 3C

DATA I/O

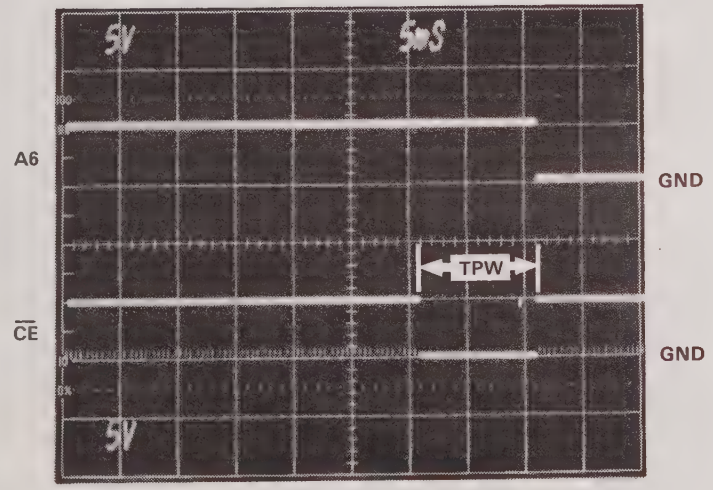
0526/1282


5V
5mS
A6
GND
PE
GND
5V

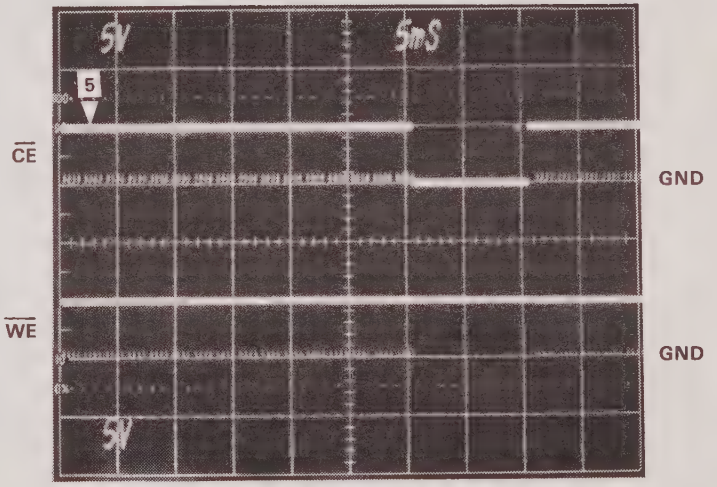
1


5V
5mS
A6
GND
WE
GND
5V

2


5V
5mS
A6
GND
TPW
CE
GND
5V

3


5V
5mS
5
CE
GND
WE
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	TPW	10.0			ms	
	TEW	100			ms	
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.3	5.3	6.3	V	701-1655/TP4
	LOW LOAD	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 3D.*
2. *Load RAM with hex 01 for Family 3E*
3. *Photos 6 and 7 show erase pulse.*

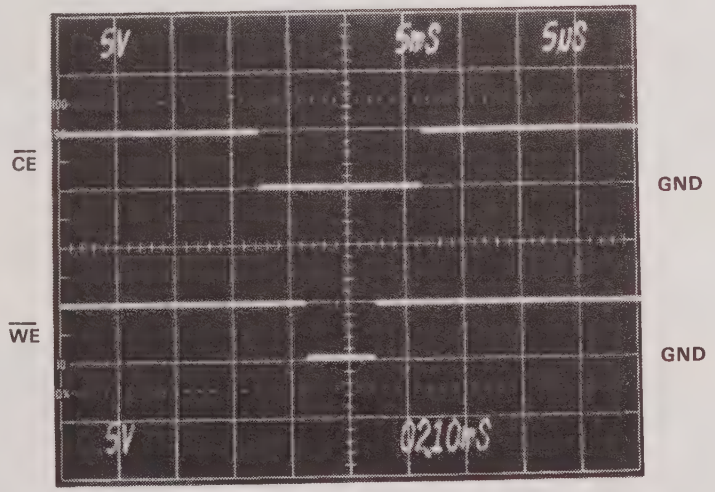
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

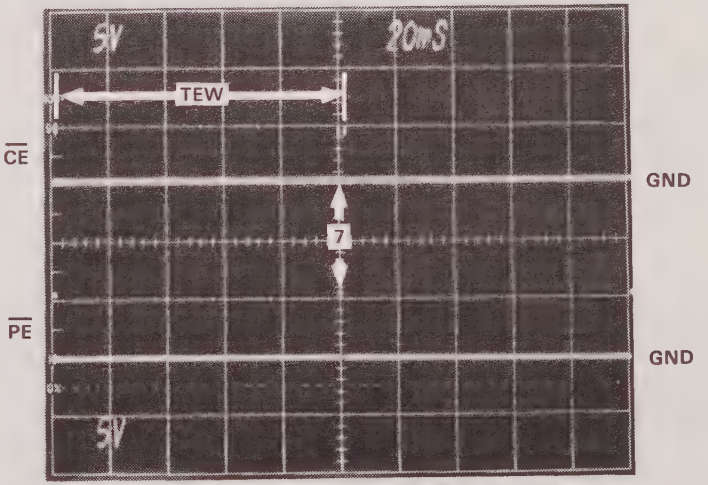
TIMING DIAGRAM

FAMILY CODES 3D, 3E

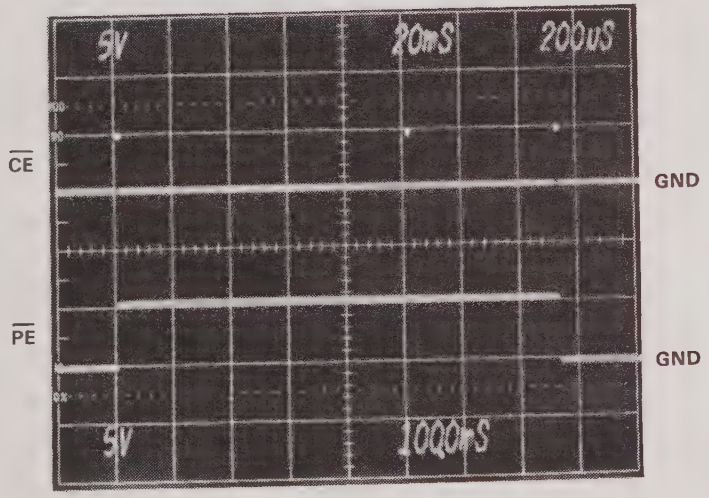
DATA I/O


5V
5mS
5uS
CE
GND
WE
GND
5V
0210mS

5


5V
20mS
TEW
CE
GND
7
PE
GND
5V

6


5V
20mS
200uS
CE
GND
PE
GND
5V
1000mS

7

B-87
981-0001

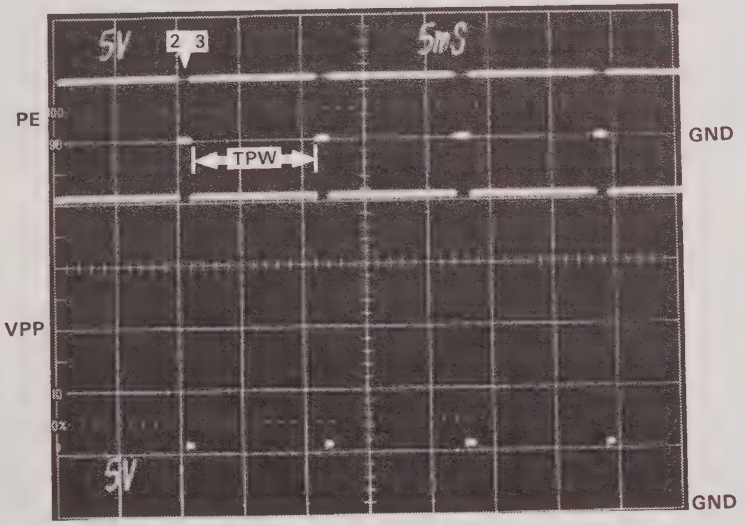
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

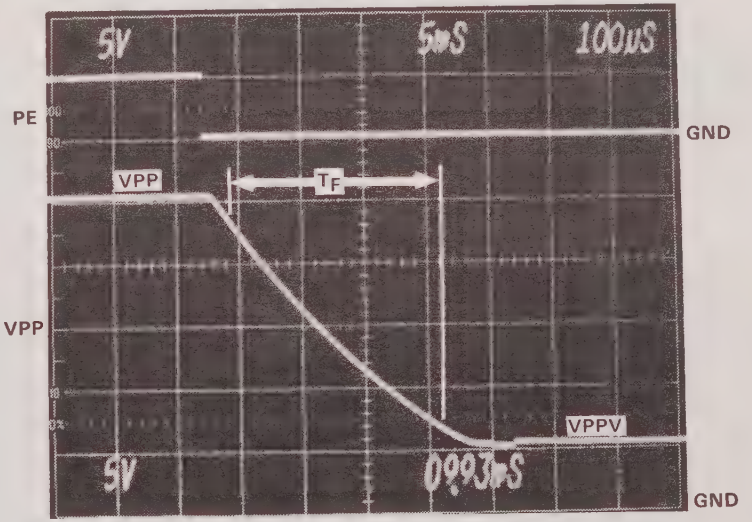
TIMING DIAGRAM

FAMILY CODES 3D, 3E

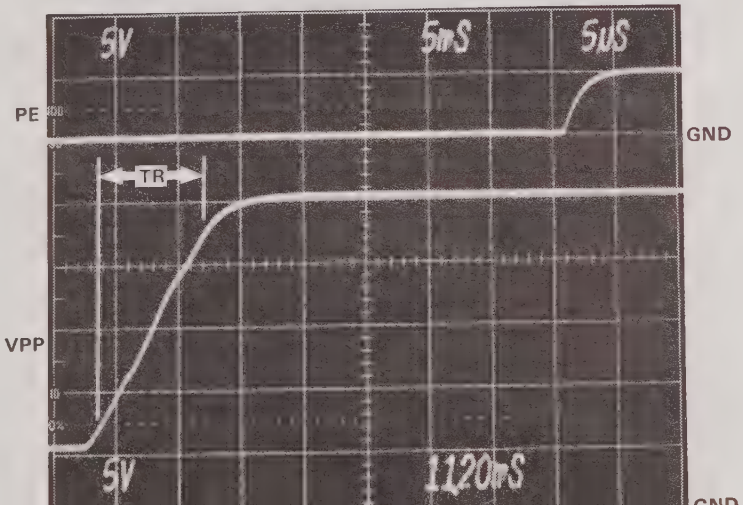
DATA I/O

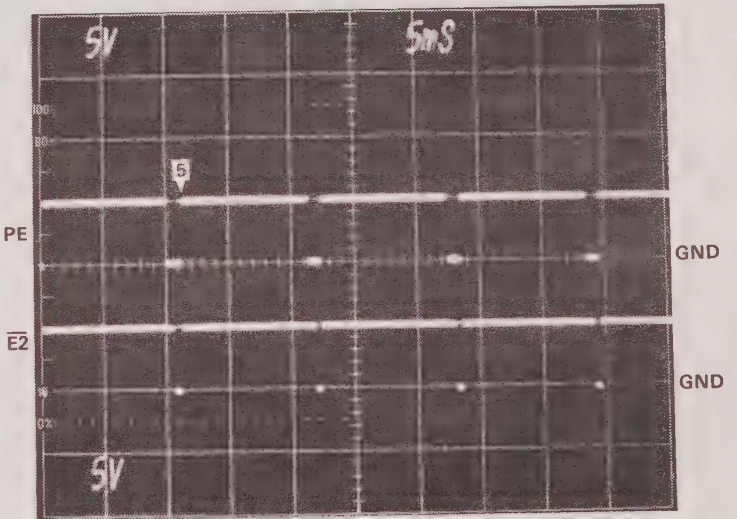

5V
2 3
5mS
PE
GND
TPW
VPP
5V
GND

1


5V
5mS
100uS
PE
GND
VPP
TF
VPP
VPPV
5V
0?9?3mS
GND

2


5V
5mS
5uS
PE
GND
TR
VPP
5V
1120mS
GND


5V
5mS
5
PE
GND
E2
GND
5V

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.00	5.25	V	
	TPW	9.8	10.0	10.2	ms	
	TR	50			ns	
	TEP	98	100	102	ms	
	TF	50			ns	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 43.*
2. *Load RAM with hex 01 for Family 44, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photo 10 is the erase waveform.*

REVISIONS

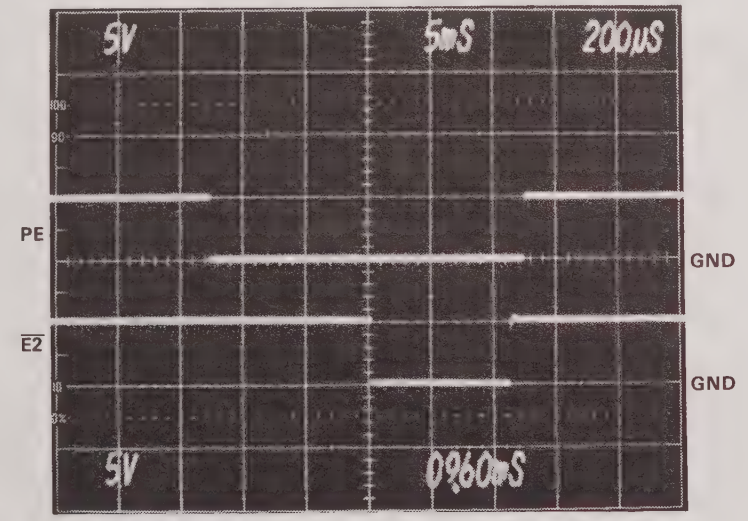
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		XA	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

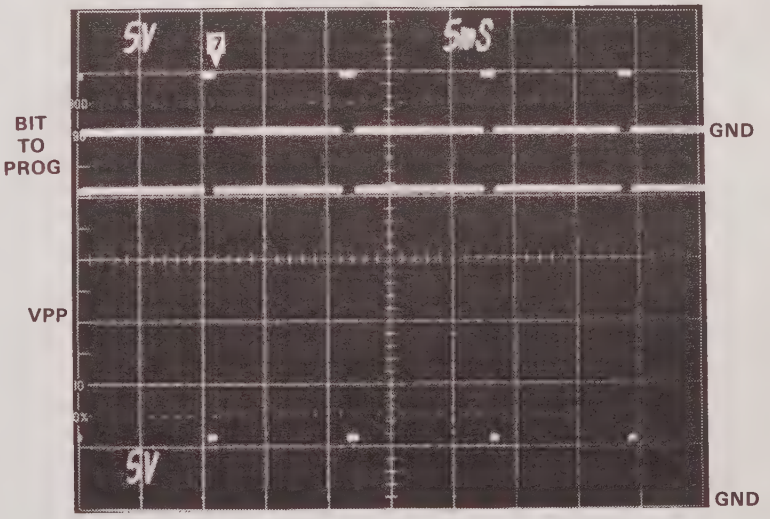
TITLE: TIMING DIAGRAM FAMILY CODES 43, 44	DRAWN BY: EE CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

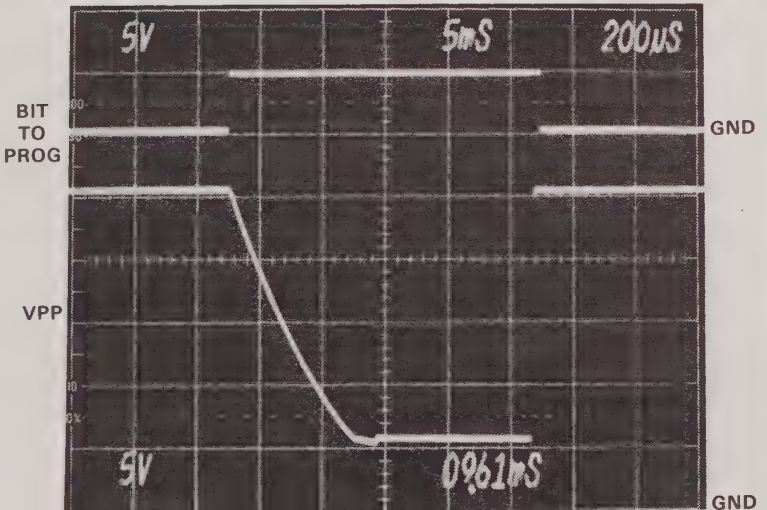
SCALE | SHEET 1/2

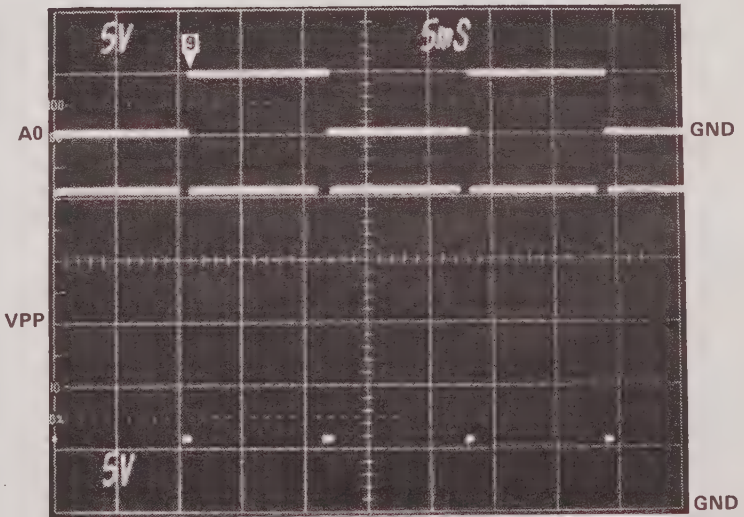

5V
5mS
200µS
PE
GND
$\overline{E2}$
GND
5V
0960mS

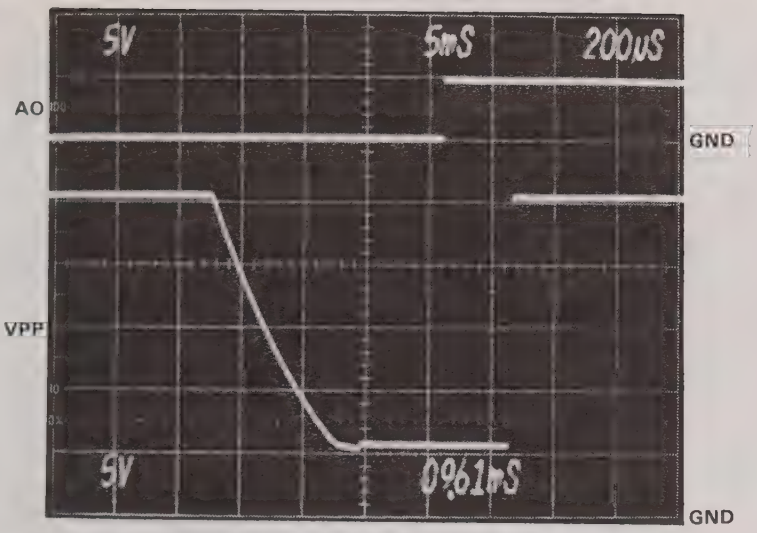
5


5V
7
5mS
BIT
TO
PROG
GND
VPP
5V
GND

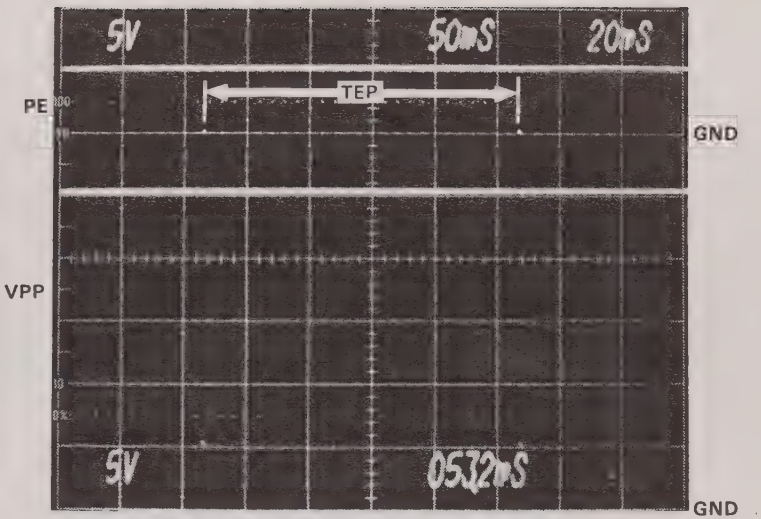
6


5V
5mS
200µS
BIT
TO
PROG
GND
VPP
5V
0961mS
GND


5V
9
5mS
A0
GND
VPP
5V
GND



9



10

B-91
981-0001

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z	11/82
		ECN #4831		JA	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

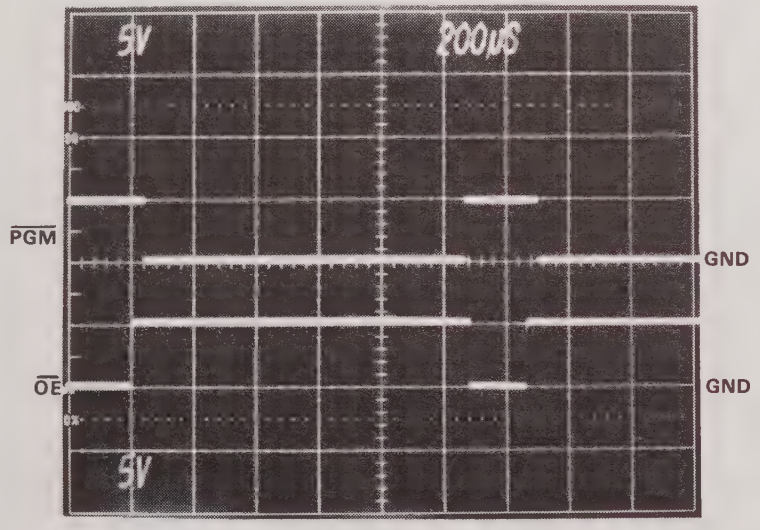
FAMILY CODES 43, 44

DRAWN BY: EE

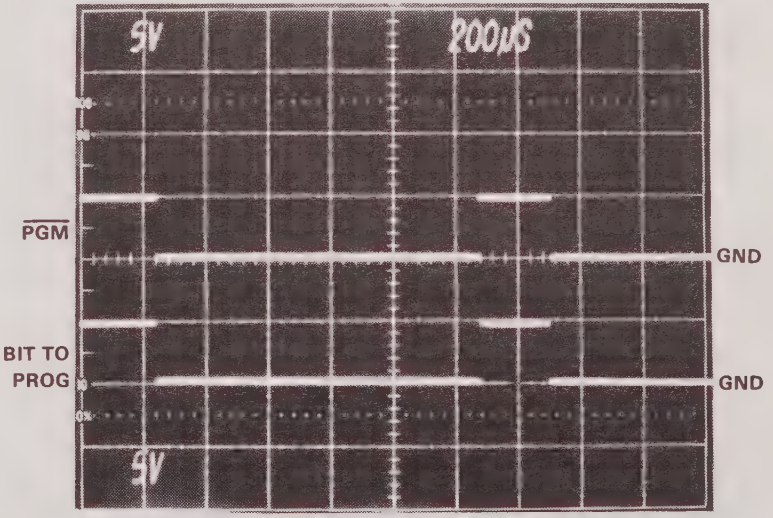
CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

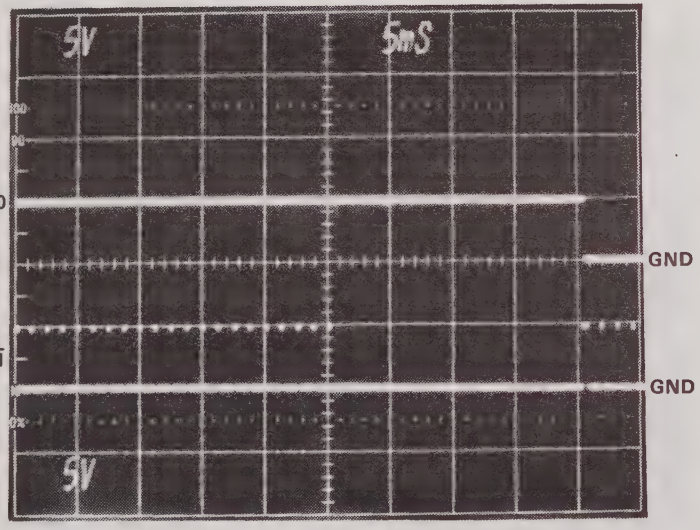
SCALE | SHEET 2/2


5V
200µS
PGM
GND
OE
GND
5V

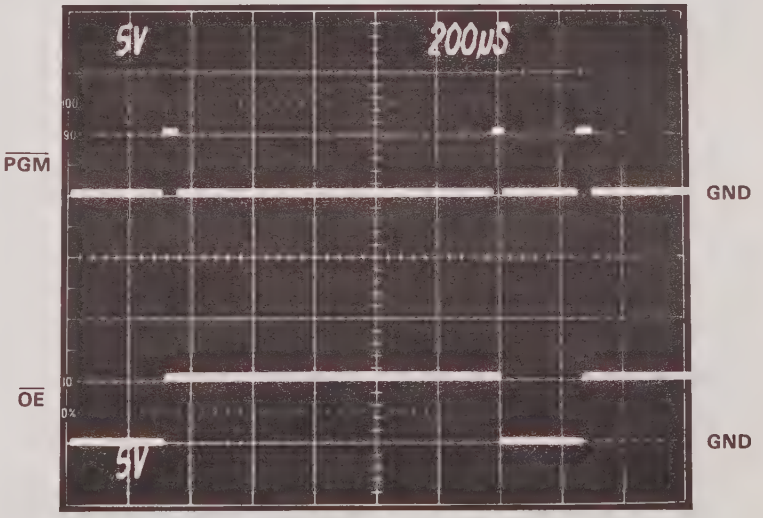
1


5V
200µS
PGM
GND
BIT TO
PROG
GND
5V

2


5V
5mS
A0
GND
PGM
GND
5V

3


5V
200µS
PGM
GND
OE
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.00	6.25	V	Not shown
	VOP					NA
	VPP	20.5	21.0	21.5	V	Not shown
	VPPV					NA
	TPW	.95	1.0	1.05	ms	
	TR					NA
	TF					NA
	Reject		20		Pulses	
	Overprogram		1		Pulse	See note 3
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

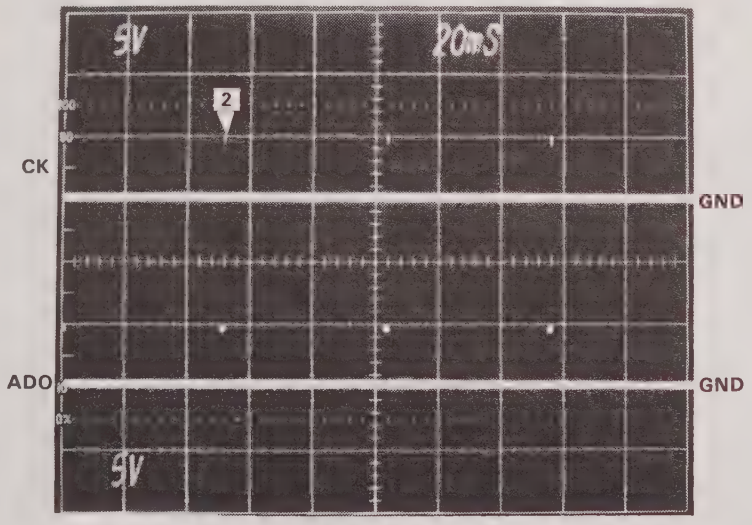
1. *Load RAM with hex FE for Family 45.*
2. *Load RAM with hex 01 for Family 46 and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The overprogram pulse is 1 ms times the number of programming pulses required to program the location.*
4. *Photo 4 is for Pinout 32.*

REVISIONS

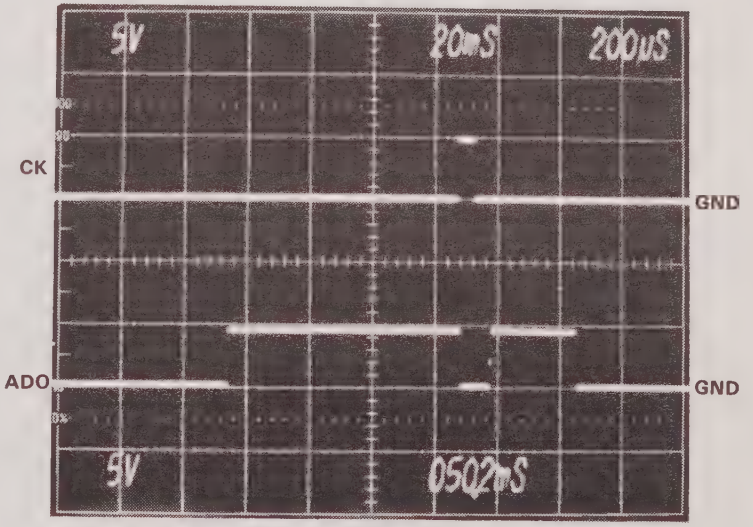
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		XH	5/83
		ECN #5023		CJZ	3/84

DATA I/O

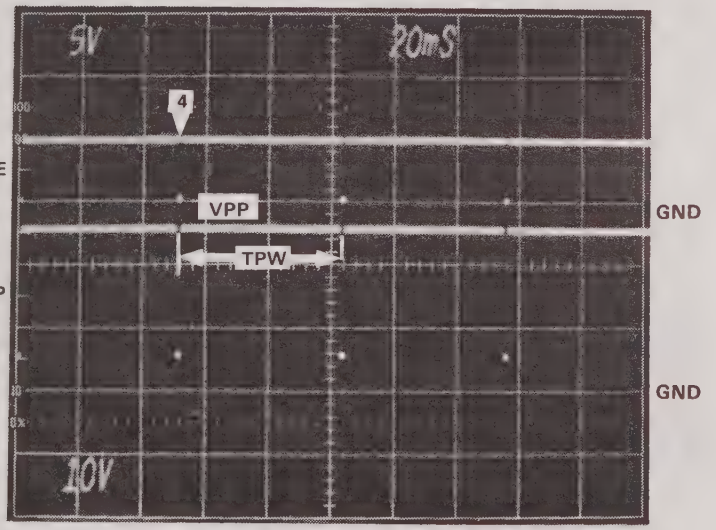
TITLE: TIMING DIAGRAM FAMILY CODES 45, 46		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 1


5V
20mS
2
CK
GND
ADO
GND
5V

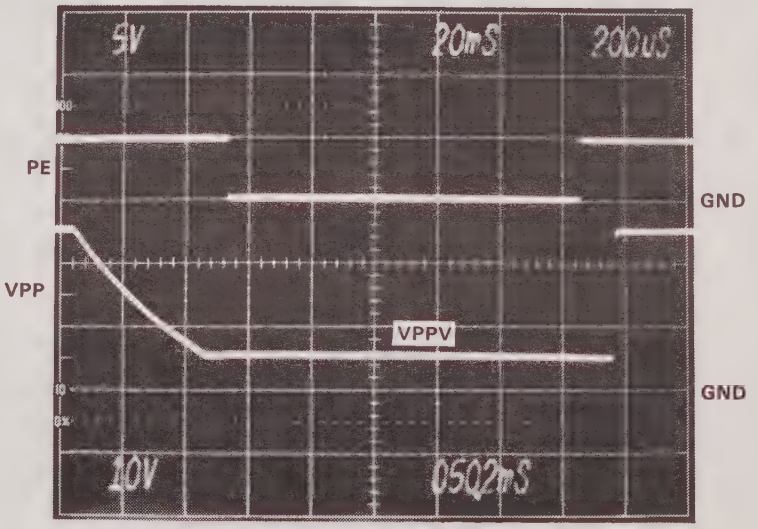
1


5V
20mS
200uS
CK
GND
ADO
GND
5V
0502mS

2


5V
20mS
4
PE
VPP
GND
VPP
TPW
GND
10V

3


5V
20mS
200uS
PE
GND
VPP
VPPV
GND
10V
0502mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not shown
	VOP					NA
	VPP	24.5	25.0	25.5	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	49.0	50.0	51.0	ms	
	TR					NA
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

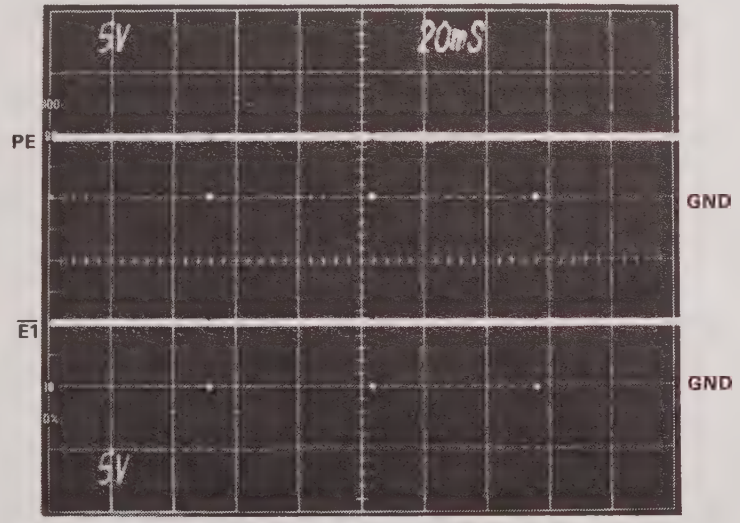
1. *Load RAM with hex FE for Family 47.*
2. *Load RAM with hex 01 for Family 48 and bit-to-prog waveform becomes bit-no-prog waveform.*

REVISIONS

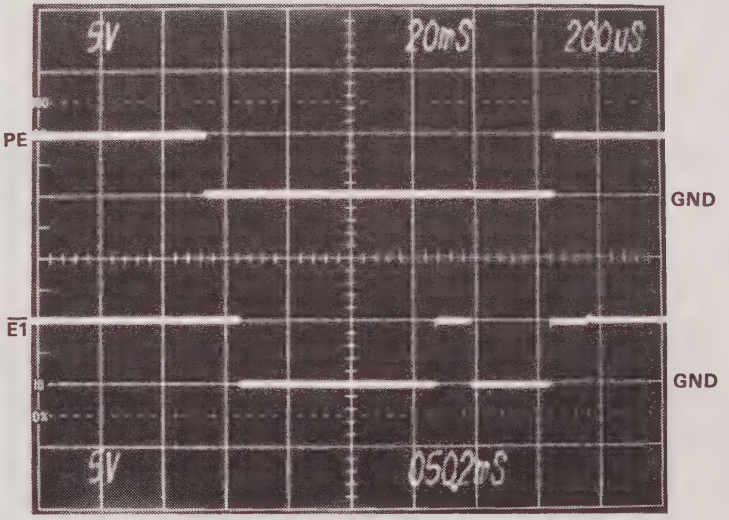
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		XH	5/83
		ECN #5023		CDZ	3/84

DATA I/O

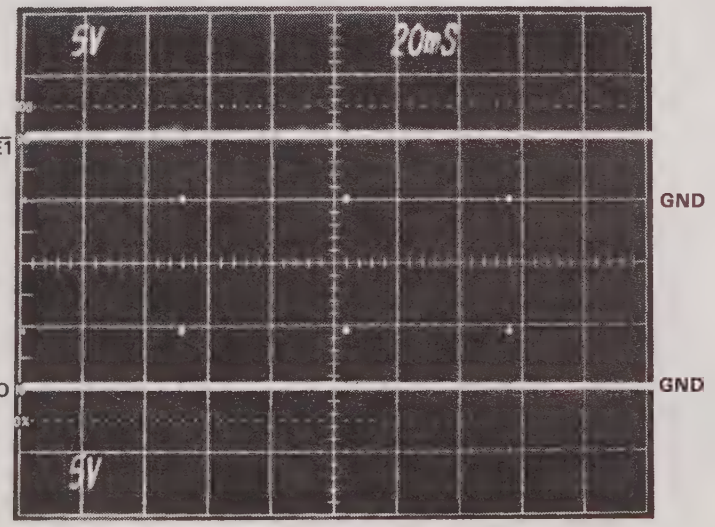
TITLE: TIMING DIAGRAM FAMILY CODES 47, 48	DRAWN BY:
	CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193
DRAWING NO.: 33-950-0059	
SCALE	SHEET 1 of 2


5V
20mS
PE
GND
E1
GND
5V

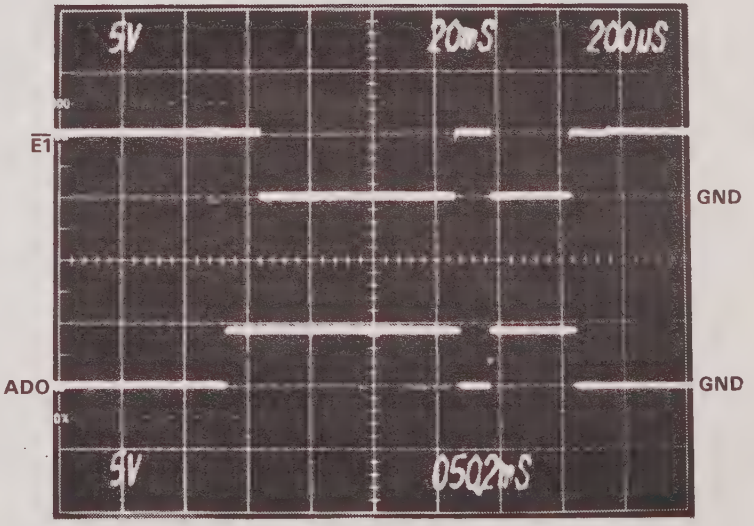
5


5V
20mS
200uS
PE
GND
E1
GND
5V
0502mS

6


5V
20mS
E1
GND
ADO
GND
5V

7

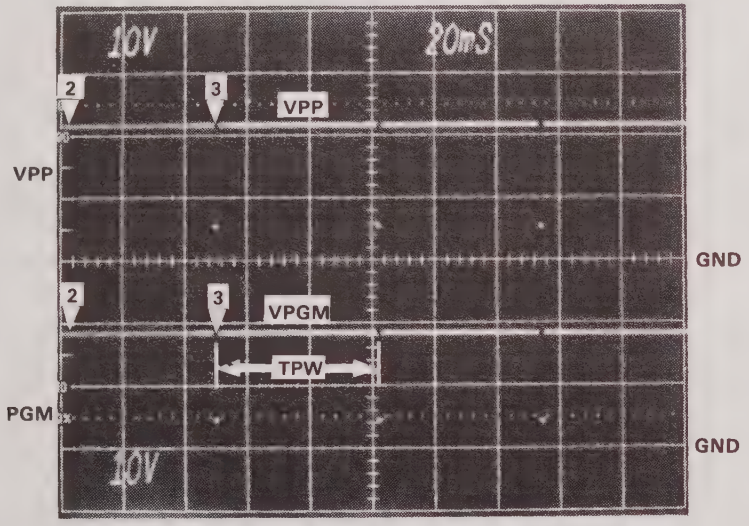

5V
20mS
200uS
E1
GND
ADO
GND
5V
0502mS

8

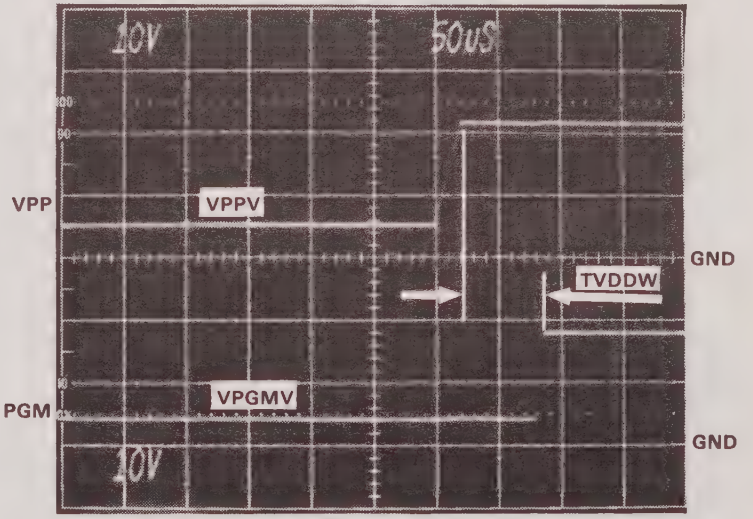
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		JH	5/23

DATA I/O

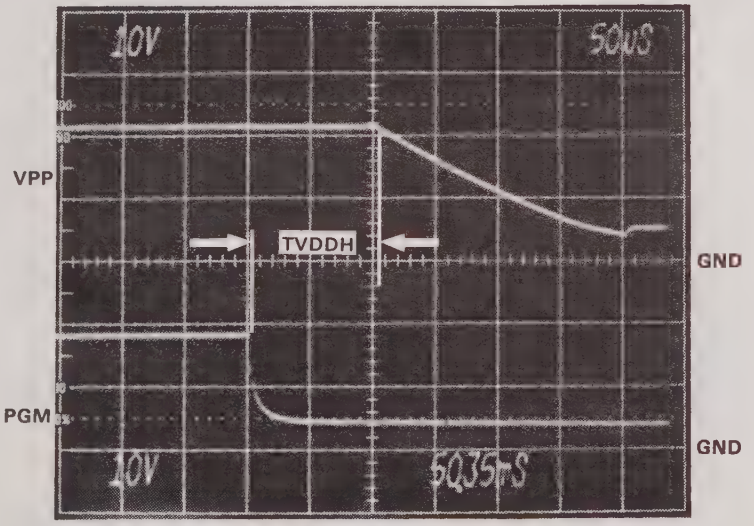
TITLE: TIMING DIAGRAM FAMILY CODES 47, 48		DRAWN BY:
		CHECKED BY: JH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2


10V
20mS
2
3
VPP
VPP
GND
2
3
VPGM
TPW
PGM
GND
10V

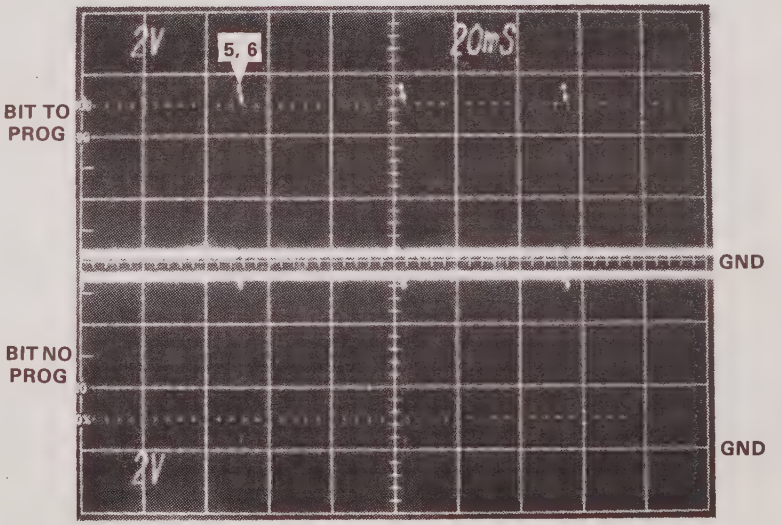
1


10V
50uS
VPP
VPPV
GND
TVDDW
PGM
VPGMV
GND
10V

2


10V
50uS
VPP
TVDDH
GND
PGM
GND
10V
5.035mS

3


2V
5, 6
20mS
BIT TO
PROG
GND
BIT NO
PROG
GND
2V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.9	5.0	5.1	V	Not shown
	VEA	17.5	18.0	18.5	V	Not shown
	VPP	20.5	21.0	21.5	V	
	VPPV	4.8	5.0	5.2	V	
	VPGM	17.5	18.0	18.5	V	
	VPGMV	4.0		5.1	V	
	TVDDW	0		1.0	ms	
	TVDDH	0		1.0	ms	
	TPW	50		60	ms	
	TWW	17			µs	See note 3
	TAW	17			µs	See note 3
	TWA	17			µs	See note 3
	Reject Overprogram		1 0		Pulse Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

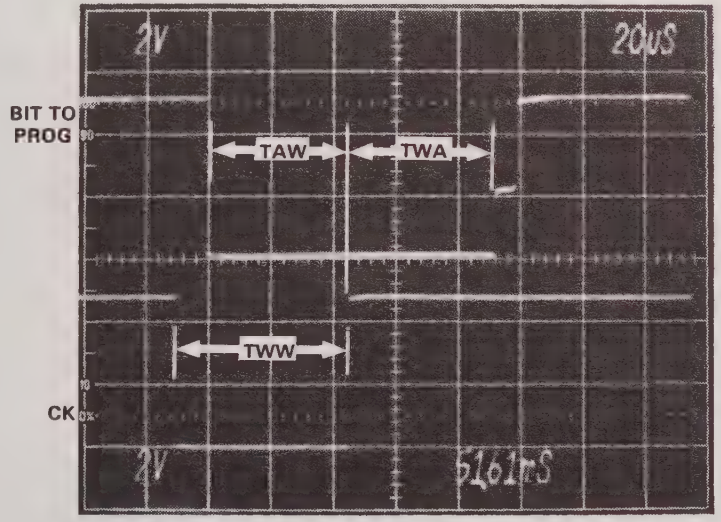
1. *Load RAM with hex FE for Family 49.*
2. *Load RAM with hex 01 for Family 50 and bit-to-prog waveform becomes bit-no-prog waveform and vice versa.*
3. *4TCY = 17 us @ 3.579545 MHz*

REVISIONS

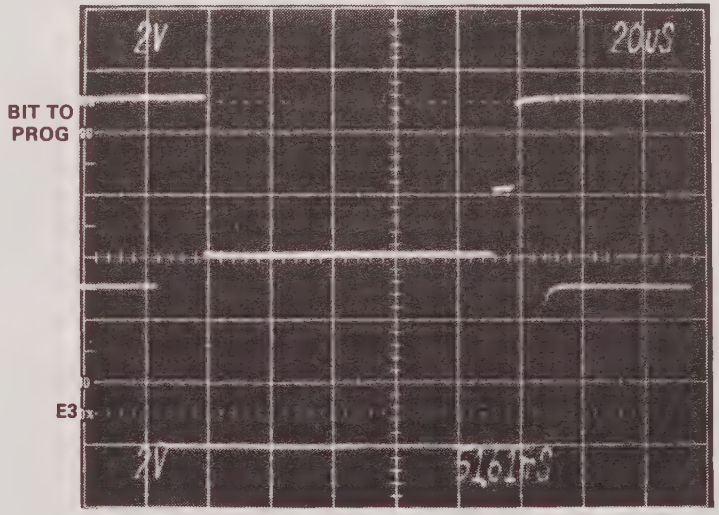
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		TH	5/85
		ECN #5023		CTB	3/87

DATA I/O

TITLE: TIMING DIAGRAM FAMILY CODES 49, 50		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 2


2V
20uS
BIT TO PROG
TAW
TWA
TWW
CK
2V
5161nS

5

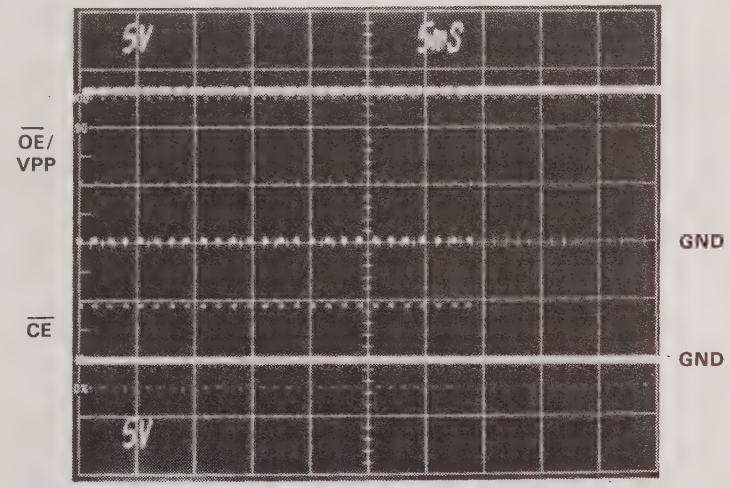

2V
20uS
BIT TO PROG
E3
2V
5161nS

6

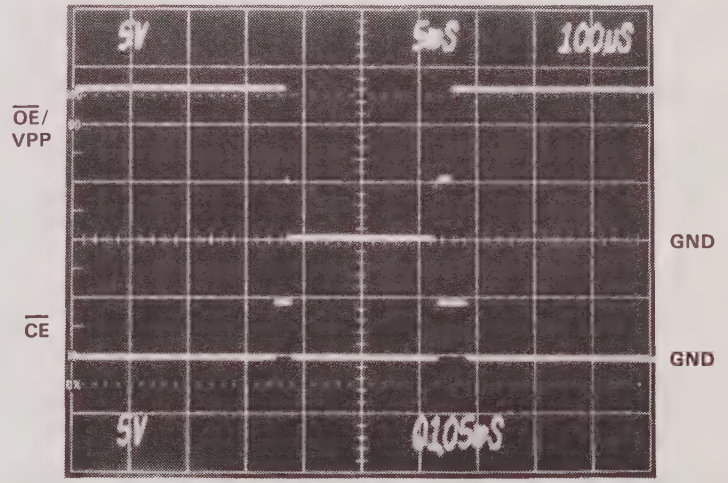
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831			

DATA I/O

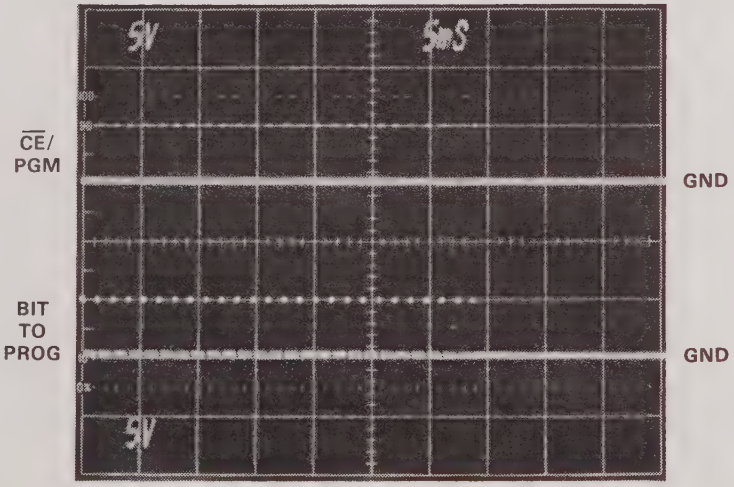
TITLE: TIMING DIAGRAM FAMILY CODES 49, 50		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2


5V
5mS
OE/
VPP
GND
CE
GND
5V

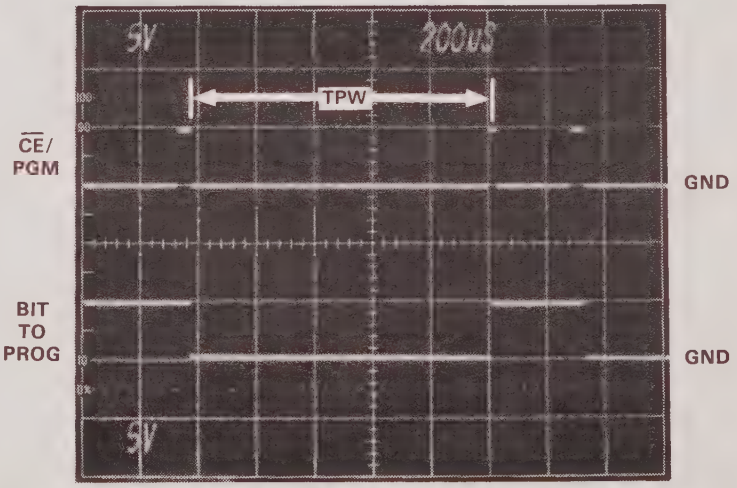
1


5V
5mS
100uS
OE/
VPP
GND
CE
GND
5V
0.05mS

2


5V
5mS
CE/
PGM
GND
BIT
TO
PROG
GND
5V

3


5V
200uS
TPW
CE/
PGM
GND
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.0	6.25	V	Not Shown
	VPP	12.0	12.5	13.0	V	
	TPW	0.95	1.0	1.05	ms	
	Reject		25		Pulses	
	Overprogram		1			See Note 3
1ST PASS	VCC	4.7	4.8	4.9	V	
VERIFY	VREF	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS	VCC	5.1	5.2	5.3	V	
VERIFY	VREF	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 4B.*
2. *Load RAM with hex 01 for Family 4C*
3. *The overprogram pulse is 3 ms times the number of programming pulses required to program the location.*

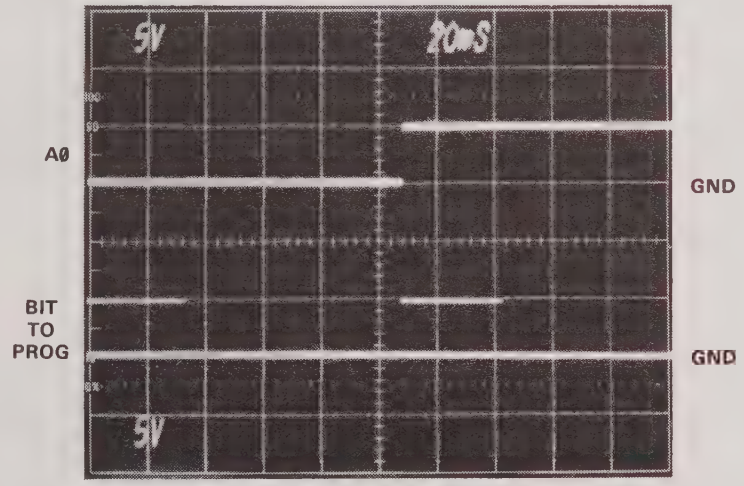
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

TIMING DIAGRAM

FAMILY CODES 4B, 4C

DATA I/O



5

B-105
981-0001

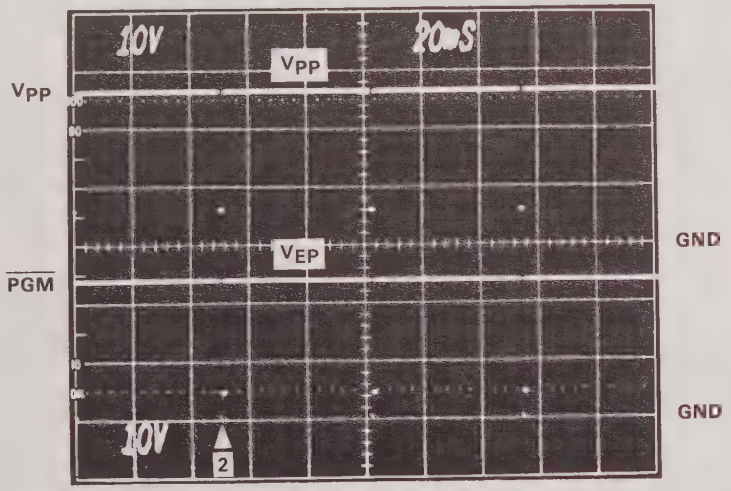
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

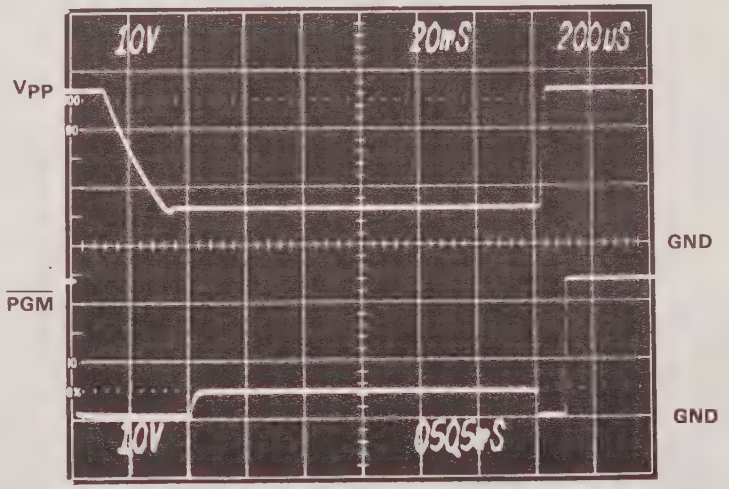
TIMING DIAGRAM

FAMILY CODES 4B, 4C

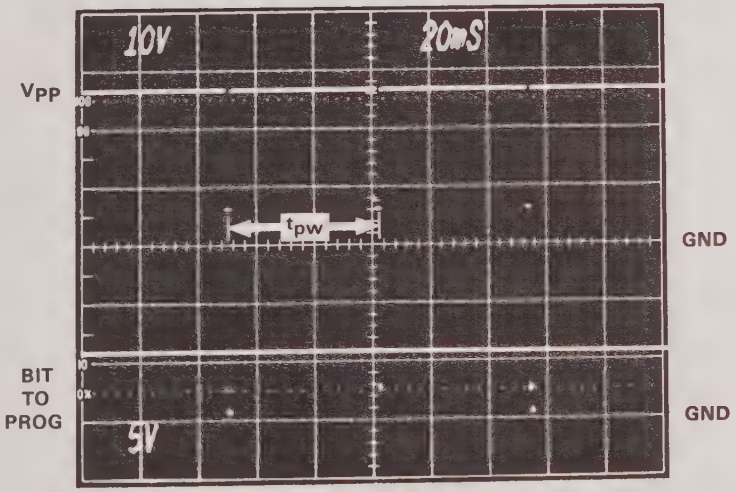
DATA I/O


10V
20mS
VPP
VPP
VEP
PGM
GND
GND
10V
2

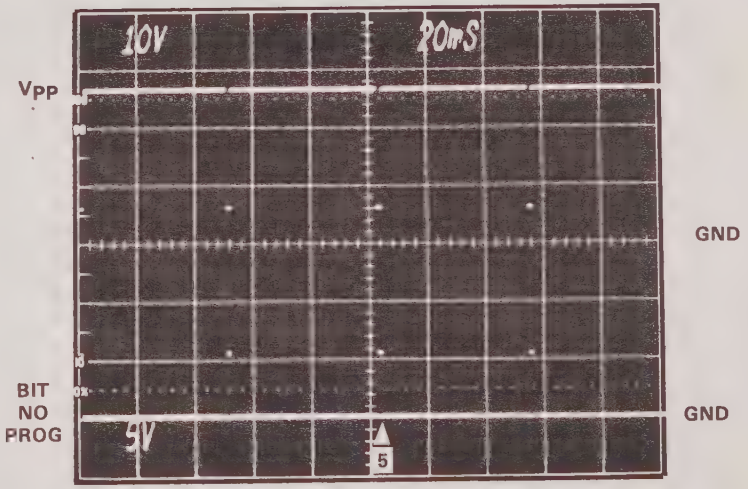
1


10V
20mS
200uS
VPP
PGM
GND
GND
10V
0505uS

2


10V
20mS
VPP
tpw
GND
BIT
TO
PROG
GND
5V

3


10V
20mS
VPP
GND
BIT
NO
PROG
GND
5V
5

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	24.0	25.0	26.0	V	
	V_{PPV}					N.A.
	V_{EP}	21.5	23	24.5	V	
	t_{pw}	49	50	51	ms	
	t_r					N.A.
	t_{ww}	20			μs	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		1		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 51.*
2. *Load RAM with hex 01 for Family 52.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CJB	3/84

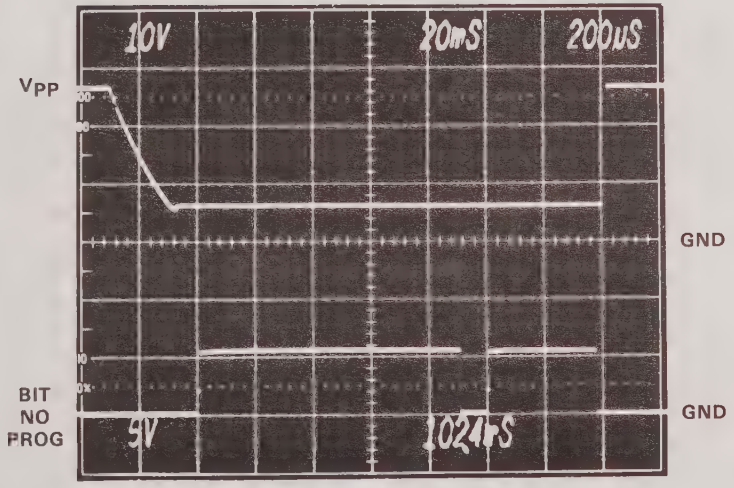
Sheet 1 of 3

TIMING DIAGRAM

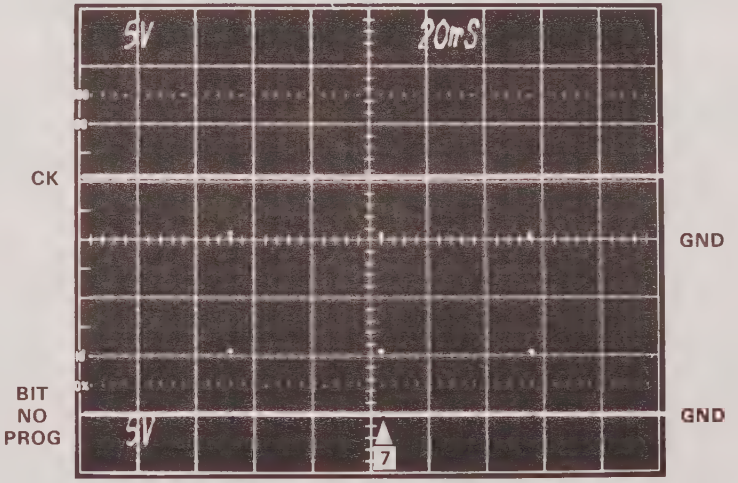
FAMILY CODES 51, 52

DATA I/O

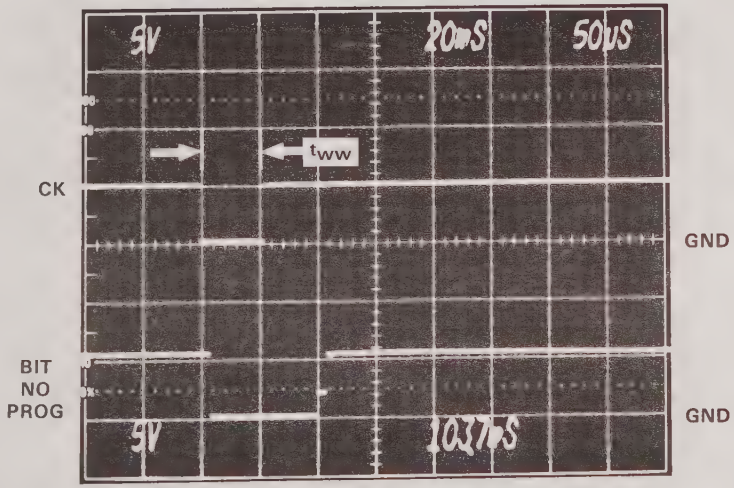
0526/1282


10V
20mS
200uS
VPP
GND
BIT
NO
PROG
GND
5V
1024mS

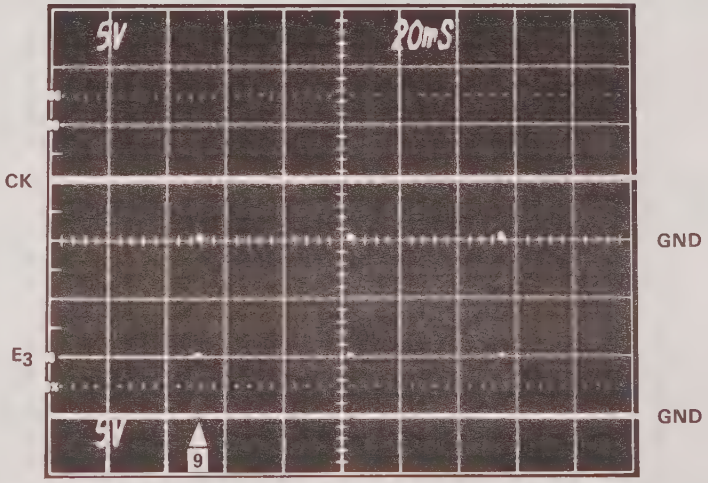
5


5V
20mS
CK
GND
BIT
NO
PROG
GND
5V
7

6


5V
20mS
50uS
tww
CK
GND
BIT
NO
PROG
GND
5V
1037mS

7


5V
20mS
CK
GND
E3
GND
5V
9

8

B-109
981-0001

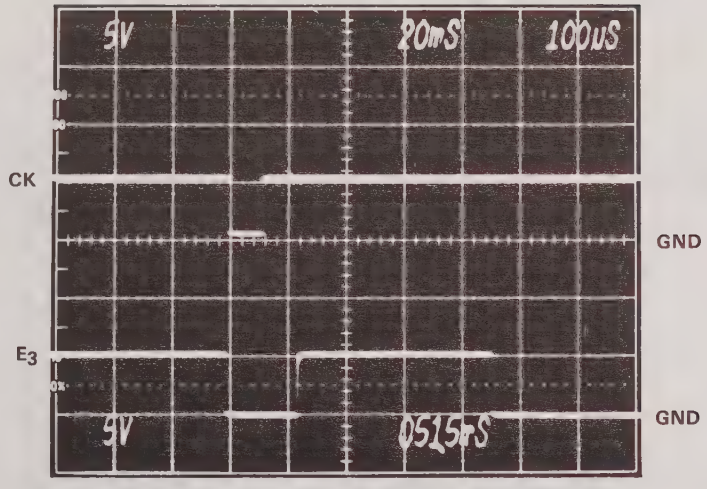
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

TIMING DIAGRAM

FAMILY CODES 51, 52

DATA I/O



9

B-111
981-0001

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	3/84

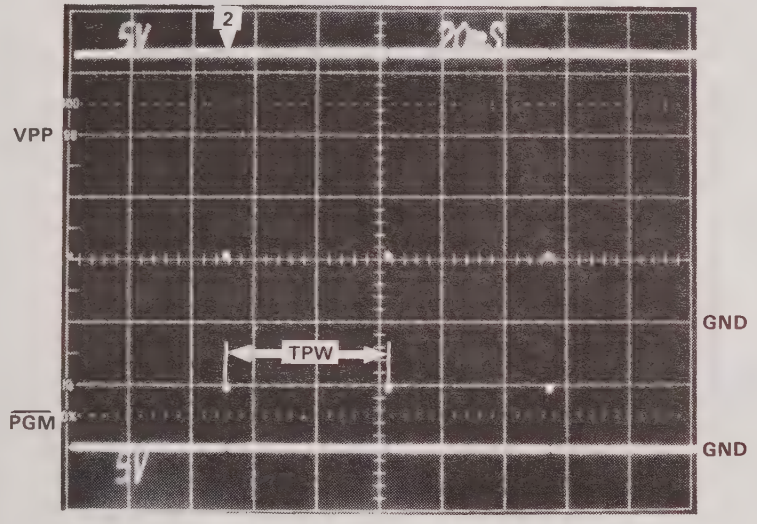
Sheet 3 of 3

TIMING DIAGRAM

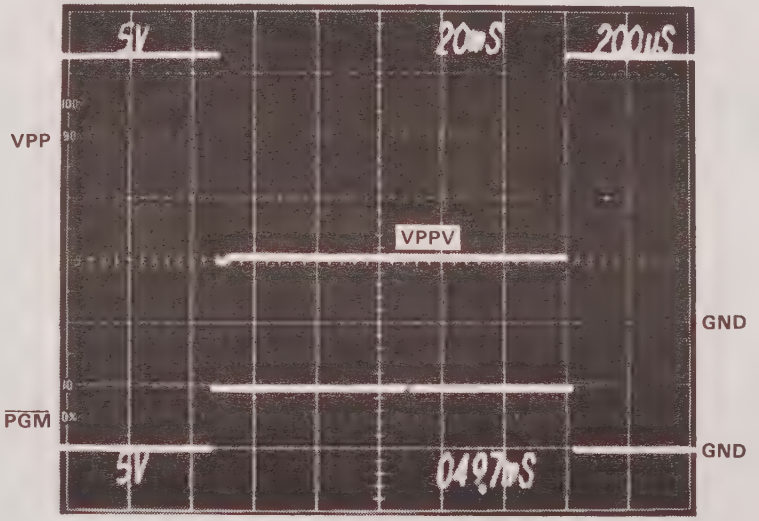
FAMILY CODES 51, 52

DATA I/O

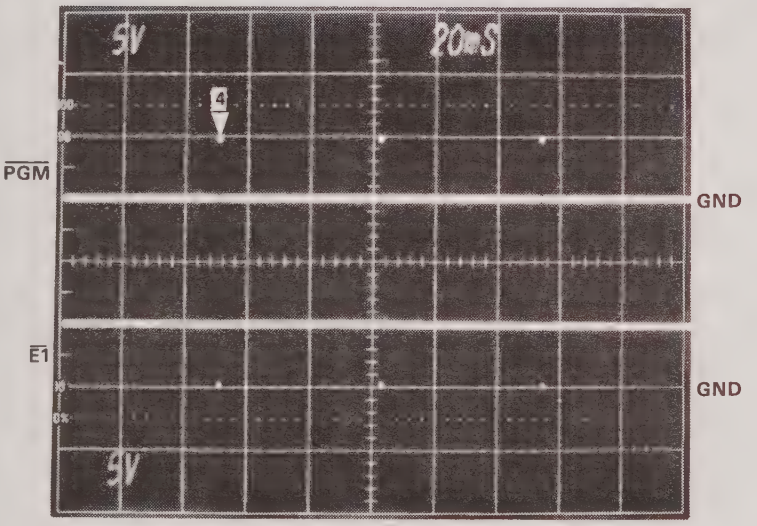
0526 1282


5V
2
20mS
VPP
GND
TPW
PGM
GND
5V

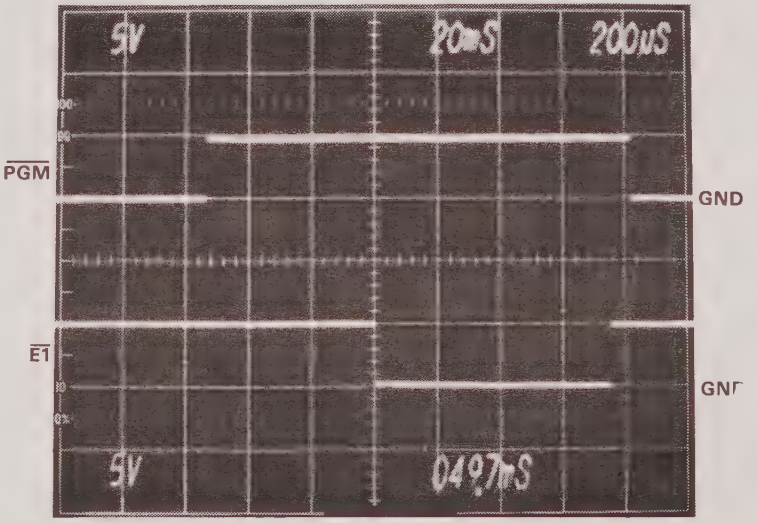
1


5V
20mS
200uS
VPP
VPPV
GND
PGM
GND
5V
049.7mS

2


5V
20mS
4
PGM
GND
E1
GND
5V

3


5V
20mS
200uS
PGM
GND
E1
GND
5V
049.7mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not shown
	VOP					NA
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	49.0	50.0	51.0	ms	
	TR					NA
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 53.*
2. *Load RAM with hex 01 for Family 54 and bit-to-prog waveform becomes bit-no-prog waveform.*

B-113
981-0001

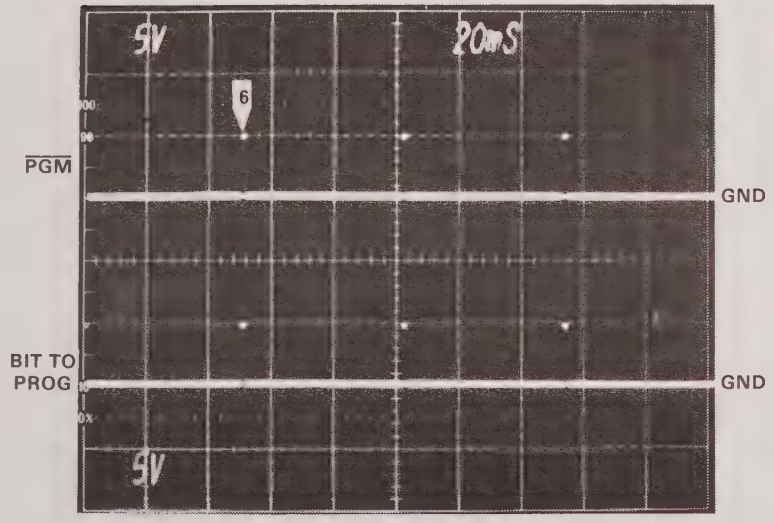
10-950-0059

REVISIONS

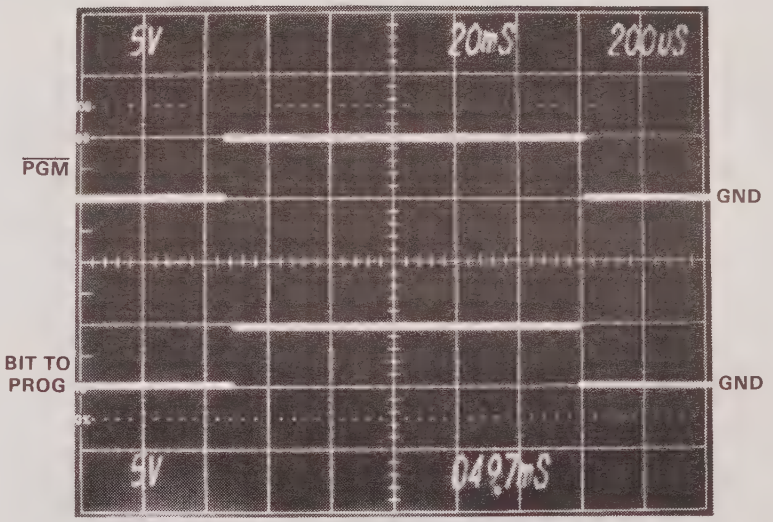
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		ZA	5/83
		ECN #5023		CJ3	3/84

DATA I/O

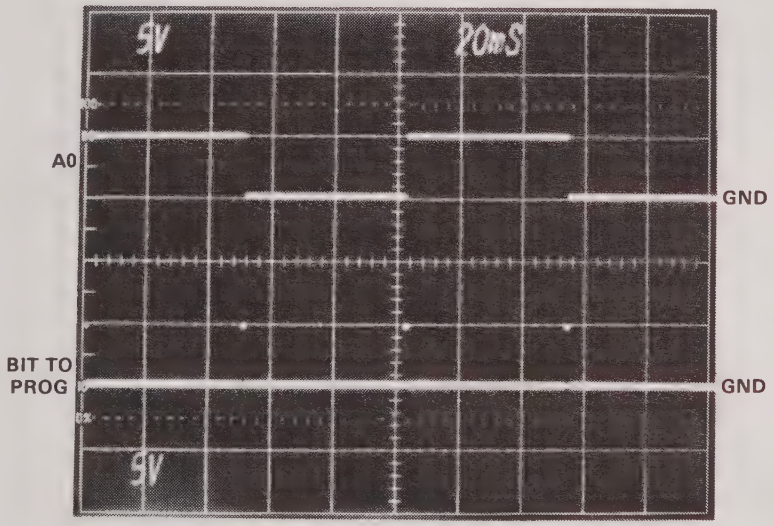
TITLE: TIMING DIAGRAM FAMILY CODES 53, 54		DRAWN BY:
		CHECKED BY: KA
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 2


5V
20mS
6
PGM
GND
BIT TO
PROG
GND
5V

5


5V
20mS
200uS
PGM
GND
BIT TO
PROG
GND
5V
0497mS

6

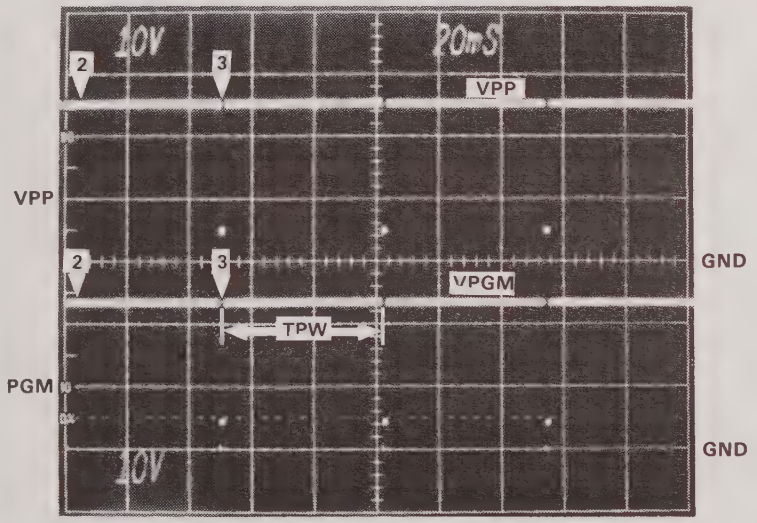

5V
20mS
A0
GND
BIT TO
PROG
GND
5V

7

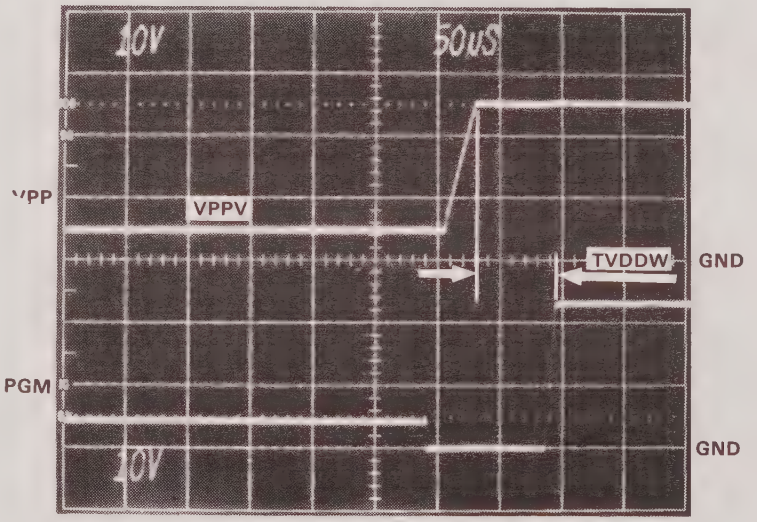
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		XH	5/83
		ECN #5023		CTZ	3/84

DATA I/O

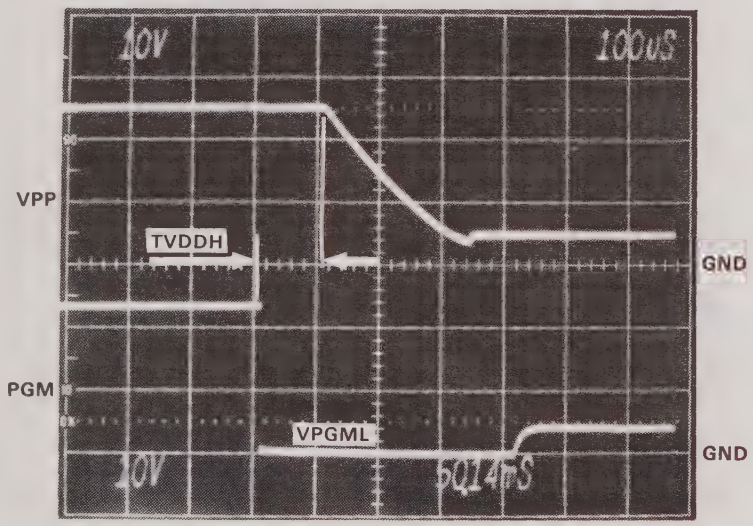
TITLE: TIMING DIAGRAM FAMILY CODES 53, 54		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2


10V
20mS
2
3
VPP
VPP
2
3
VPGM
GND
TPW
PGM
GND
10V

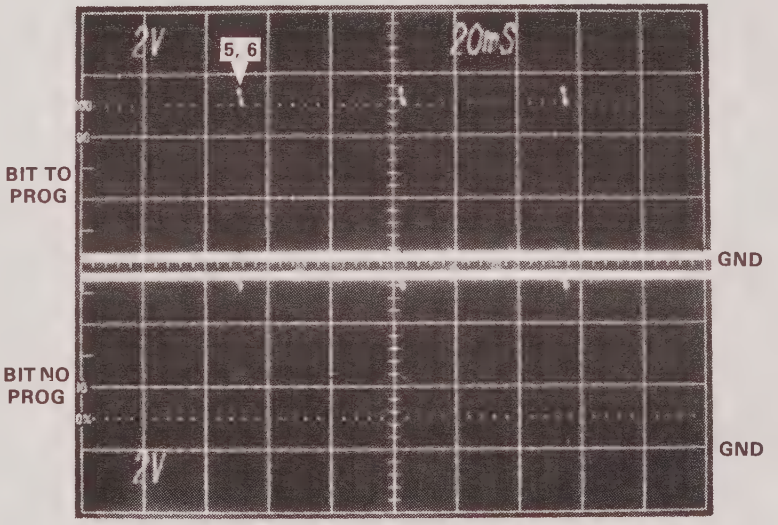
1


10V
50uS
VPP
VPPV
TVDDW
GND
PGM
GND
10V

2


10V
100uS
VPP
TVDDH
GND
PGM
VPGML
GND
10V
5014mS

3


2V
5, 6
20mS
BIT TO
PROG
GND
BIT NO
PROG
GND
2V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.9	5.0	5.1	V	Not shown
	VEA	21.5	23.0	24.5	V	Not shown
	VPP	24.0	25.0	26.0	V	
	VPPV	4.0	5.0	5.2	V	
	VPGM	21.5	23.0	24.5	V	
	VPGML		0	0.3	V	
	TVDDW	17			µs	See note 3
	TVDDH	0			µs	See note 3
	TPW	50		60	ms	
	TWW	17			µs	See note 3
	TAW	17			µs	See note 3
	TWA	17			µs	See note 3
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

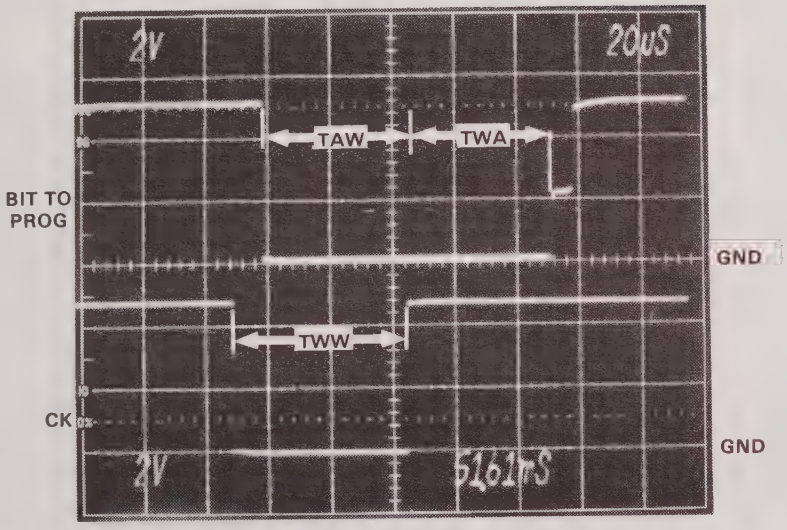
1. *Load RAM with hex FE for Family 55.*
2. *Load RAM with hex 01 for Family 56 and bit-to-prog waveform becomes bit-no-prog waveform and vice versa.*
3. *4TCY = 17 µs @ 3.579545 MHz*

REVISIONS

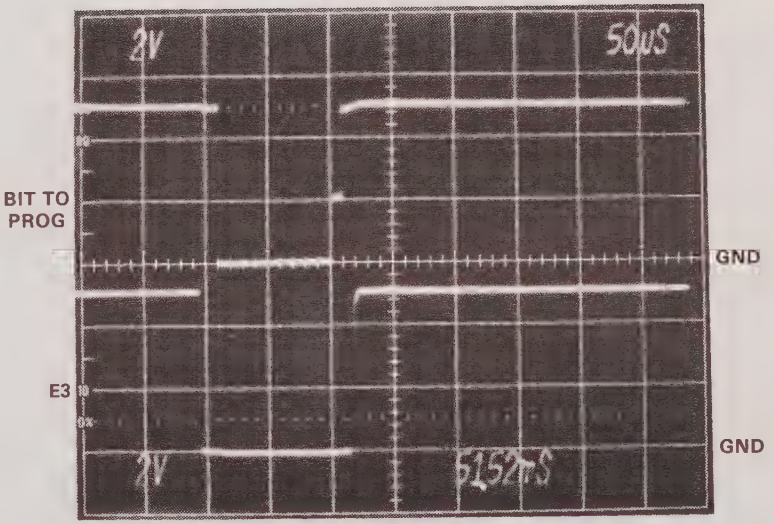
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		ZH	5/83
		ECN #5023		CTJ	3/84

DATA I/O

TITLE: TIMING DIAGRAM FAMILY CODES 55, 56		DRAWN BY:
		CHECKED BY: ZH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 2


2V
20uS
TAW
TWA
BIT TO PROG
GND
TWW
CK
GND
2V
5161nS

5


2V
50uS
BIT TO PROG
GND
E3
GND
2V
5152nS

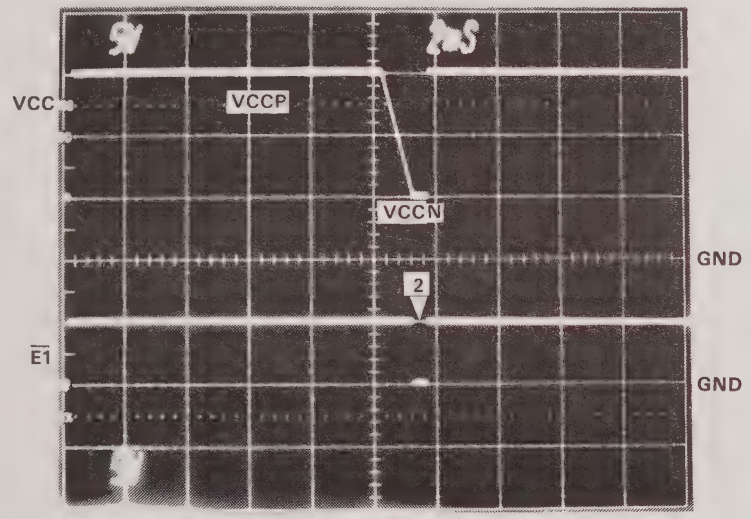
6

B-119
981-0001

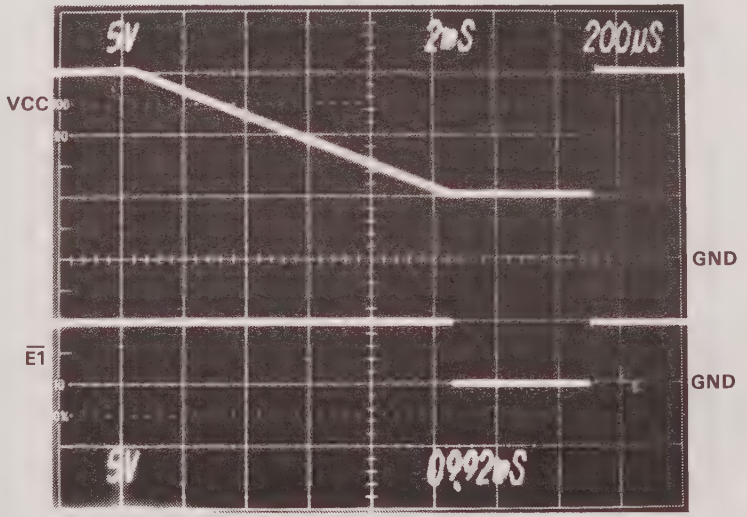
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		XX	5/83

DATA I/O

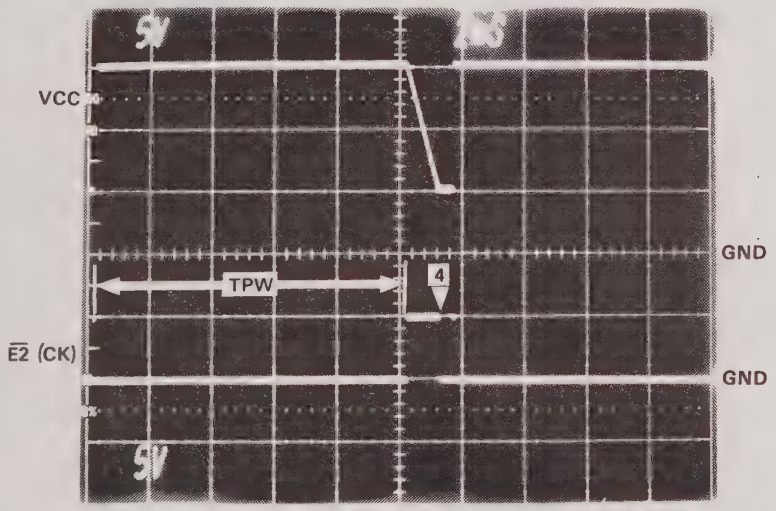
TITLE: TIMING DIAGRAM FAMILY CODES 55, 56		DRAWN BY:
		CHECKED BY: XX
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2


5V
2mS
VCC
VCCP
VCCN
GND
2
E1
GND
5V

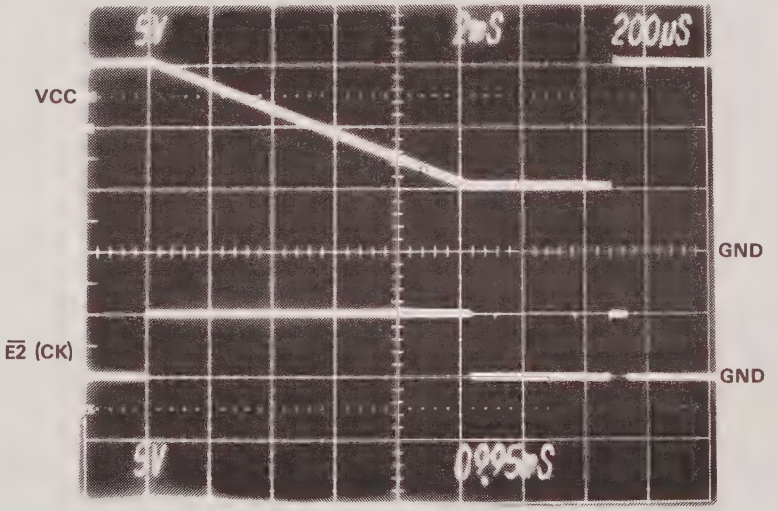
1


5V
2mS
200uS
VCC
GND
E1
GND
5V
0.992mS

2


5V
VCC
GND
TPW
4
E2 (CK)
GND
5V

3


5V
2mS
200uS
VCC
GND
E2 (CK)
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	14.0	15.0	16.0	V	
	VCCN	4.0	5.0	6.0	V	
	TPW	9.8	10.0	10.2	ms	
	TR					NA
	TF					NA
	Reject		2		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 57, and bit-no-prog waveform becomes bit-to-prog waveform.*
2. *Load RAM with hex 01 for Family 58.*
3. *Photos 7 and 8 are erase waveforms.*
4. *On the E2(CK) pin, one or two clock pulses may be seen, depending on which pulse location is observed.*
5. *Photo 5 is for Family 58. For Family 57, it is bit-to-prog.*

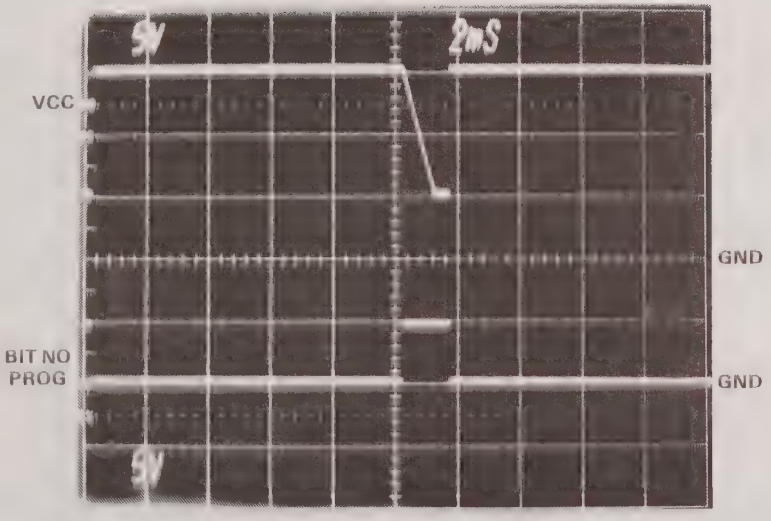
B-121
981-0001

REVISIONS

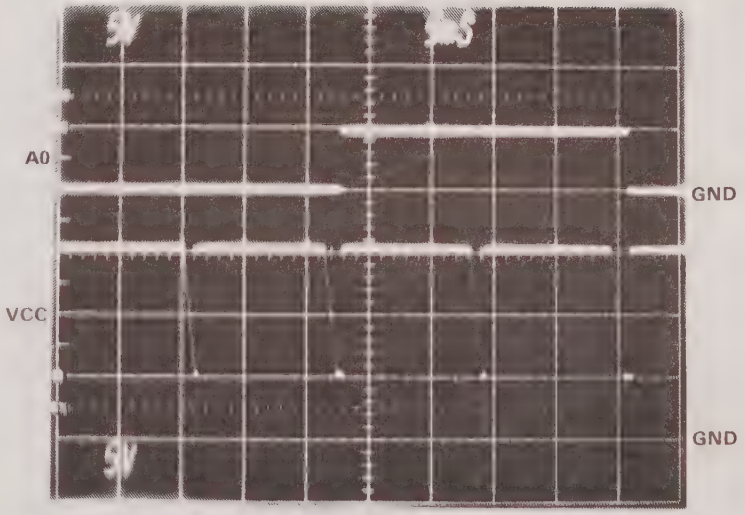
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		XH	7/23
		ECN #5023		C73	3/84

DATA I/O

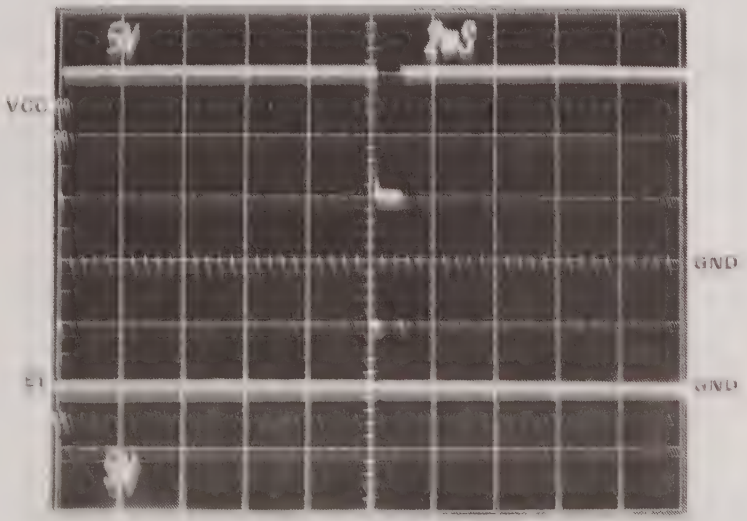
TITLE: TIMING DIAGRAM — FAMILY CODES 57, 58	DRAWN BY:	CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 2


5V
2mS
VCC
GND
BIT NO
PROG
GND
5V

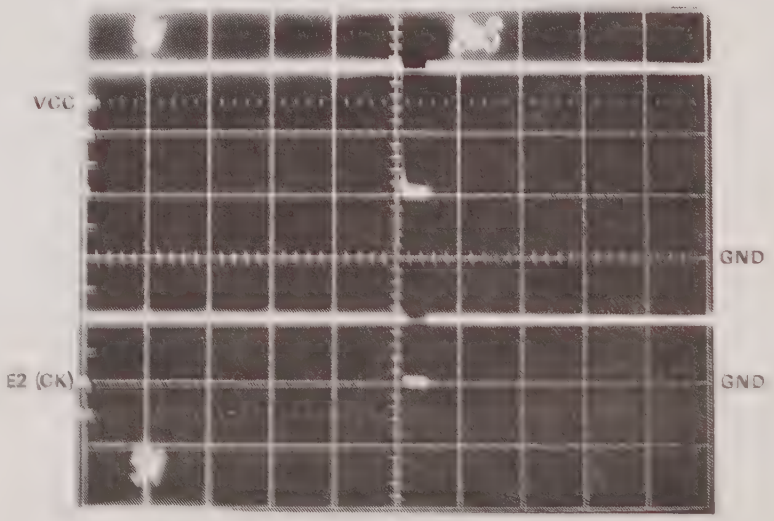
5


5V
A0
GND
VCC
GND
5V

6


5V
2mS
VCC
GND
E1
GND
5V

7


VCC
GND
E2 (CK)
GND

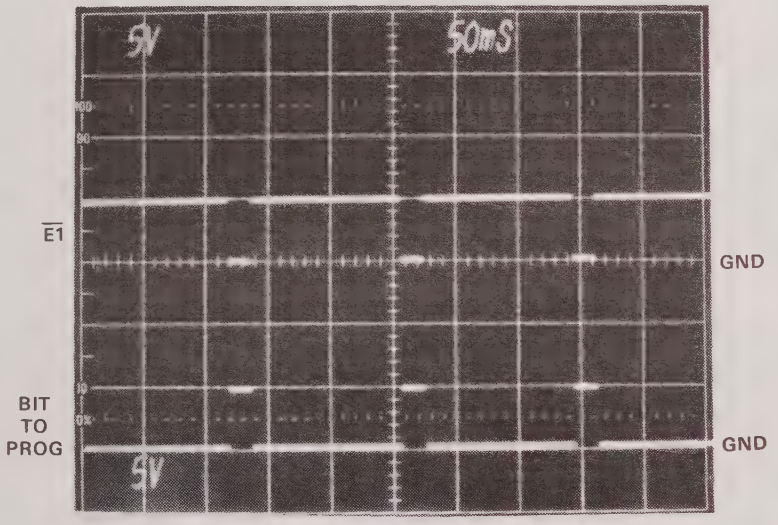
8

B-123
981-0001

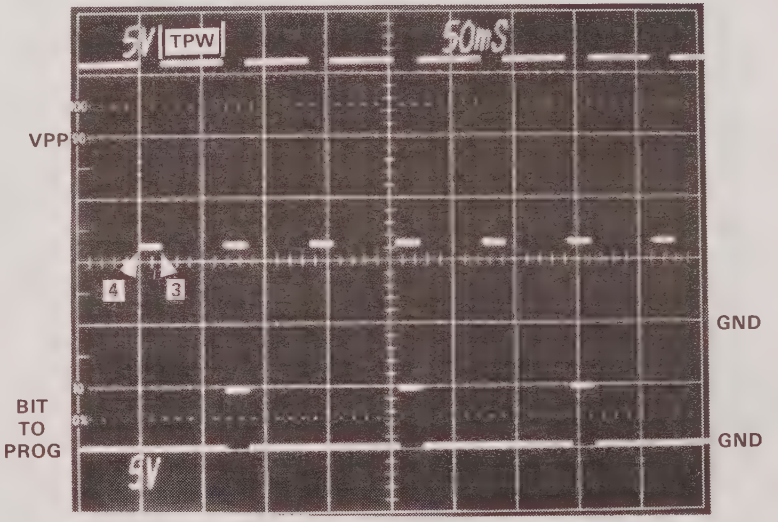
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		[illegible]	[illegible]

DATA I/O

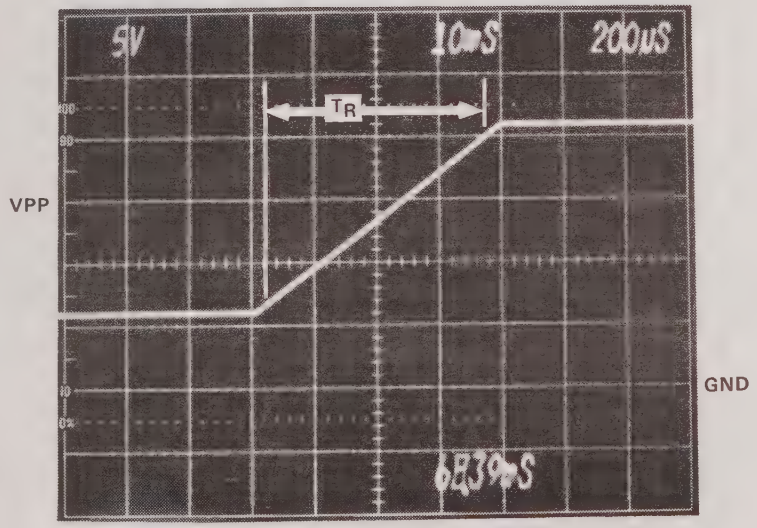
TITLE: TIMING DIAGRAM FAMILY CODES 57, 58			DRAWN BY:
			CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059	
SCALE			SHEET 2 of 2


5V
50mS
$\overline{E1}$
GND
BIT
TO
PROG
GND
5V

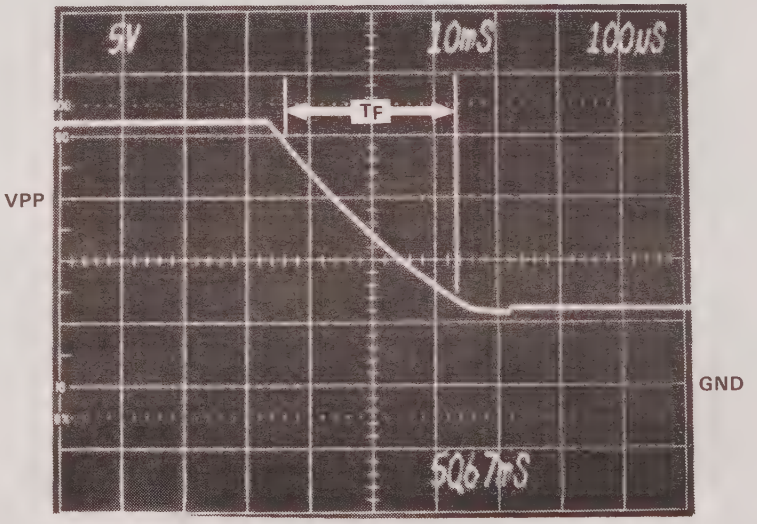
1


5V
TPW
50mS
VPP
4
3
GND
BIT
TO
PROG
GND
5V

2


5V
10mS
200uS
VPP
T_R
GND
6839mS

3


5V
10mS
100uS
VPP
T_F
GND
5067mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.5	5.8	6.1	V	Not Shown
	VPP	20.0	20.5	21.0	V	
	VPPN	5.7	5.9	6.1	V	
	TPW	45	50	55	ms	
	T_R	50			µs	
	T_F	50			µs	
	Reject		4		Pulses	See note 3
	Overprogram		1		Pulses	See note 3
1ST PASS VERIFY	VCC	4.8	4.9	5.0	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	16.4	17.4	18.4	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	3.4	3.5	3.6	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	19.1	20.1	21.1	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 59.*
2. *Load RAM with hex 01 for Family 60, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Pulse 2 of the 4-pulse string is actually an overprogram pulse.*

B-125
981-0001

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		JH	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 59, 60

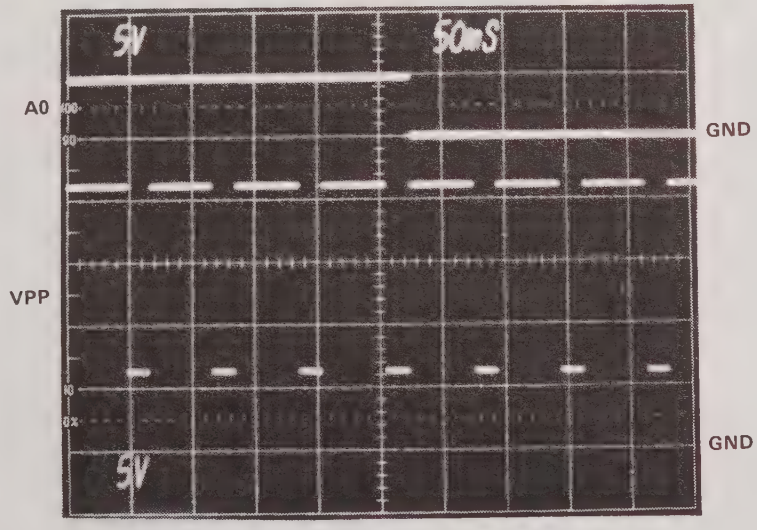
DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 1/2

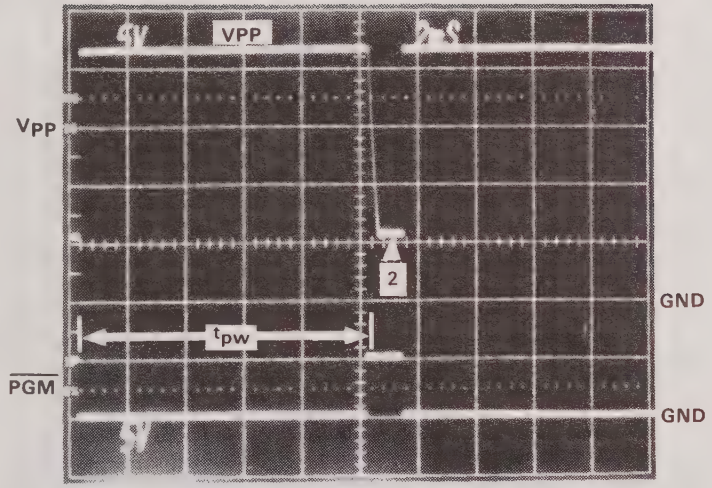


5

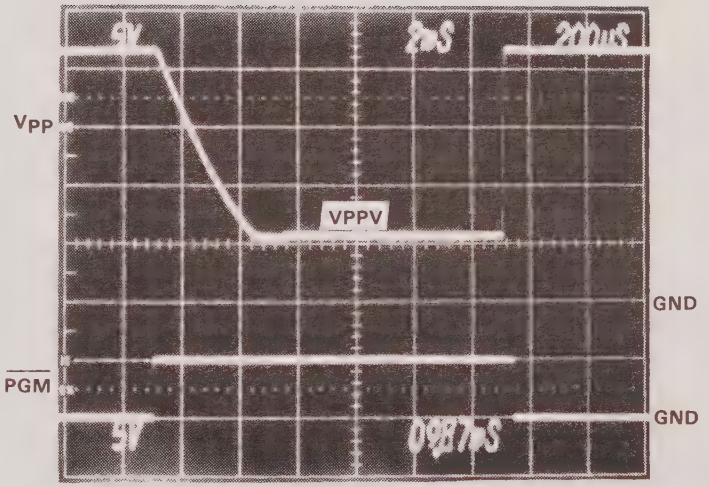
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJG	11/82
		ECN #4831		JH	5/83

DATA I/O ISSAQUAH, WA

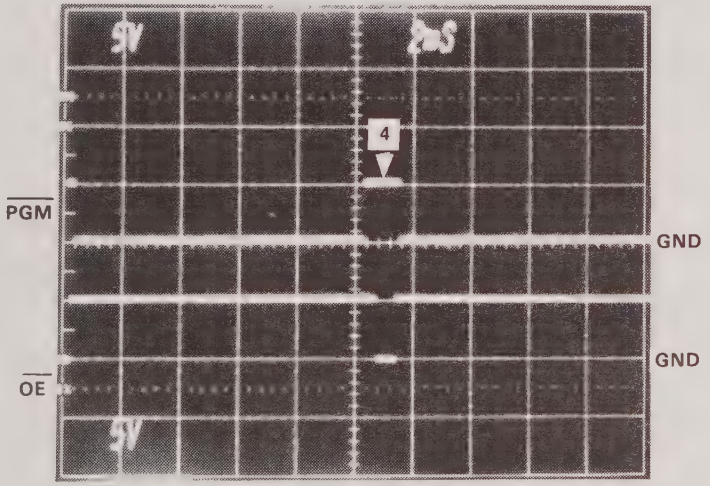
TITLE: TIMING DIAGRAM FAMILY CODES 59, 60		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2


5V
VPP
2mS
VPP
2
GND
tpw
PGM
GND
5V

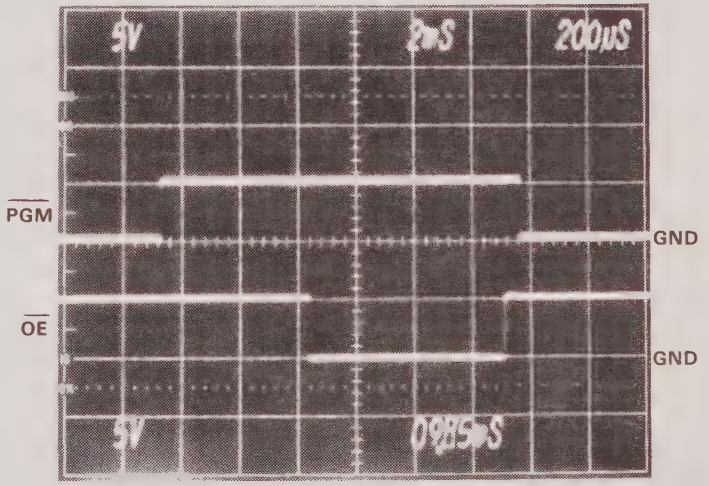
1


5V
2mS
200uS
VPP
VPPV
GND
PGM
GND
5V
098.7mS

2


5V
2mS
4
PGM
GND
OE
GND
5V

3


5V
2mS
200uS
PGM
GND
OE
GND
5V
098.5mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	20.5	21.0	21.5	V	
	V_{PPV}	4.75	5.0	5.25	V	
	t_{pw}	9.5	10.0	10.5	ms	
	t_r					N.A.
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 63.*
2. *Photos 7 and 8 are for Pinout 24.*

REVISIONS

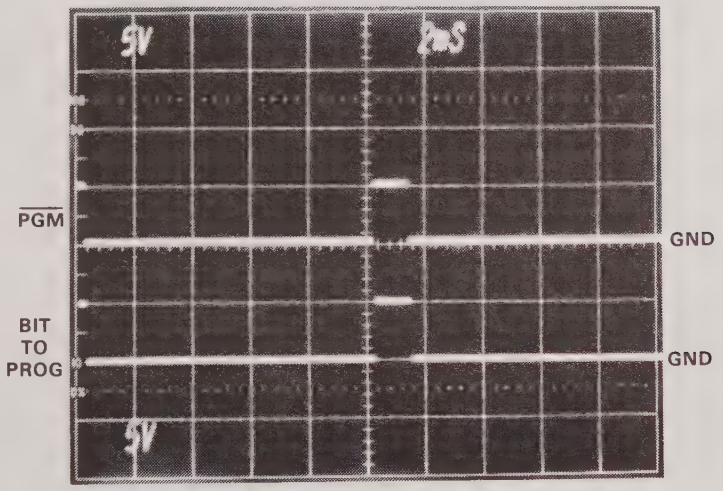
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	3/84

Sheet 1 of 2

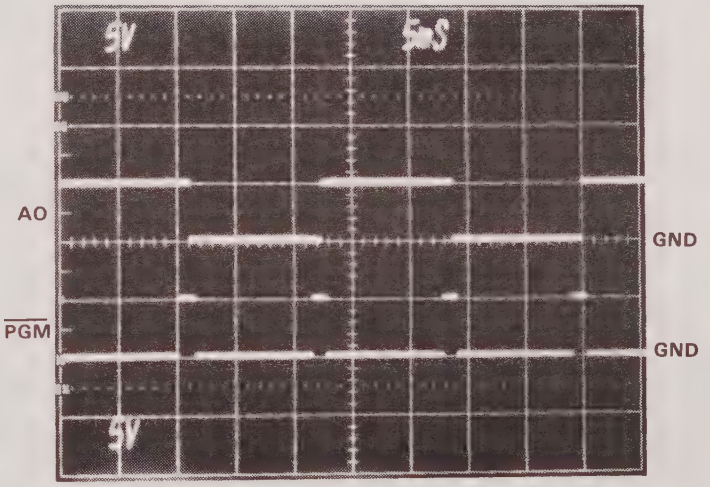
TIMING DIAGRAM

FAMILY CODES 63, 64

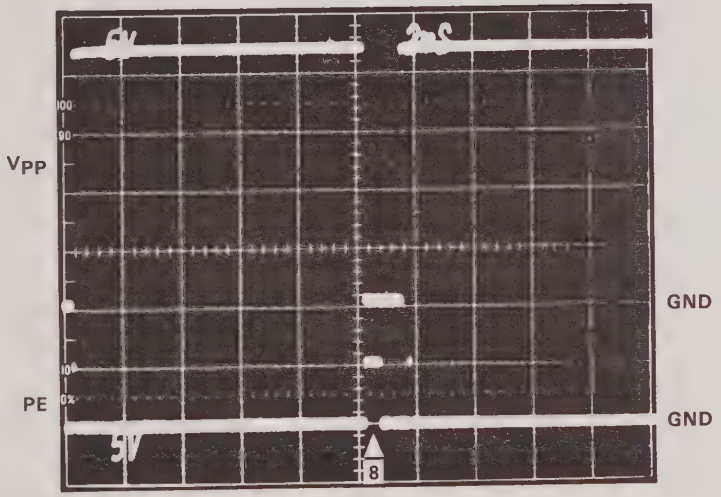
DATA I/O


5V
2mS
PGM
GND
BIT
TO
PROG
GND
5V

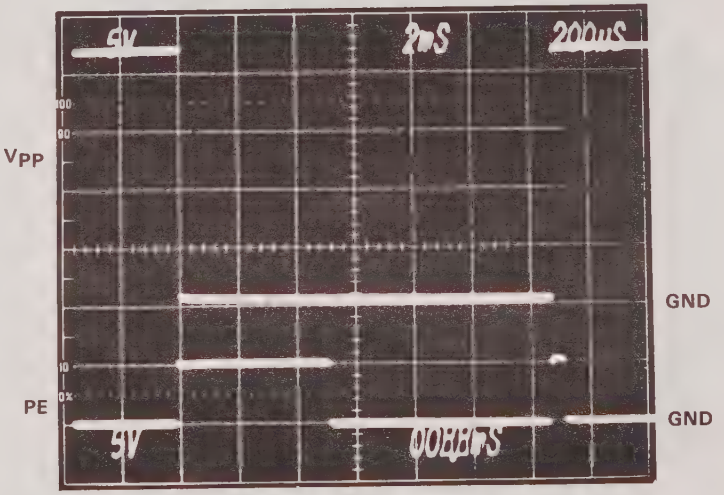
5


5V
5mS
AO
GND
PGM
GND
5V

6


5V
2mS
VPP
GND
PE
GND
5V
8

7


5V
2mS
200mS
VPP
GND
PE
GND
5V

8

B-131
981-0001

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	3/84

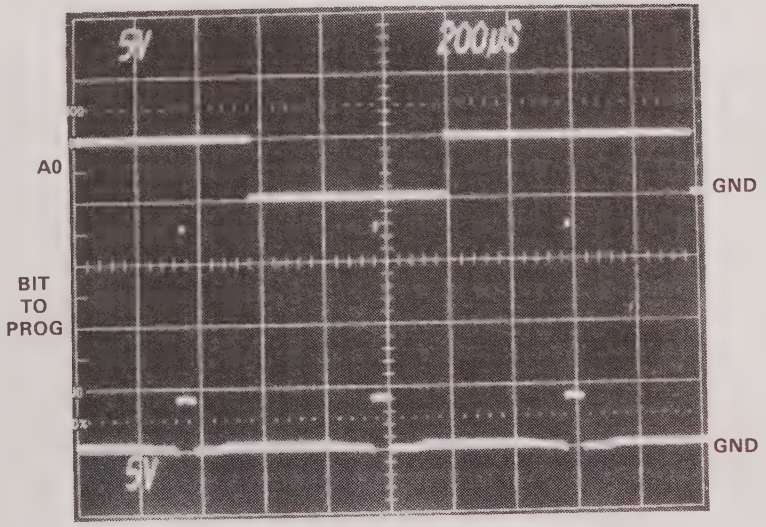
Sheet 2 of 2

TIMING DIAGRAM

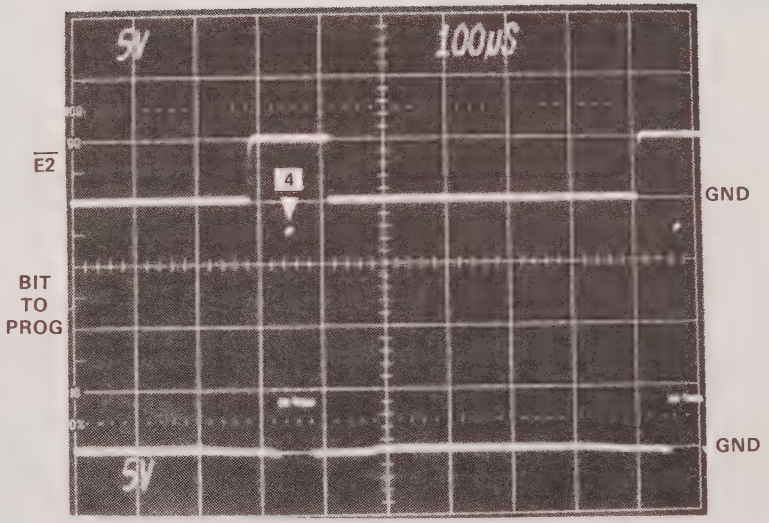
FAMILY CODES 63, 64

DATA I/O

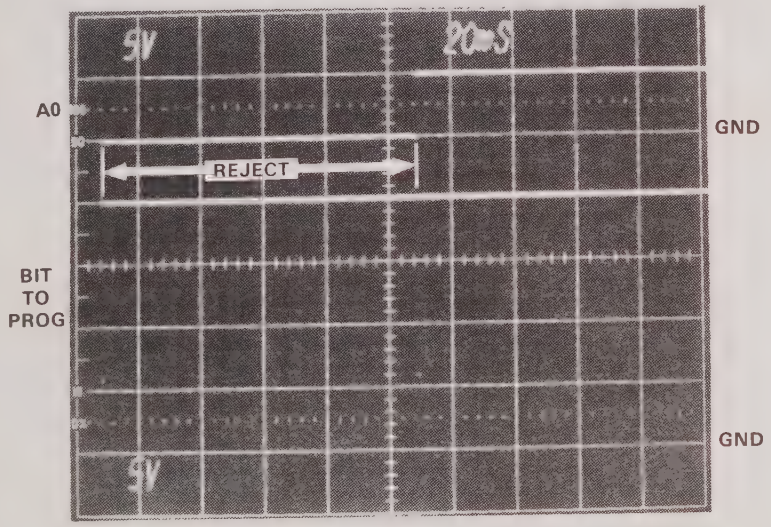
0526/1282


5V
200µS
A0
GND
BIT
TO
PROG
GND
5V

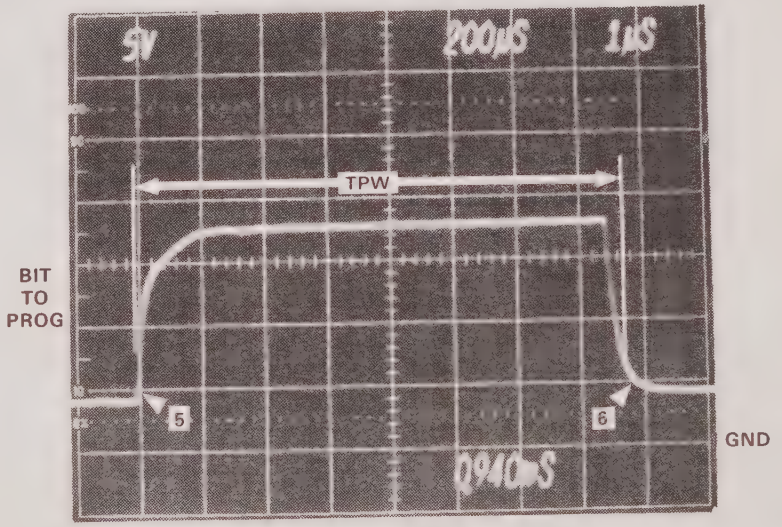
1


5V
100µS
E2
4
GND
BIT
TO
PROG
GND
5V

2


5V
20mS
A0
GND
REJECT
BIT
TO
PROG
GND
5V

3


5V
200µS
1µS
TPW
BIT
TO
PROG
5
6
GND
0940mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VOP	19.0	19.5	20.0	V	
	TPW	7.1	7.5	7.9	µs	See Note 3
	TR	0.16		1.1	µs	
	TF	0.16		1.1	µs	
	Overprogram		1		Pulses	
	Reject		10,000		Pulses	See Note 4
	Duty Cycle	70			%	
1ST PASS VERIFY	VCC	4.5	4.6	4.7	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	25.5	26.0	26.5	V	701-1655/TP4
	Low Load	25.5	26.0	26.5	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.5	6.6	6.7	V	
	VREF	4.4	4.5	4.6	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	6.7	7.2	7.7	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 65.*
2. *Load RAM with hex 01 for Family 66.*
3. *Measurement taken at 9V point of 01 with a 200 Ω load.*
4. *10,000 pulses equals 100 ms, as shown in photo 3.*
5. *Do not use a wirewound load resistor.*
6. *01 loaded with a 200Ω, 2-watt resistor for photos 1, 2, 4-6.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		24	5/23
		ECN #5023		CTB	3/84

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
FAMILY CODES 65, 66

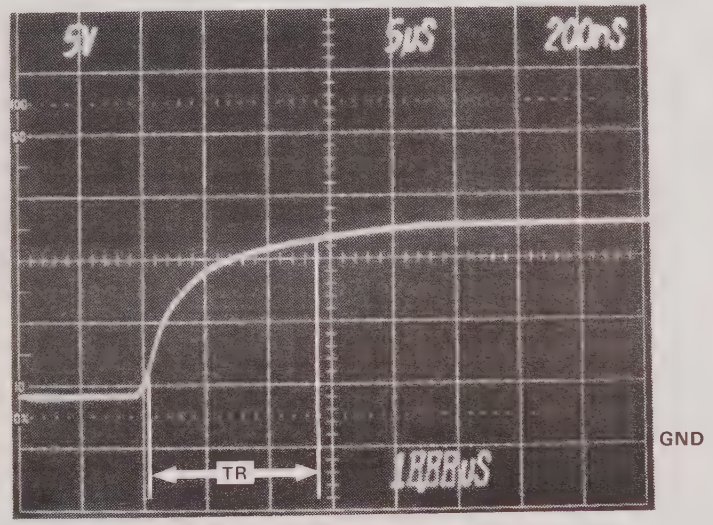
DRAWN BY: PAP

CHECKED BY: ZA

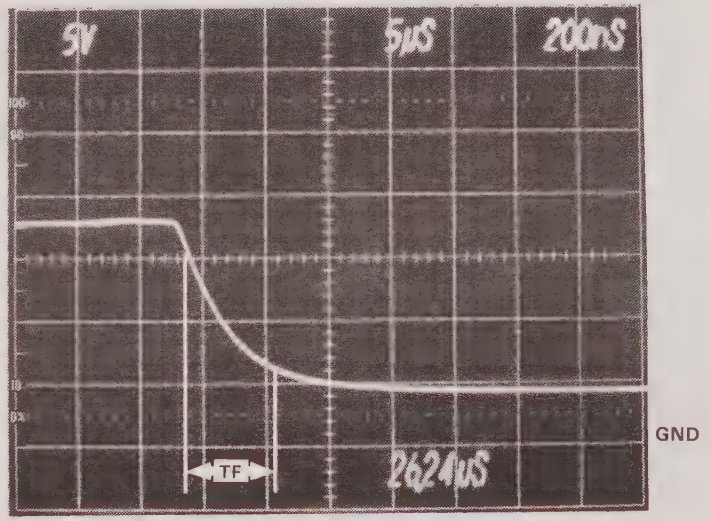
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 1/2


5V
5µS
200nS
BIT
TO
PROG
GND
TR
1.88µS

5

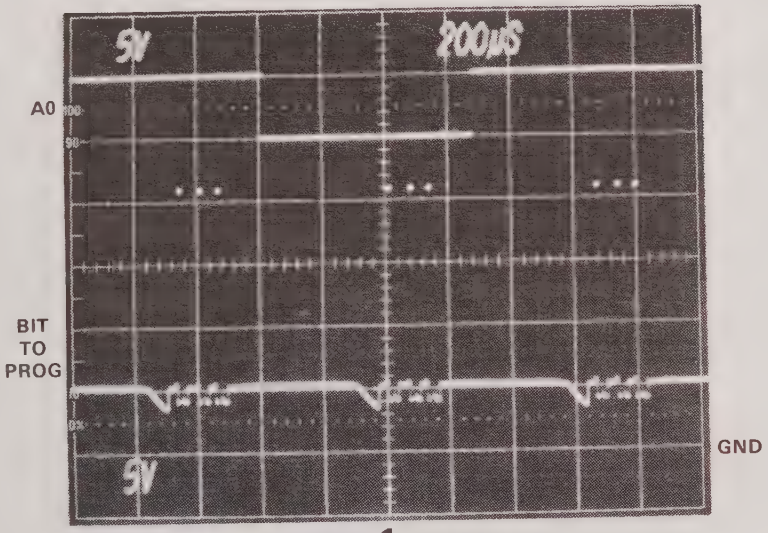

5V
5µS
200nS
GND
TF
2624nS

6

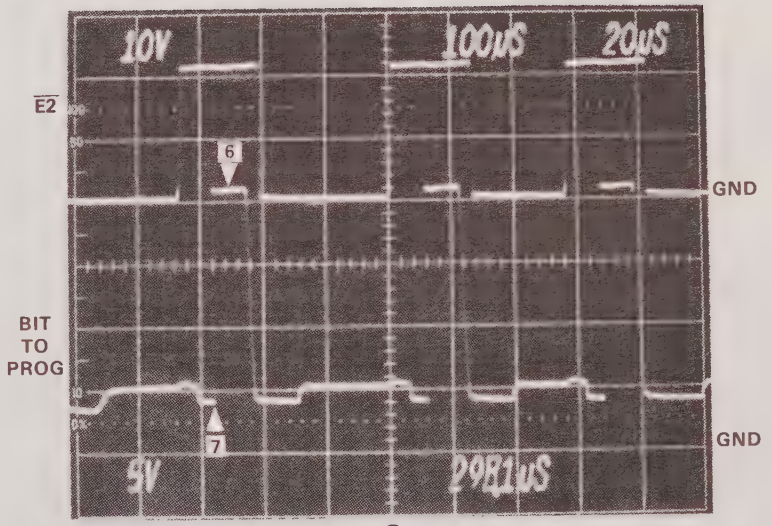
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		XH	5/8

DATA I/O ISSAQUAH, WA

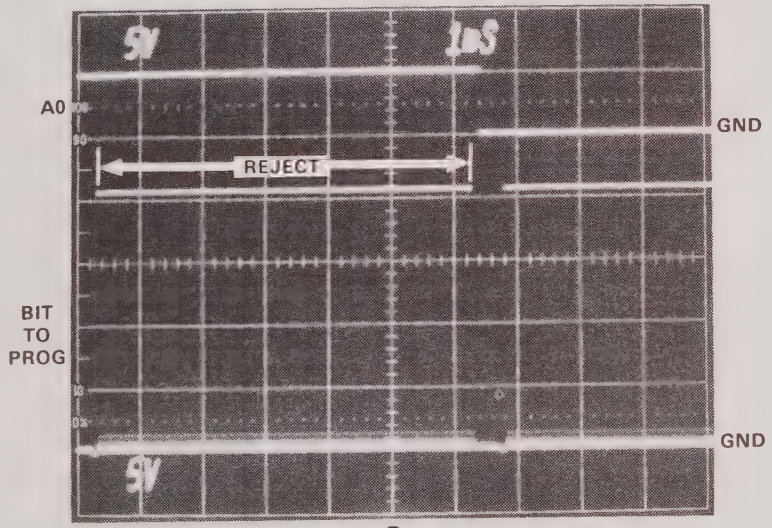
TITLE: TIMING DIAGRAM FAMILY CODES 65, 66			DRAWN BY: PAP
			CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059	
SCALE			SHEET 2/2


5V
200uS
A0
BIT
TO
PROG
GND
5V

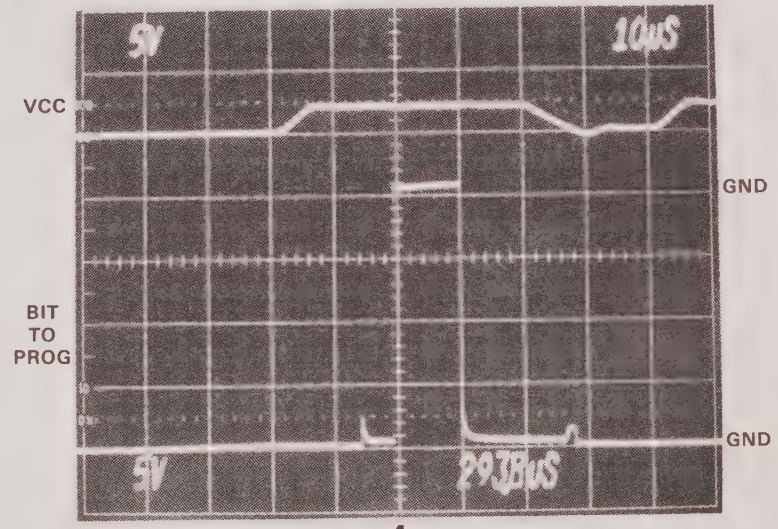
1


10V
100uS
20uS
E2
6
GND
BIT
TO
PROG
7
GND
5V
29.81uS

2


5V
1mS
A0
GND
REJECT
BIT
TO
PROG
GND
5V

3


5V
10uS
VCC
GND
BIT
TO
PROG
GND
5V
29.18uS

4

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	6.7	7.0	7.5	V	
	VPP	20.0	20.0	22.0	V	
	VOP	20.0	20.0	22.0	V	
	TPW	10.0	11.0	12.0	µs	See Note 3
	TR			2.0	µs	
	TF			2.0	µs	
	Overprogram		2		Pulses	
	Reject		100		Pulses	See Note 4
	Duty Cycle	15	20	25	%	
1ST PASS VERIFY	VCC	4.0	4.1	4.2	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	25.0	26.0	27.0	V	701-1655/TP4
	Low Load	25.0	26.0	27.0	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.9	7.0	7.1	V	
	VREF	3.9	4.0	4.1	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	5.6	6.6	7.6	V	701-1655/TP3

1. *Load RAM with hex FE for Family 67.*
2. *Load RAM with hex 01 for Family 68.*
3. *Measurement taken at 15V point of 01 with a 200 Ω load.*
4. *100 pulses equals 6 ms, as shown in photo 3.*
5. *V_{CC} loaded with a 330 Ω resistor, as shown in photo 5.*
6. *Do not use a wirewound load resistor.*
7. *01 is loaded with a 200 Ω resistor, as shown in photos 3-7.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		CJ	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 67, 68

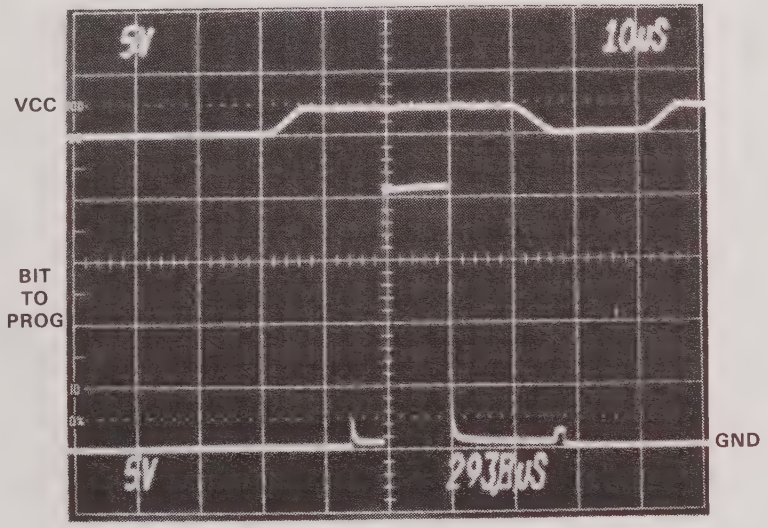
DRAWN BY: BG / PP

CHECKED BY:

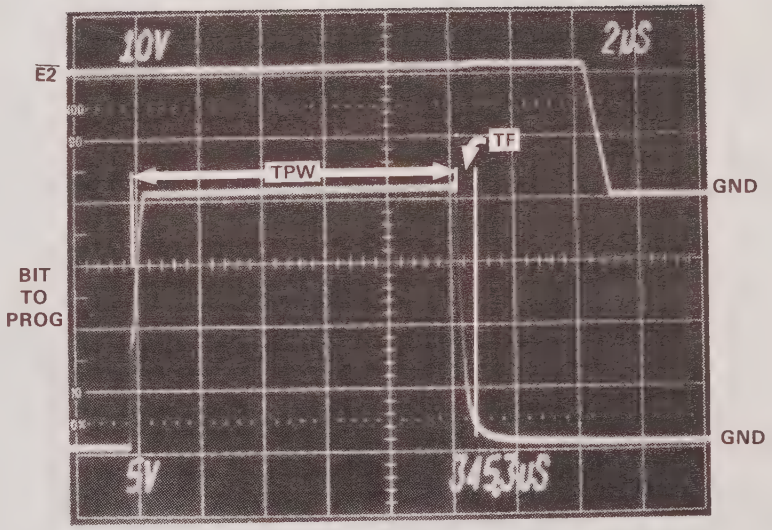
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

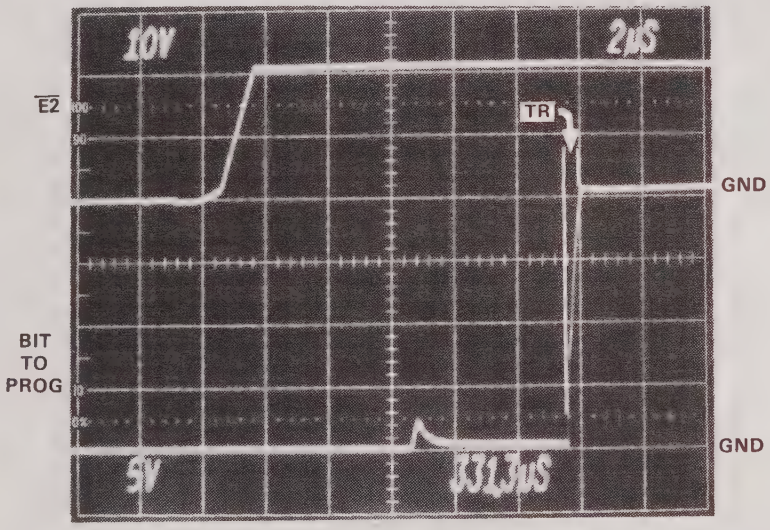
SHEET 1/2


5V
10uS
VCC
BIT
TO
PROG
GND
5V
293uS

5


10V
2uS
E2
TF
TPW
GND
BIT
TO
PROG
GND
5V
345uS

6

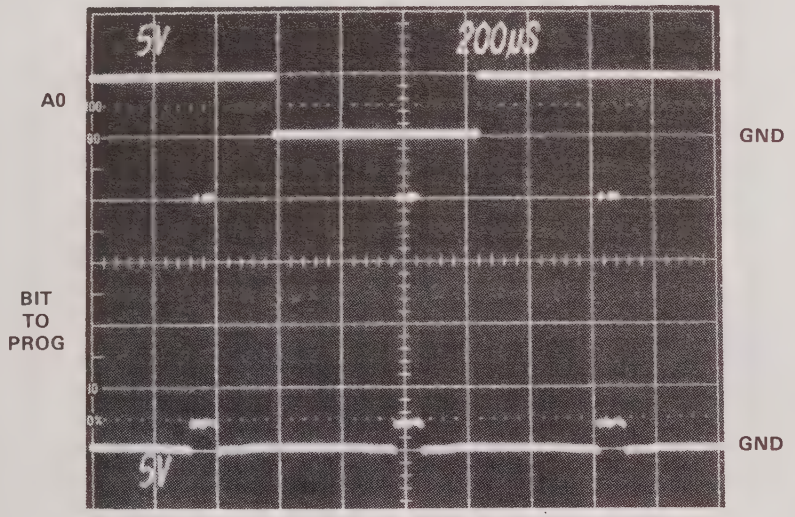

10V
2uS
E2
TR
GND
BIT
TO
PROG
GND
5V
331uS

7

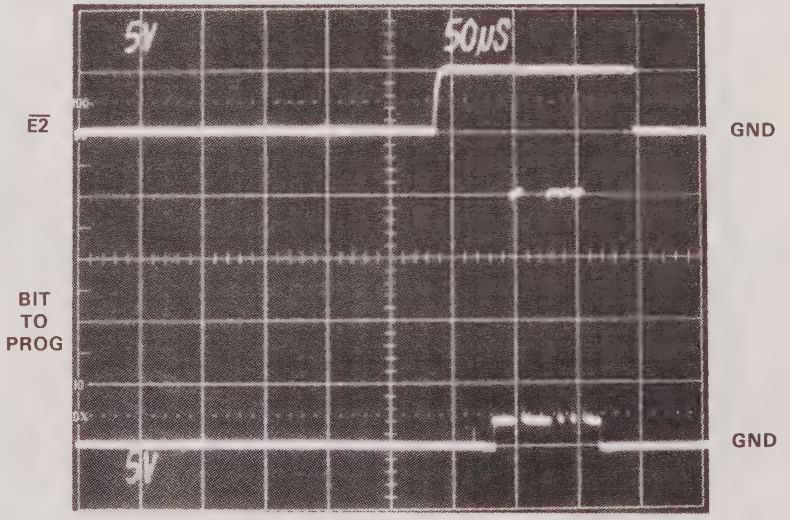
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		XH	5/83

DATA I/O ISSAQUAH, WA

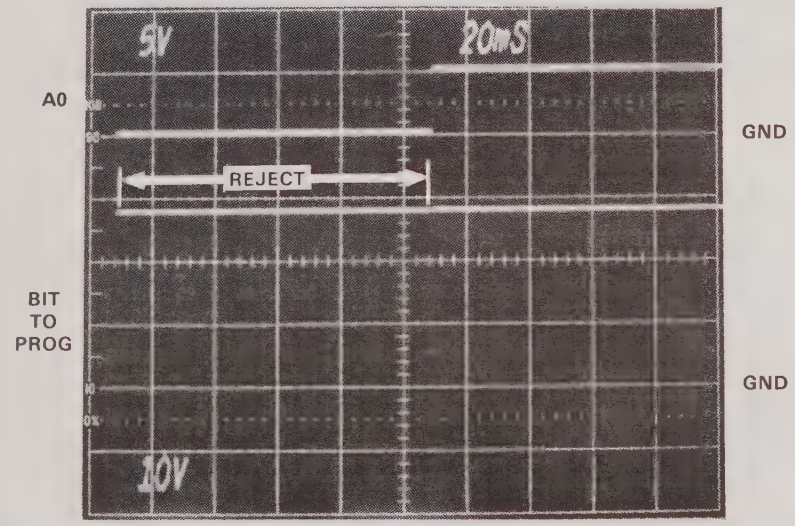
TITLE: TIMING DIAGRAM FAMILY CODES 67, 68		DRAWN BY: BG / PAP CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2

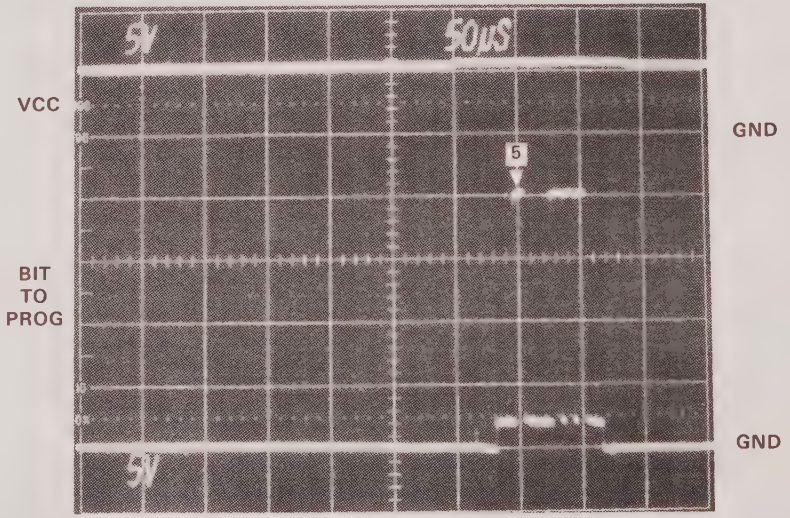

5V
200µS
A0
GND
BIT
TO
PROG
GND
5V

1


5V
50µS
$\overline{E2}$
GND
BIT
TO
PROG
GND
5V

2


5V
20mS
A0
GND
REJECT
BIT
TO
PROG
GND
10V


5V
50µS
VCC
GND
5
BIT
TO
PROG
GND
5V

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.00	5.20	5.40	V	
	VPP					NA
	VOP	27.5	28.0	28.5	V	
	TPW	7.0	7.5	8.0	µs	See Note 3
	T_R	0.21		0.30	µs	
	T_F	0.21		0.30	µs	
	Overprogram		4		Pulses	See Note 4
	Reject		10,000		Pulses	
	Duty Cycle	70	75	80	%	
1ST PASS VERIFY	VCC	4.0	4.1	4.2	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	25.0	26.0	27.0	V	701-1655/TP4
	Low Load	25.0	26.0	27.0	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.4	6.5	6.6	V	
	VREF	6.9	7.0	7.1	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	8.6	9.6	10.6	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 69.*
2. *Load RAM with hex 01 for Family 70.*
3. *Measurement taken at 10V point of 01 with a 100 Ω load.*
4. *10,000 pulses equals 100 ms, as shown in photo 3.*
5. *Do not use a wirewound load resistor.*
6. *01 loaded with a 100Ω, 5-watt resistor for photos 1, 2, 4-7.*

REVISIONS

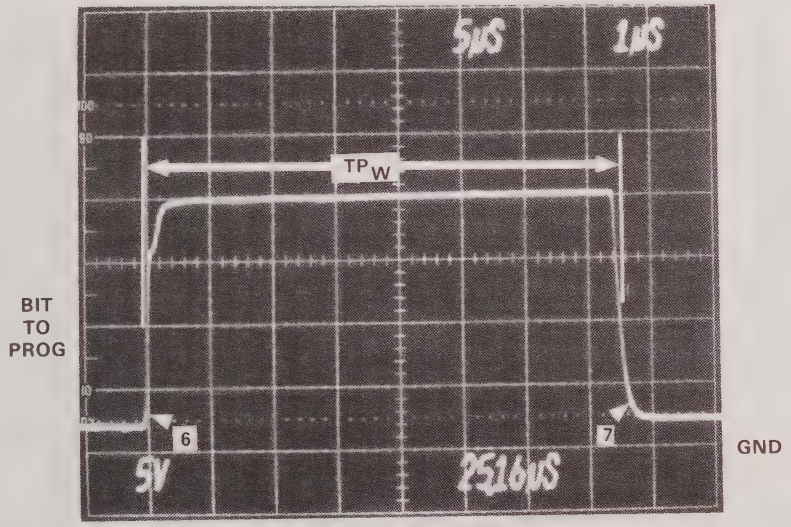
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.F.J.	11/82
		ECN #4831		KM	5/84
		ECN #5023		CFJ	3/84

DATA I/O ISSAQUAH, WA

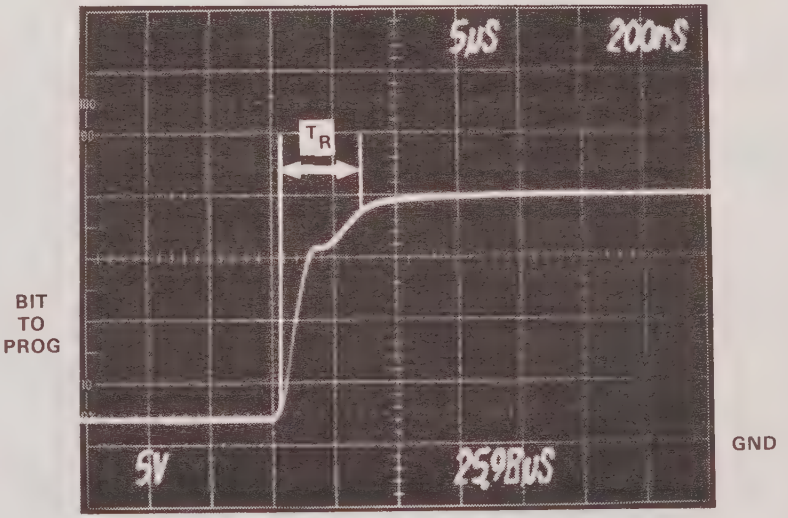
TITLE: TIMING DIAGRAM	DRAWN BY:
FAMILY CODES 69, 70	CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

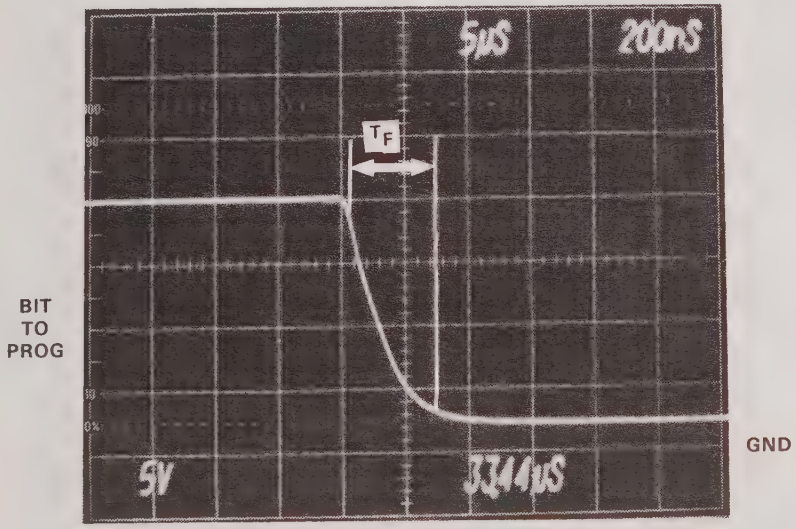
SCALE | SHEET 1/2


5µS
1µS
TPW
BIT
TO
PROG
6
7
GND
5V
2516µS

5


5µS
200nS
TR
BIT
TO
PROG
GND
5V
2598µS

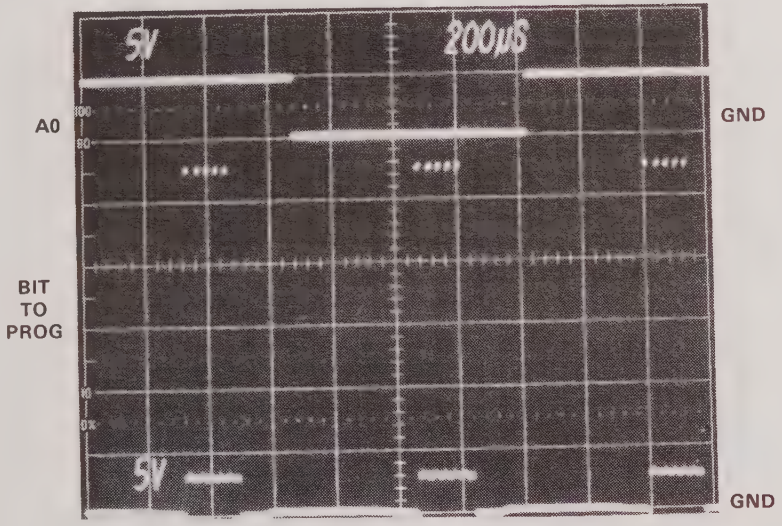
6


5µS
200nS
TF
BIT
TO
PROG
GND
5V
3344µS

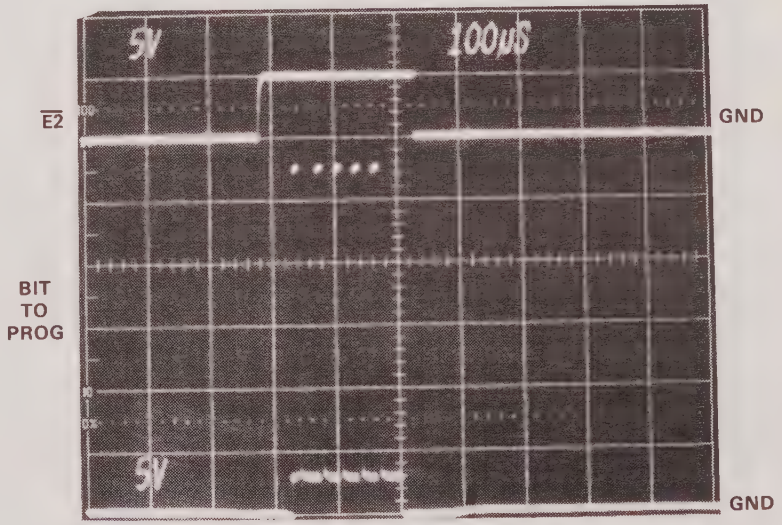
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.T.J.	11/82
		ECN #4831		XA	5/83

DATA I/O ISSAQUAH, WA

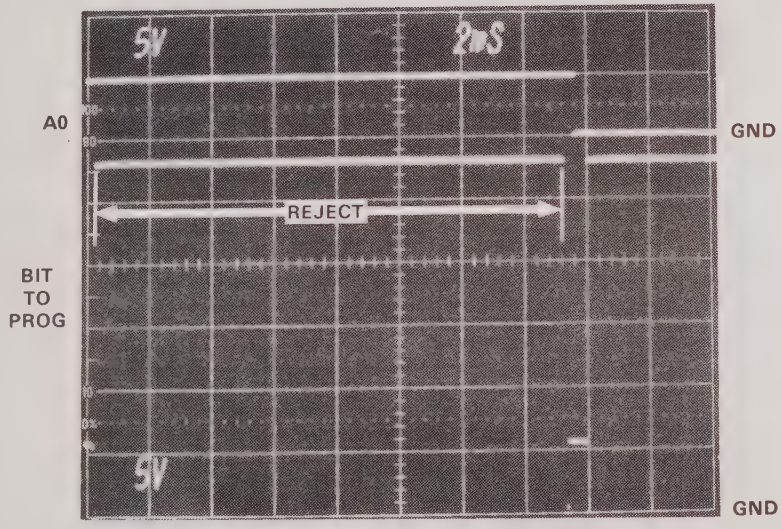
TITLE: TIMING DIAGRAM FAMILY CODES 69, 70		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2

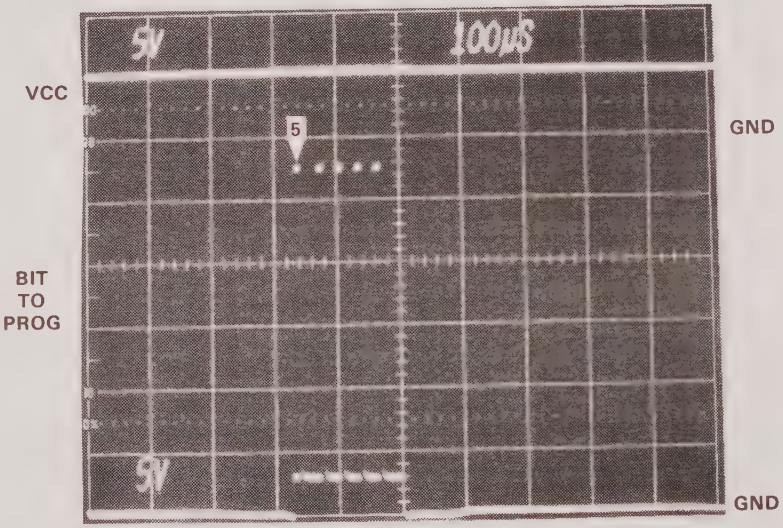

5V
200µS
A0
GND
BIT
TO
PROG
5V
GND

1


5V
100µS
$\overline{E2}$
GND
BIT
TO
PROG
5V
GND

2


5V
2mS
A0
GND
REJECT
BIT
TO
PROG
5V
GND


5V
100µS
VCC
5
GND
BIT
TO
PROG
5V
GND

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.90	5.10	5.30	V	
	VPP					NA
	VOP	27.5	28.0	28.5	V	
	TPW	7.0	7.5	8.0	µs	See Note 3
	T_R	0.28			µs	
	T_F	0.28			µs	
	Overprogram		4		Pulses	
	Reject		1,000		Pulses	See Note 4
	Duty Cycle	70			%	
1ST PASS VERIFY	VCC	4.0	4.1	4.2	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	25.5	26.0	26.5	V	701-1655/TP4
	Low Load	25.5	26.0	26.5	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.4	6.5	6.6	V	
	VREF	3.9	4.0	4.1	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	6.2	6.7	7.2	V	701-1655/TP3

NOTES

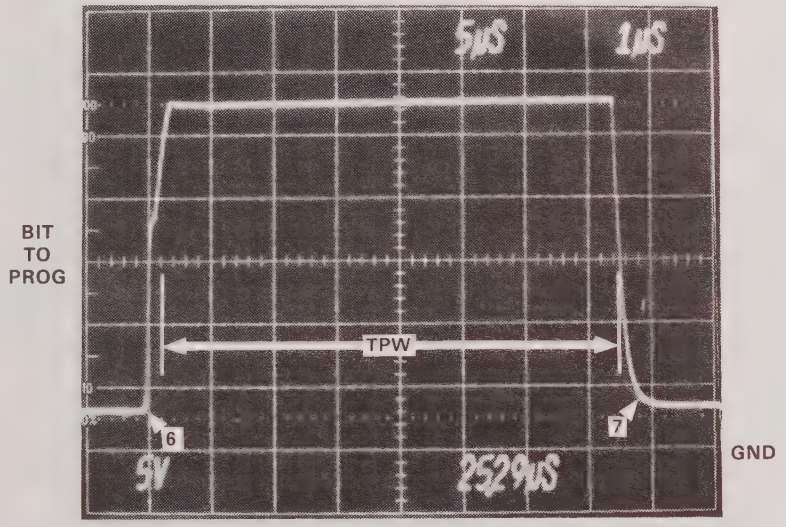
1. *Load RAM with hex FE for Family 71*
2. *Load RAM with hex 01 for Family 72.*
3. *Measurement taken a5 15V point of 01 with one 150Ω load.*
4. *1,000 pulses equals 10 ms, as shown in photo 3.*
5. *Do not use a wirewound load resistor.*
6. *01 loaded with a 150Ω, 6-watt resistor for photos 1, 2, 4-7.*

REVISIONS

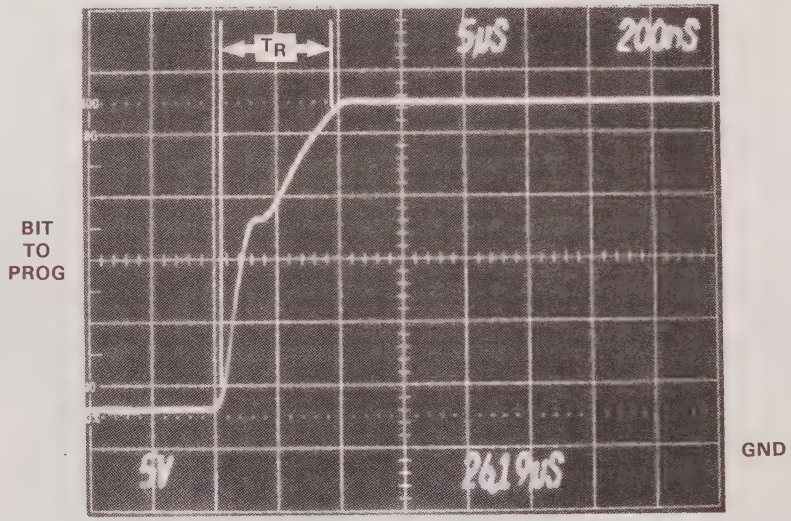
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		XH	5/83
		ECN #5023		CTZ	3/84

DATA I/O ISSAQUAH, WA

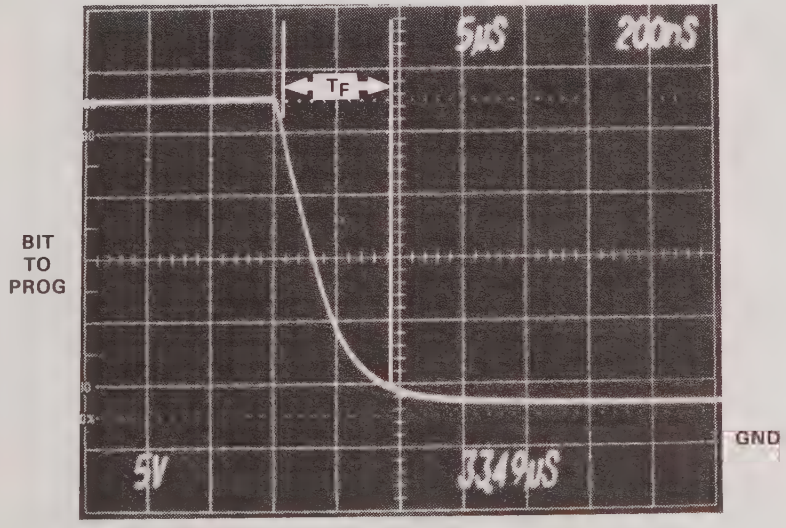
TITLE: TIMING DIAGRAM		DRAWN BY: PP
FAMILY CODES 71, 72		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2


BIT
TO
PROG
5µS
1µS
TPW
6
7
5V
2529µS
GND

5


BIT
TO
PROG
TR
5µS
200nS
5V
2619µS
GND

6

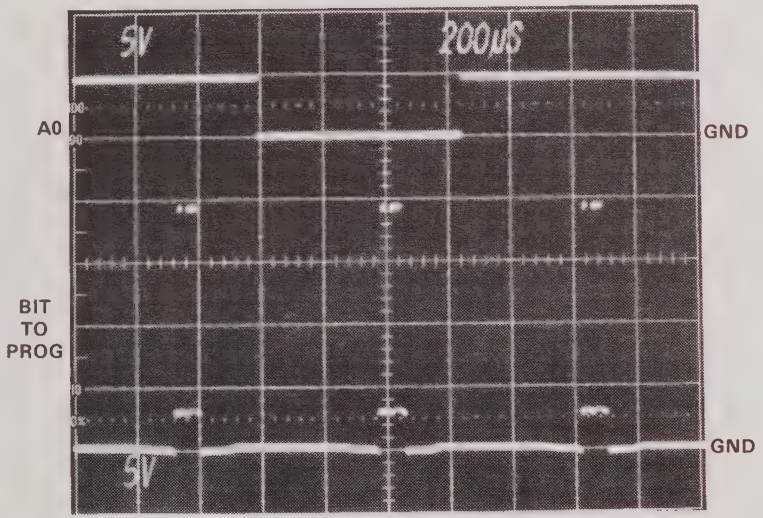

BIT
TO
PROG
5µS
200nS
TF
GND
5V
3319µS

7

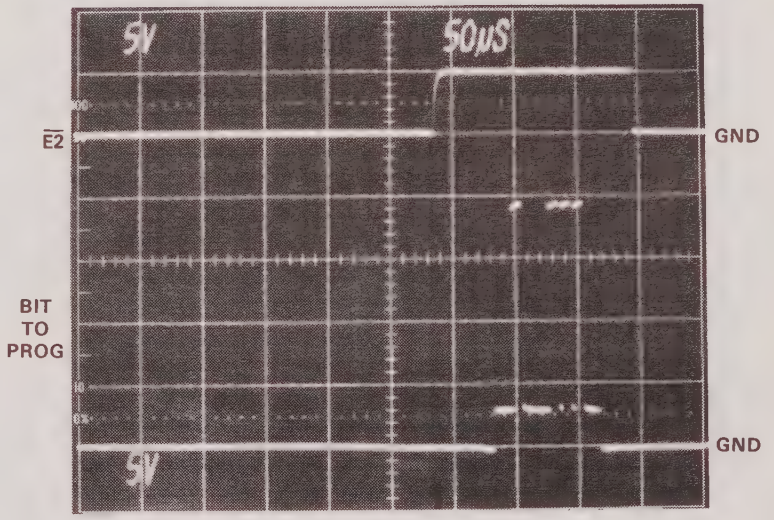
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		XH	5/83

DATA I/O ISSAQUAH, WA

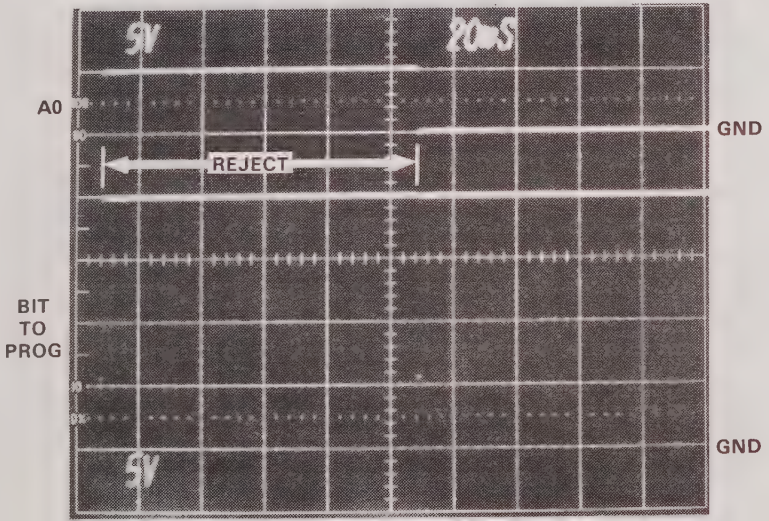
TITLE: TIMING DIAGRAM FAMILY CODES 71, 72		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2

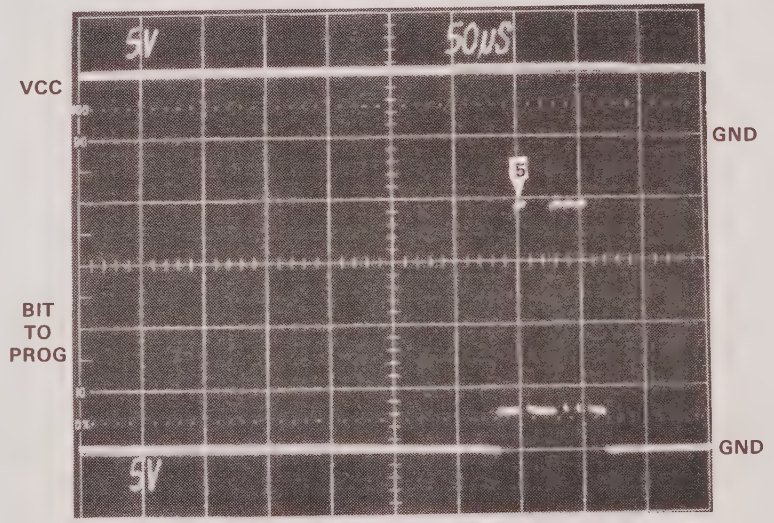

5V
200µS
A0
GND
BIT
TO
PROG
GND
5V

1


5V
50µS
$\overline{E2}$
GND
BIT
TO
PROG
GND
5V

2


5V
20mS
A0
GND
REJECT
BIT
TO
PROG
GND
5V


5V
50µS
VCC
GND
5
BIT
TO
PROG
GND
5V

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.90	5.10	5.30	V	
	VPP					NA
	VOP	19.6	20.0	20.0	V	
	TPW	7.1	7.5	7.9	µs	See Note 3
	TR	180			ns	
	TF	180			ns	
	Overprogram		4		Pulses	
	Reject		10,000		Pulses	See Note 4
	Duty Cycle	70			%	
1ST PASS VERIFY	VCC	4.5	4.6	4.7	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	25.5	26.0	26.5	V	701-1655/TP4
	Low Load	25.5	26.0	26.5	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.5	6.6	6.7	V	
	VREF	4.4	4.5	4.6	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	6.7	7.2	7.7	V	701-1655/TP3

NOTES

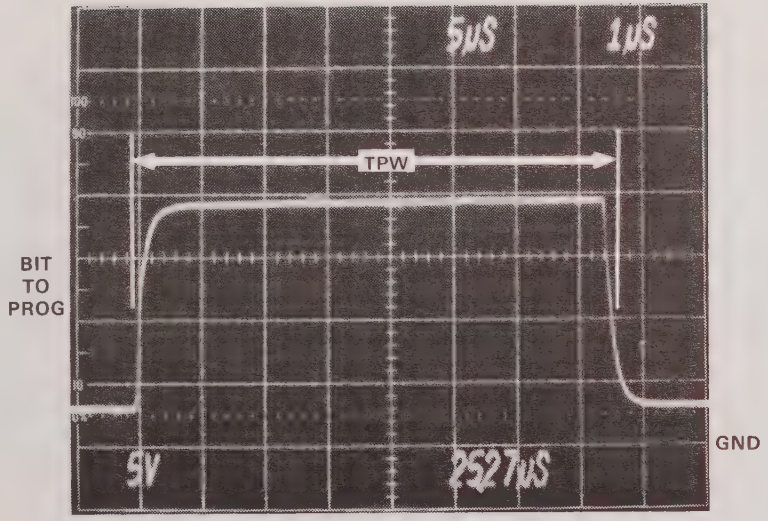
1. *Load RAM with hex FE for Family 73.*
2. *Load RAM with hex 01 for Family 74.*
3. *Measurement taken at 10V point of 01 with a 150 Ω load.*
4. *10,000 pulses equals 100 ms, as shown in photo 3.*
5. *Do not use a wirewound load resistor.*
6. *For Pinouts 16 and 21, E2 is seen on E1.*

REVISIONS

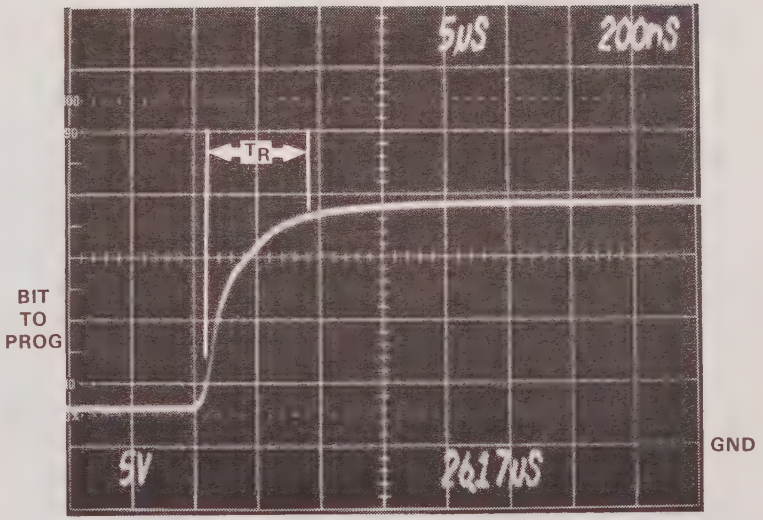
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		XH	5/83
		ECN #5023		C73	3/84

DATA I/O ISSAQUAH, WA

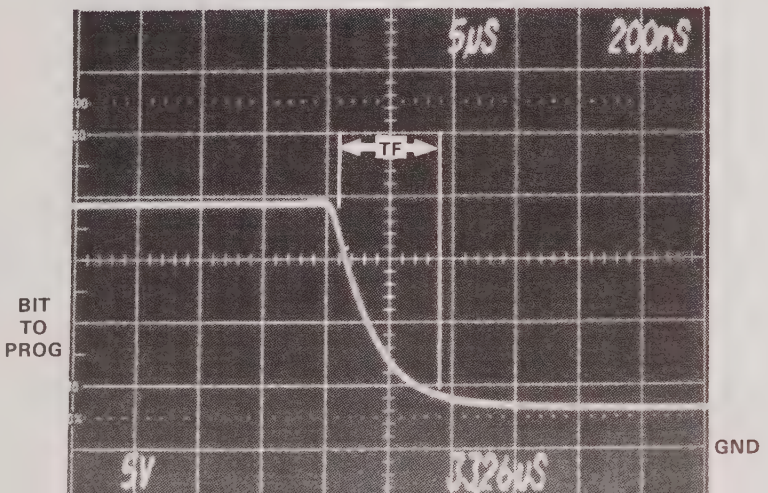
TITLE: TIMING DIAGRAM		DRAWN BY: EE
FAMILY CODES 73, 74		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2


5μS
1μS
TPW
BIT
TO
PROG
GND
5V
2527μS

5


5μS
200nS
TR
BIT
TO
PROG
GND
5V
2617μS

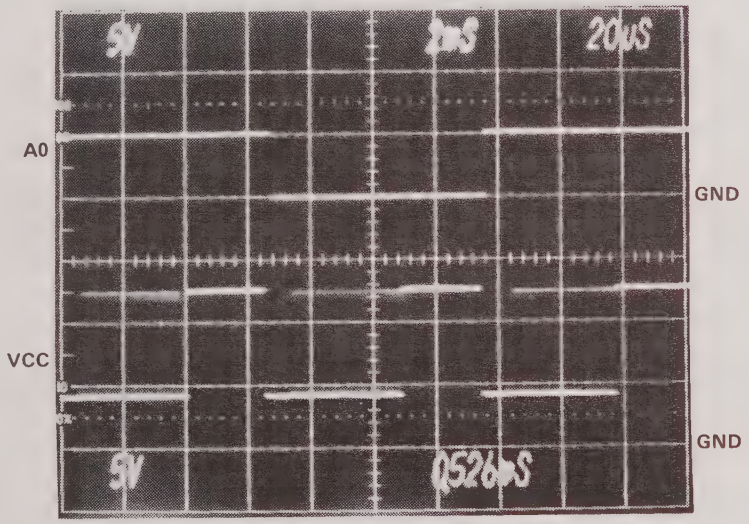
6


5μS
200nS
TF
BIT
TO
PROG
GND
5V

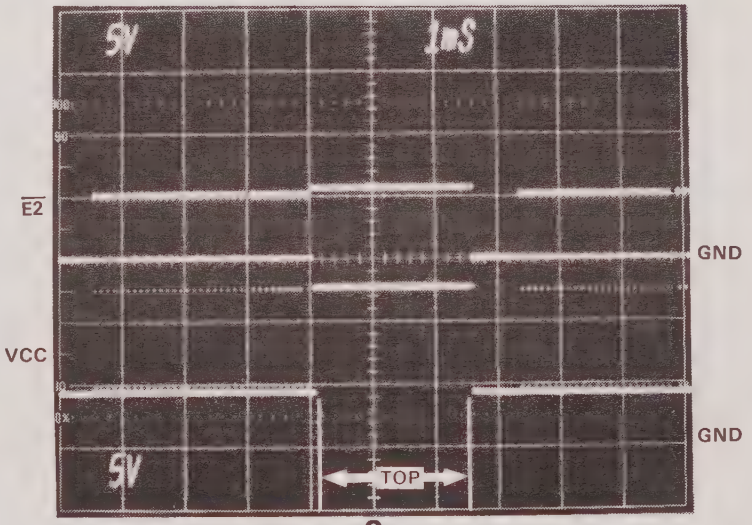
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		XH	5/83

DATA I/O ISSAQUAH, WA

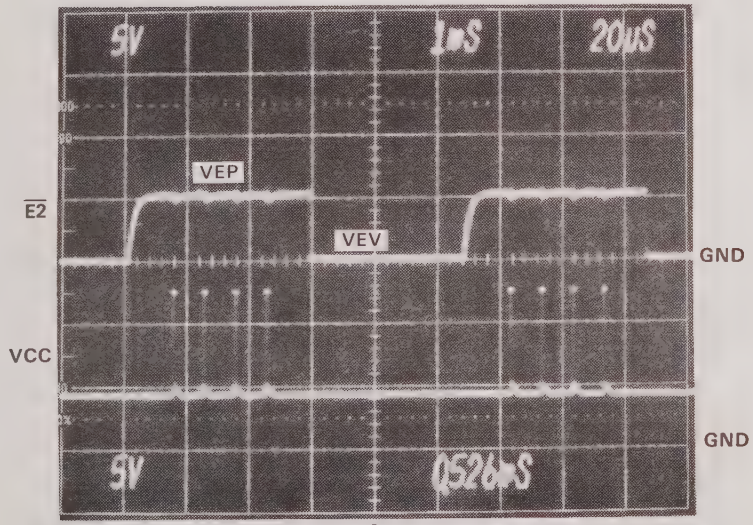
TITLE: TIMING DIAGRAM FAMILY CODES 73, 74			DRAWN BY: EE CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059	
SCALE			SHEET 2/2


5V
1mS
20μS
A0
GND
VCC
GND
5V
0526mS

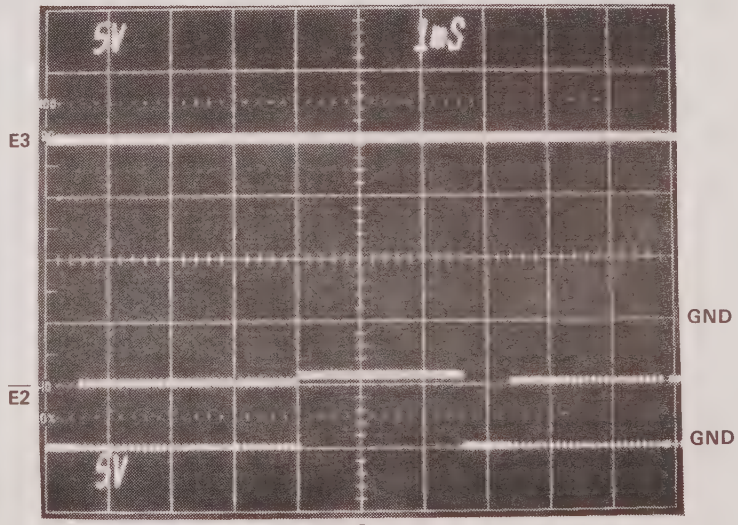
1


5V
1mS
E2
GND
VCC
GND
5V
TOP

2


5V
1mS
20μS
VEP
E2
VEV
GND
VCC
GND
5V
0526mS

3


5V
1mS
E3
GND
E2
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	12.0	12.5	13.0	V	See Note 6
	VCCV	4.25	4.5	4.75	V	
	VEP	3.0	5.0	5.5	V	
	VEV	0.0	0.2	0.4	V	
	TPWB	140	200	260	ns	See Note 4
	TPWE	7.2	8.0	8.8	µs	See Note 4
	TR	320	400	480	ns	See Note 5
	TF	50	100	200	ns	See Note 5
	Reject	780	800	820	ms	
	TOP	2.2	2.5	2.8	ms	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	0.4	0.5	0.6	V	701-1655/TP2
	High Load	17.5	18.5	19.5	V	701-1655/TP4
	Low Load	17.5	18.5	19.5	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	2.2	2.3	2.4	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	6.9	7.9	8.9	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 75.*
2. *Load RAM with hex 01 for Family 76.*
3. *To observe waveforms, load 01 with a 100 Ω, 2-watt resistor. Do not use a wirewound resistor.*
4. *V_{CC} pulse width ramps linearily from TPWB to TPWE. This is visible only with no load on 01. TPW is measured at 12V.*
5. *TR and TF are measured from 5V to 12V.*
6. *Photos 5 and 6 were taken with V_{CC} loaded with a 50 Ω, 5-watt resistor. Do not use a wirewound resistor.*

B-153
981-0001

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4772		XX	1/83
		ECN #4831		XX	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 75, 76

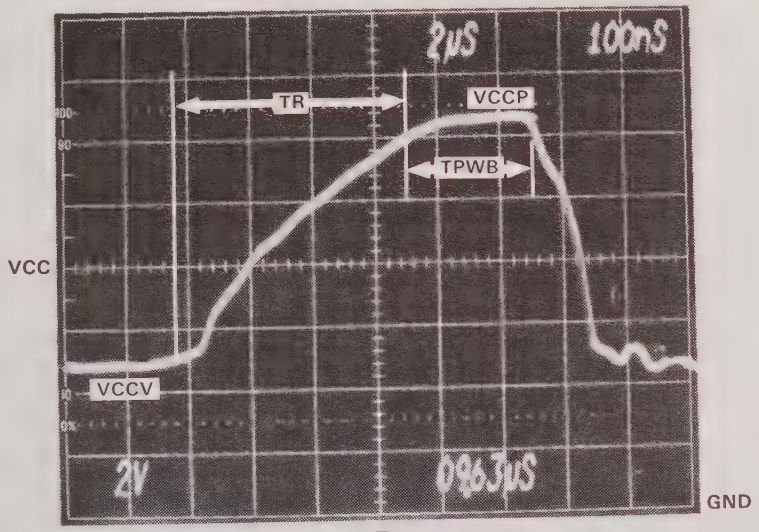
DRAWN BY: BG

CHECKED BY:

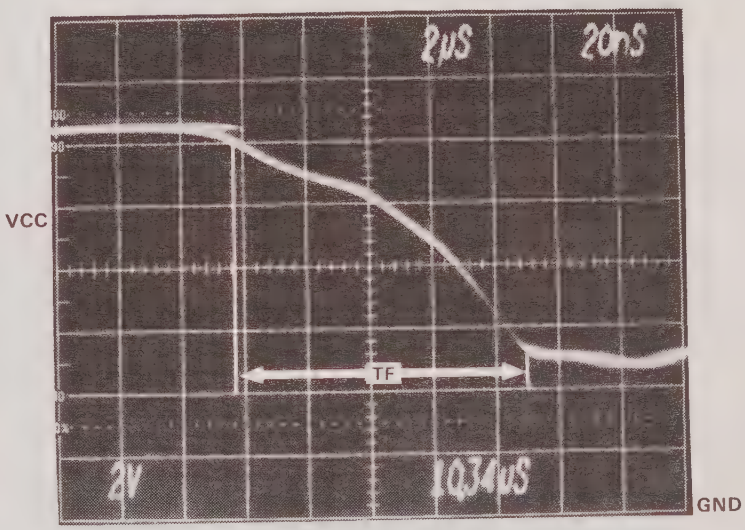
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 1/2


2µS
100nS
TR
VCCP
TPWB
VCC
VCCV
2V
0.63µS
GND

5

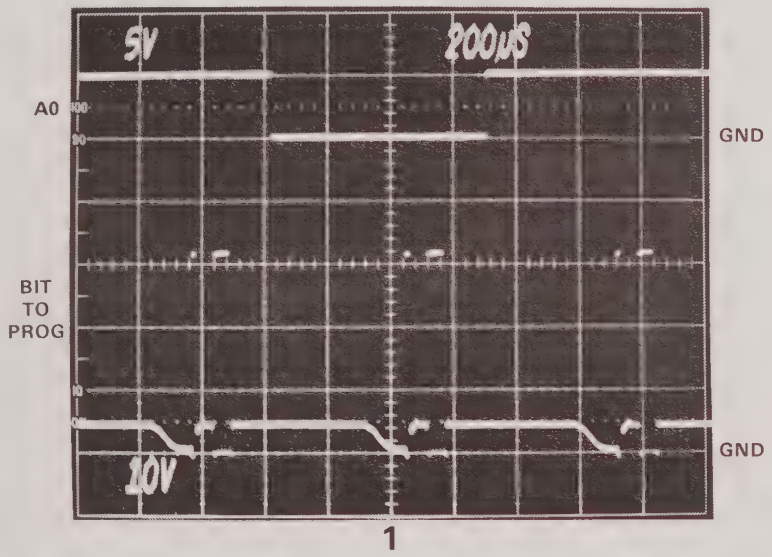

2µS
20nS
VCC
TF
2V
1.31µS
GND

6

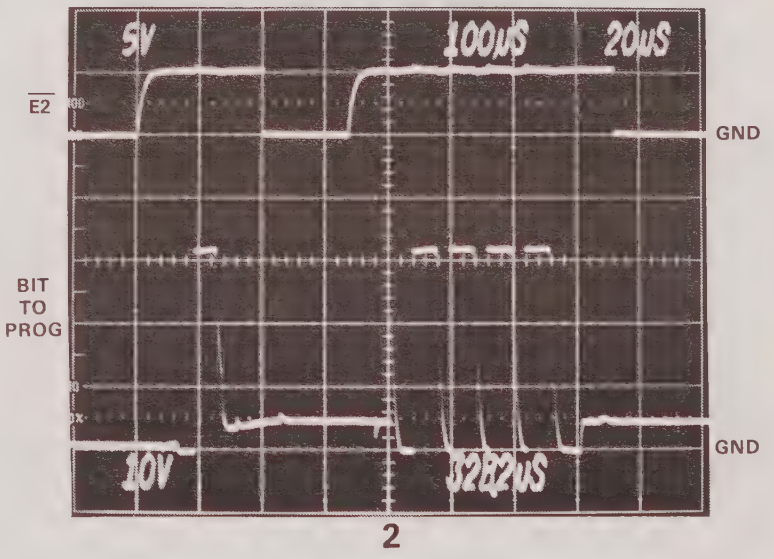
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.J.	11/82
		ECN #4831		XH	5/83

DATA I/O ISSAQUAH, WA

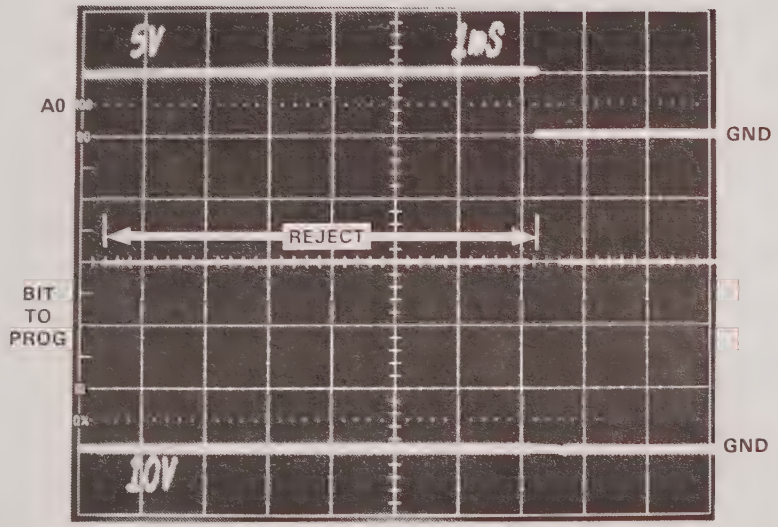
TITLE: TIMING DIAGRAM FAMILY CODES 75, 76			DRAWN BY: BLK KLL CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059	
SCALE			SHEET 2/2


5V
200µS
A0
GND
BIT
TO
PROG
GND
10V

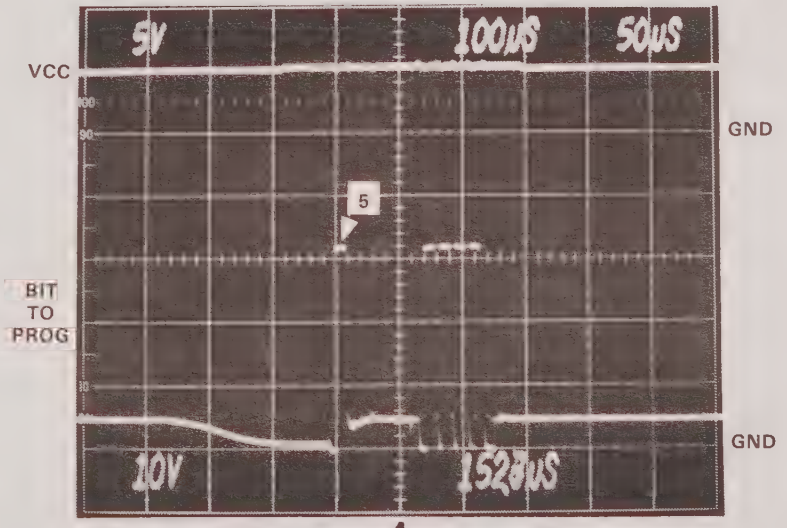
1


5V
100µS
20µS
E2
GND
BIT
TO
PROG
GND
10V

2


5V
1mS
A0
GND
REJECT
BIT
TO
PROG
GND
10V

3


5V
100µS
50µS
VCC
GND
5
BIT
TO
PROG
GND
10V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.00	5.20	5.40	V	
	VPP					NA
	VOP	31.5	31.7	32.0	V	
	TPW	7.2	7.5	7.8	µs	See Note 3
	TR	0.34		0.68	µs	
	TF	0.34		0.48	µs	
	Overprogram		4		Pulses	
	Reject		100		Pulses	See Note 4
	Duty Cycle	11			%	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	7.8	8.8	9.8	V	701-1655/TP4
	Low Load	7.8	8.8	9.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.4	6.5	6.6	V	
	VREF	3.9	4.0	4.1	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	5.6	6.6	7.6	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 77.*
2. *Load RAM with hex 01 for Family 78.*
3. *Measurement taken at 15V point of 01 with 150 Ω load.*
4. *100 pulses equals 6.8 ms, as shown in photo 3, with 150 Ω load.*
5. *Do not use a wirewound load resistor.*
6. *Photos 1, 2, and 4 have 01 loaded with 3.3K Ω.*

REVISIONS

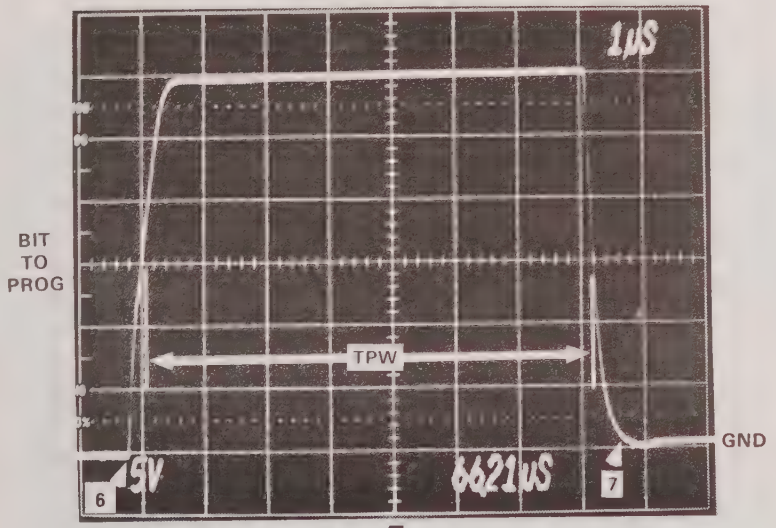
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ.	11/82
		ECN #4772		XA	1/83
		ECN #4831		ZH	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

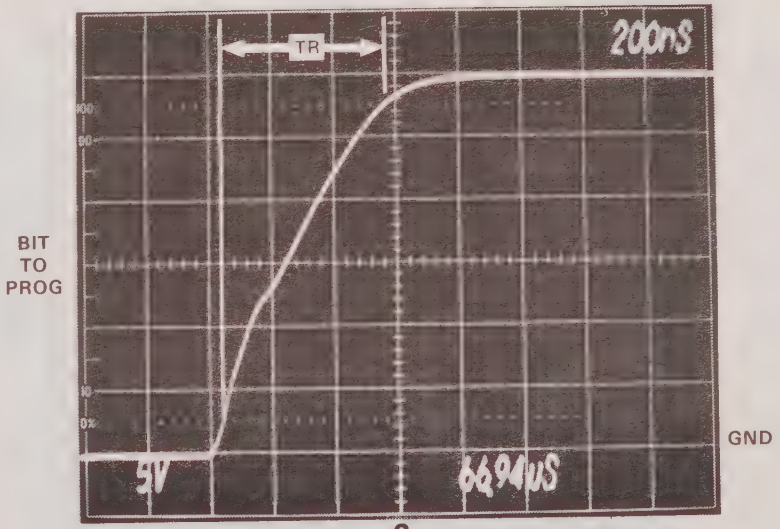
TITLE: TIMING DIAGRAM FAMILY CODES 77, 78	DRAWN BY: EE CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

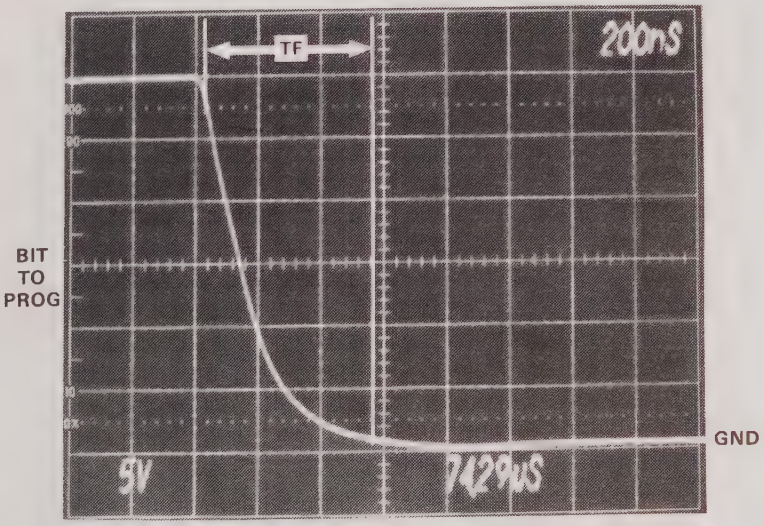
SCALE | SHEET 1/2


1µS
BIT
TO
PROG
TPW
GND
5V
6
6621µS
7

5


TR
200nS
BIT
TO
PROG
GND
5V
6694µS

6

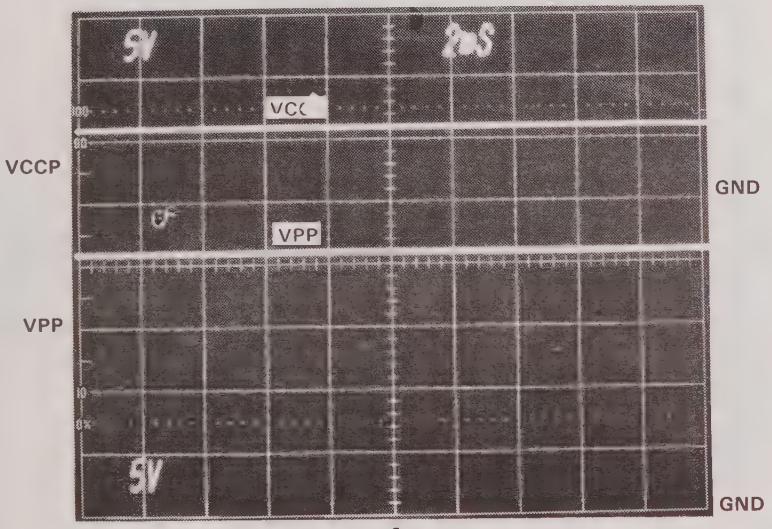

TF
200nS
BIT
TO
PROG
GND
5V
7429µS

7

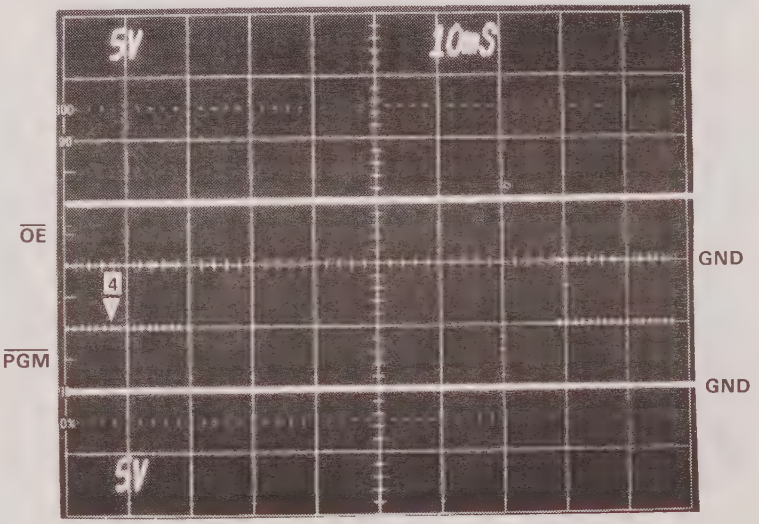
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		ZH	5/83

DATA I/O ISSAQUAH, WA

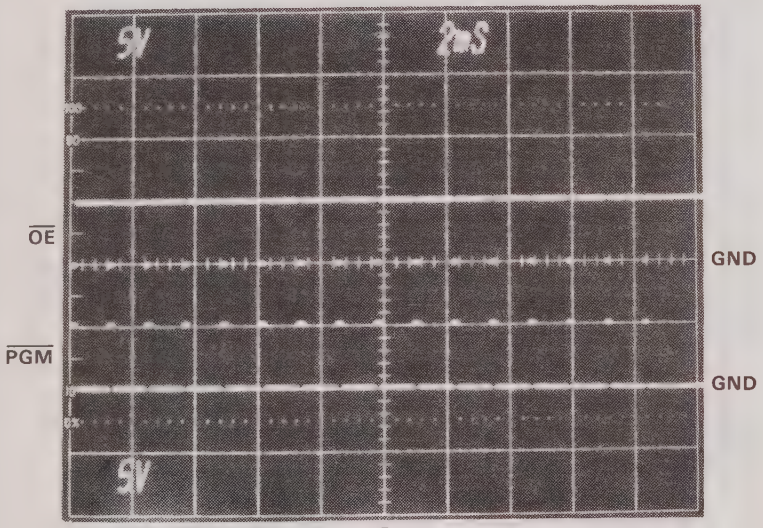
TITLE: TIMING DIAGRAM FAMILY CODES 77, 78		DRAWN BY: EE CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE:		SHEET 2/2


5V
2mS
VCC
VCCP
GND
VPP
VPP
5V
GND

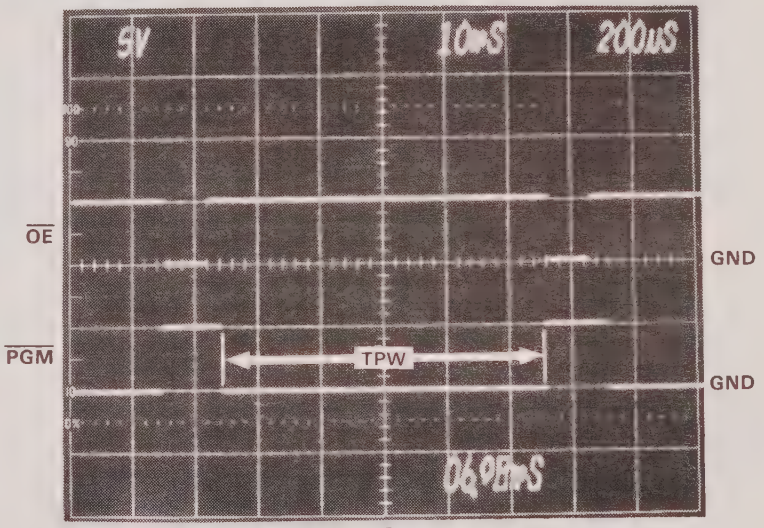
1


5V
10mS
OE
GND
4
PGM
GND
5V

2


5V
2mS
OE
GND
PGM
GND
5V

3


5V
10mS
200uS
OE
GND
PGM
TPW
GND
06 OBMS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.0	6.25	V	
	VOP					NA
	VPP	20.5	21.0	21.5	V	
	VPPV					NA
	TPW	0.95	1.0	1.05	ms	
	TR					NA
	TF					NA
	Reject		15		Pulses	
	Overprogram		1		Pulses	See Note 3
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

1. *Load RAM with hex FE for Family 79.*
2. *Load RAM with hex 01 for Family 80, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The overprogram pulse follows the reject pulses and its length is the number of reject pulses multiplied by 4 ms.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.B.	11/82
		ECN #4831		KH	5/83
		ECN #5023		CJB	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 79, 80

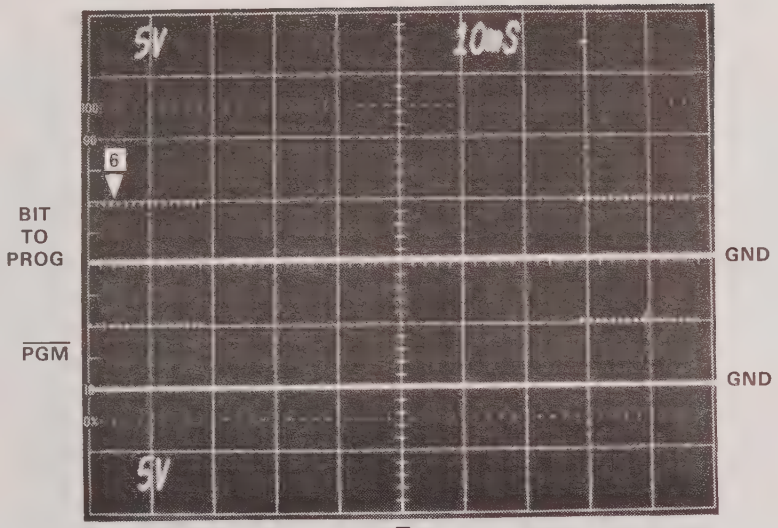
DRAWN BY: BG/KH

CHECKED BY:

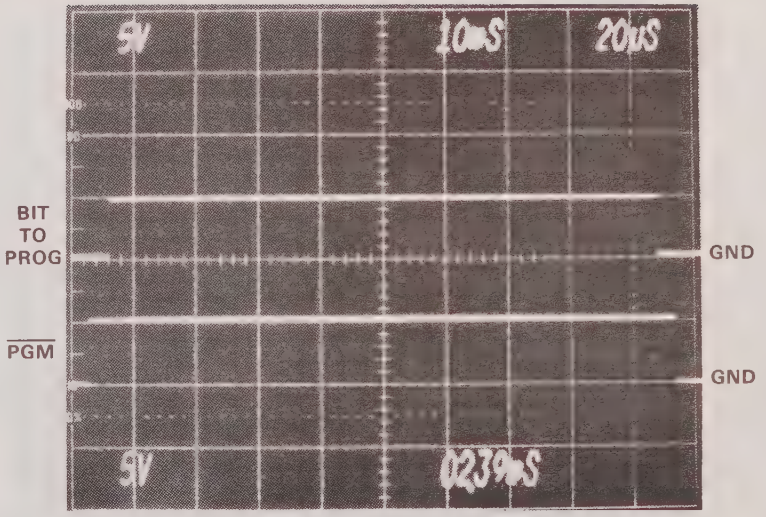
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-005

SCALE

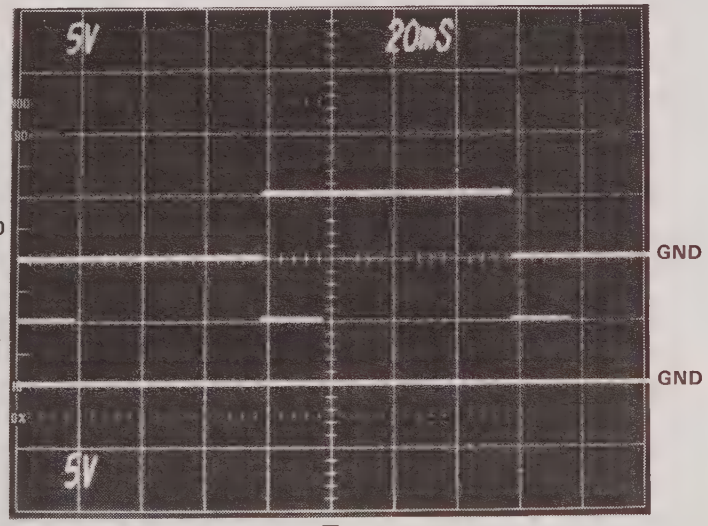
SHEET 1/2


5V
10mS
6
BIT
TO
PROG
GND
PGM
GND
5V

5


5V
10mS
20uS
BIT
TO
PROG
GND
PGM
GND
5V
0239mS

6


5V
20mS
A0
GND
PGM
GND
5V

7

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		XH	5/83

DATA I/O ISSAQUAH, WA

TITLE TIMING DIAGRAM

FAMILY CODES 79, 80

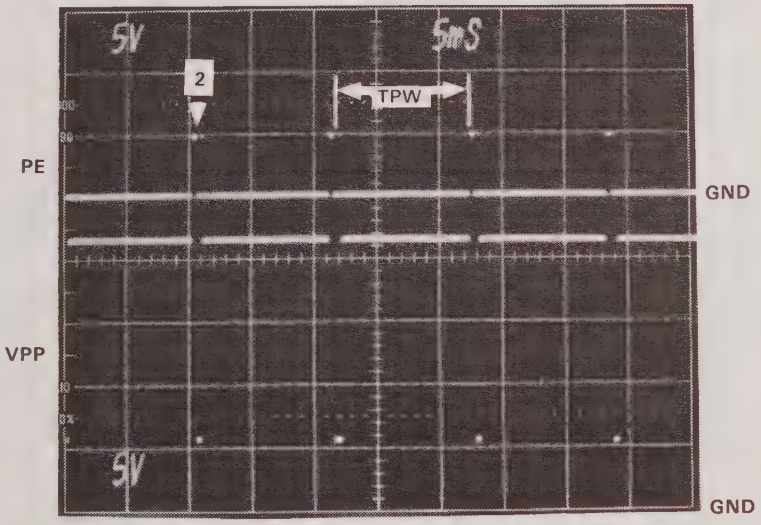
DRAWN BY: [signature]

CHECKED BY:

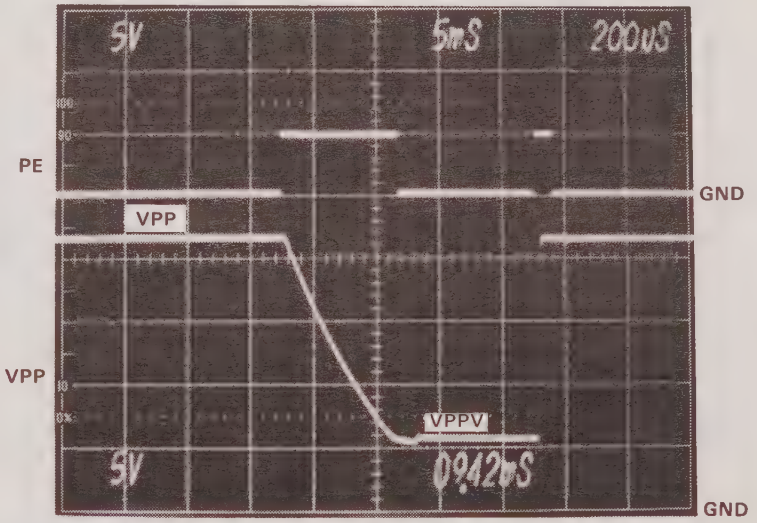
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

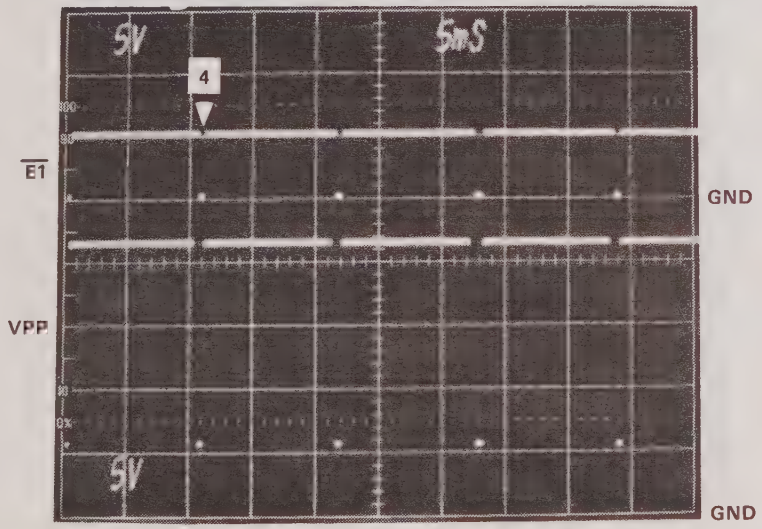
SHEET 2/2


5V
5mS
2
TPW
PE
GND
VPP
5V
GND

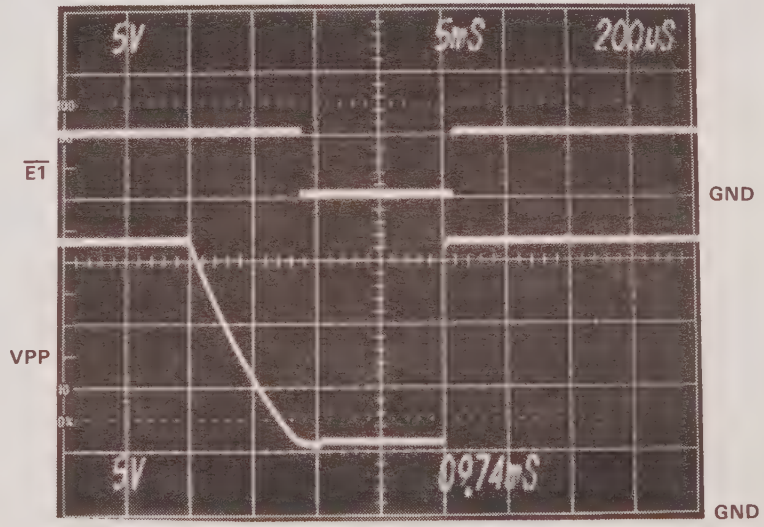
1


5V
5mS
200uS
PE
GND
VPP
VPP
VPPV
5V
0.942mS
GND

2


5V
5mS
4
E1
GND
VPP
5V
GND

3


5V
5mS
200uS
E1
GND
VPP
5V
0.974mS
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	20.0	21.0	22.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	9.8	10.0	10.2	ms	
	TR	1			µs	
	TF	1			µs	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 81.*
2. *Load RAM with hex 01 for Family 82, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photos 13 through 18 are Byte erase waveforms.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		XH	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE TIMING DIAGRAM

FAMILY CODES 81, 82

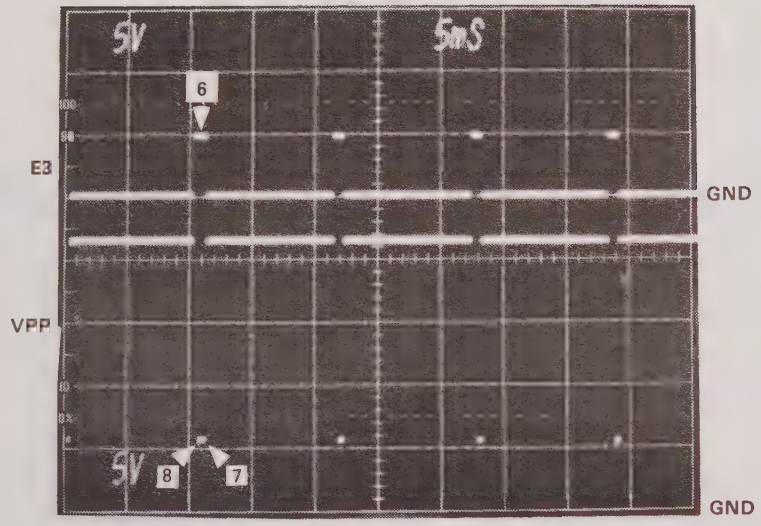
DRAWN BY:

CHECKED BY:

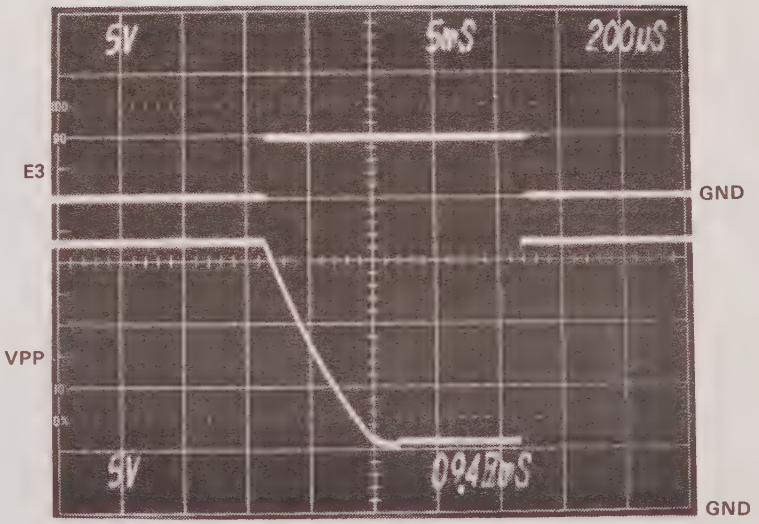
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

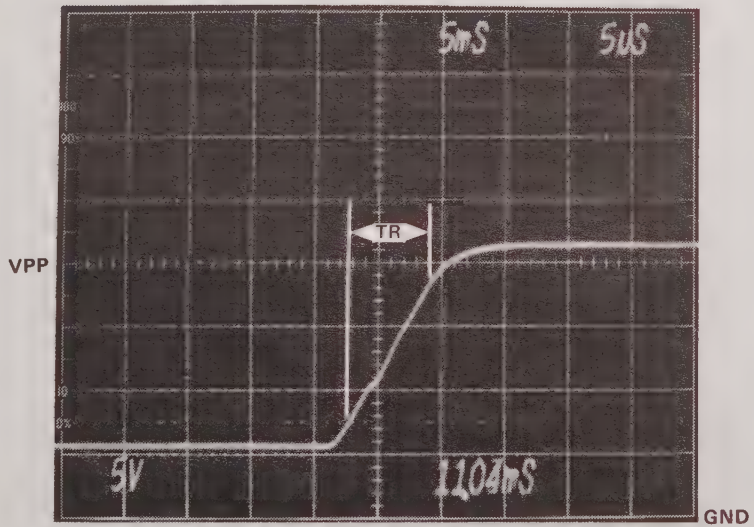
SHEET 1/4


5V
5mS
6
E3
GND
VPP
5V
8
7
GND

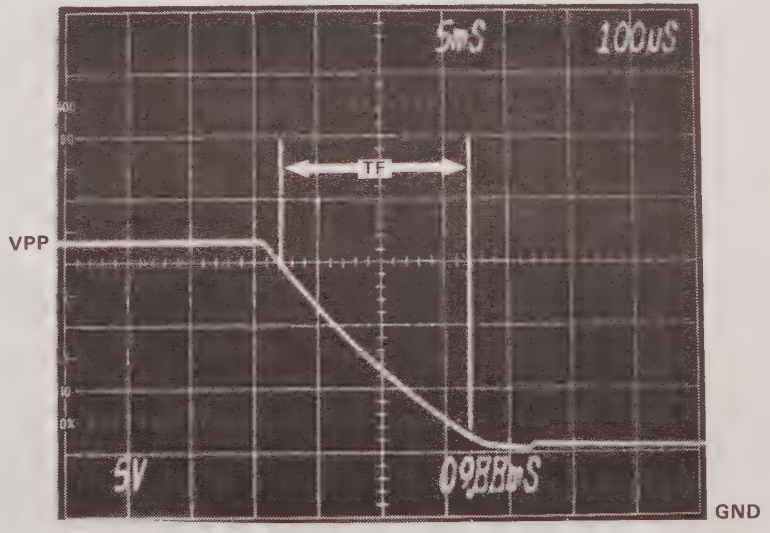
5


5V
5mS
200uS
E3
GND
VPP
5V
GND

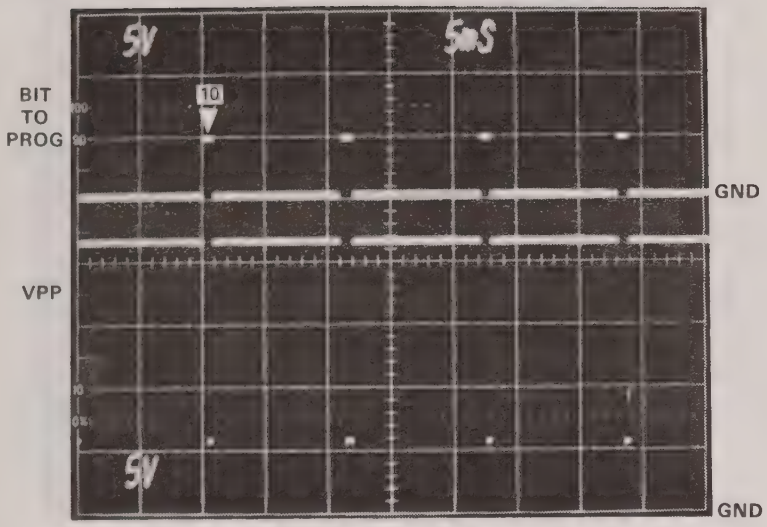
6


5mS
5uS
TR
VPP
5V
GND

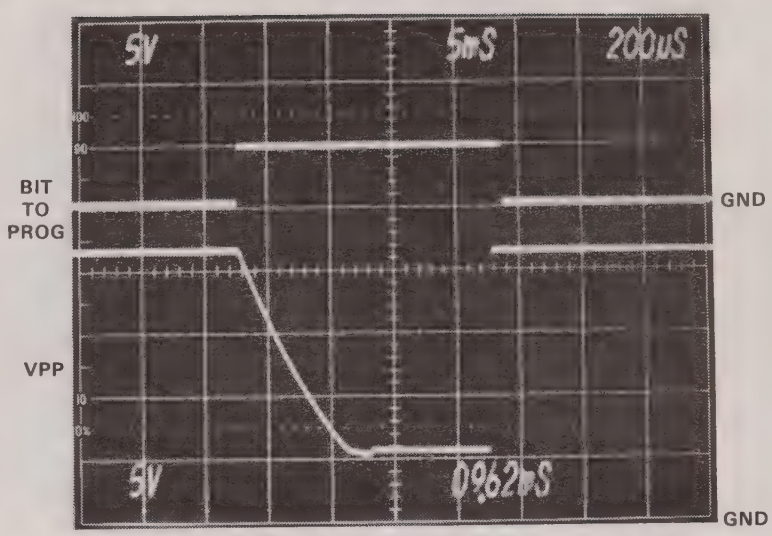
7


5mS
100uS
TF
VPP
5V
GND

8



9

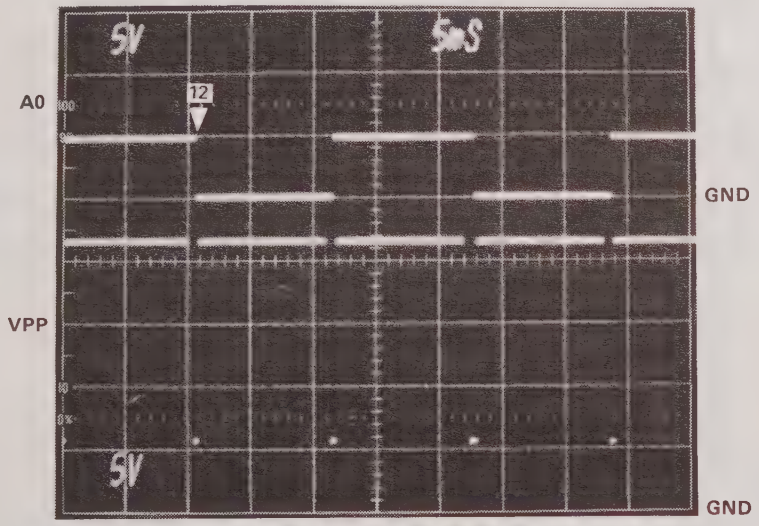


10

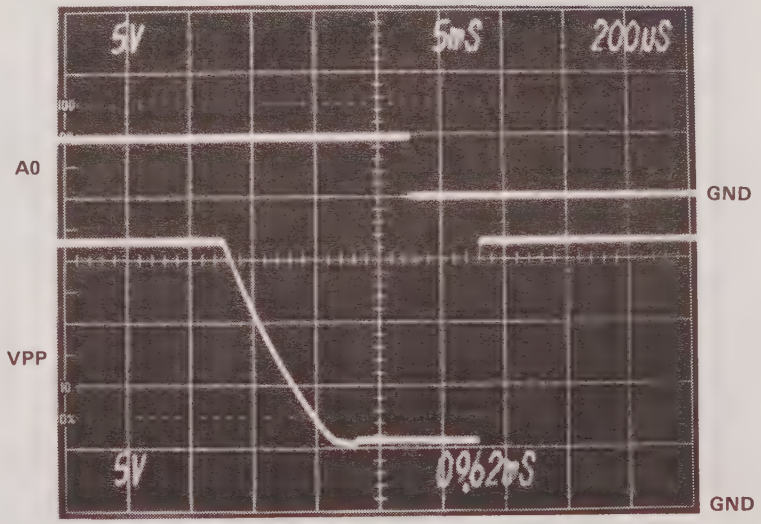
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		KM	5/83

DATA I/O ISSAQUAH, WA

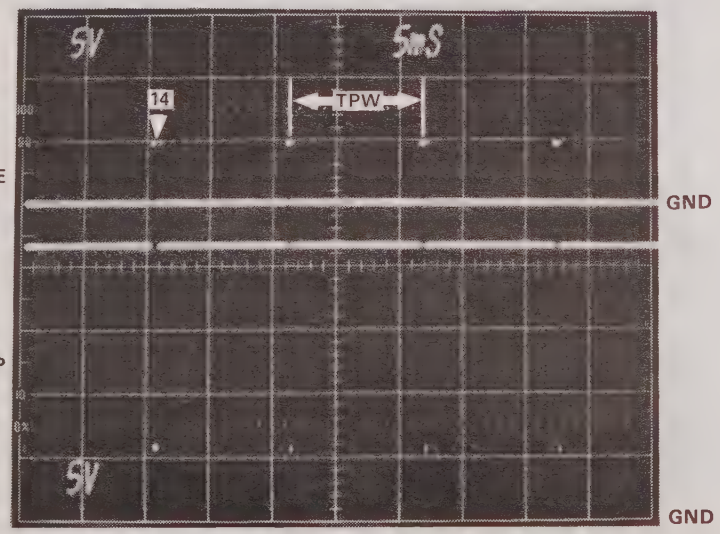
TITLE: TIMING DIAGRAM		DRAWN BY:
FAMILY CODES 81, 82		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/4


5V
5mS
A0
12
GND
VPP
5V
GND

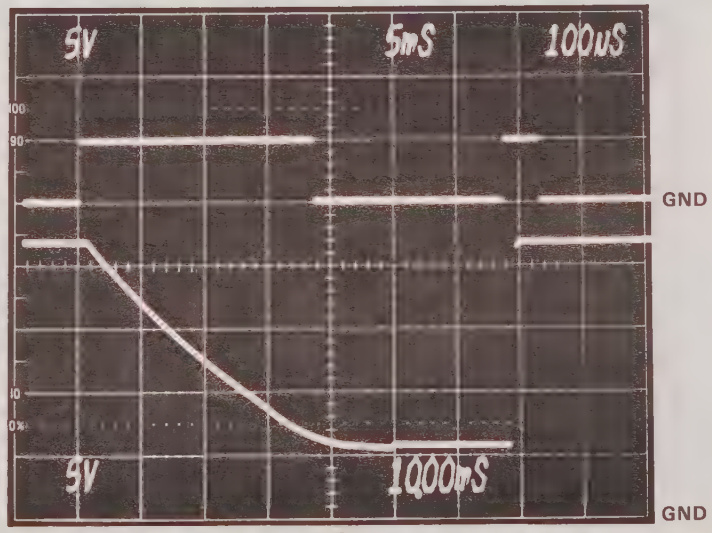
11


5V
5mS
200uS
A0
GND
VPP
5V
0962mS
GND

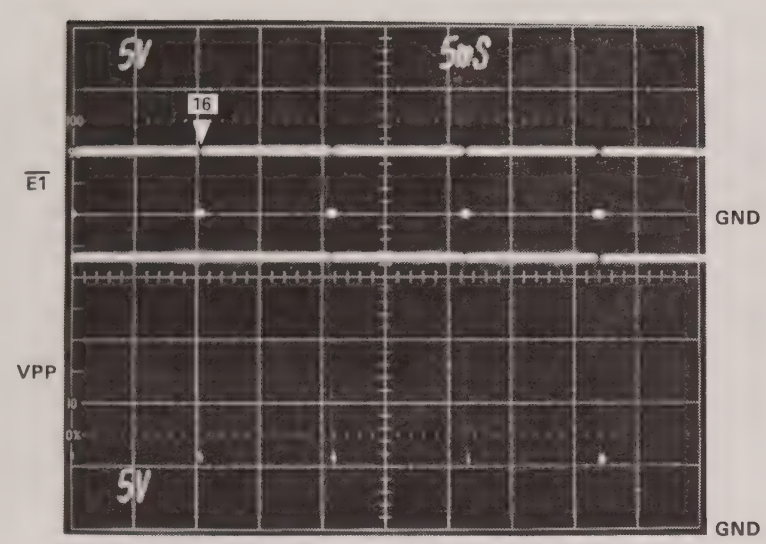
12


5V
5mS
14
TPW
PE
GND
VPP
5V
GND

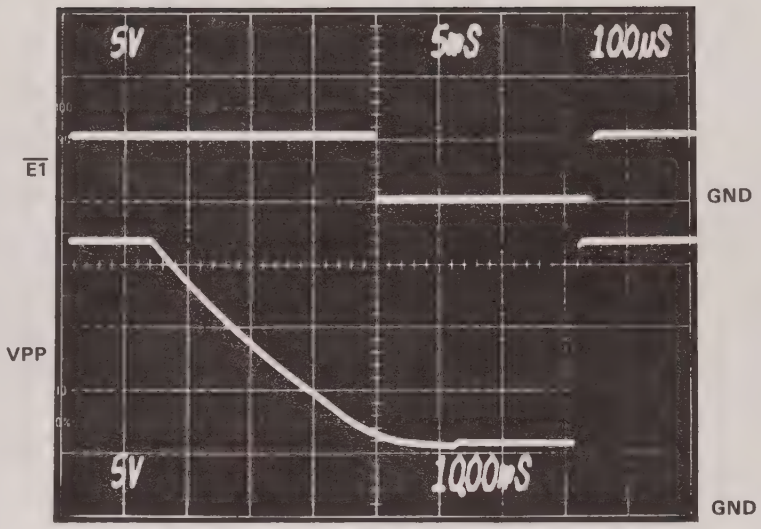
13


5V
5mS
100uS
PE
GND
VPP
5V
1000mS
GND

14



15



16

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ.	11/82
		ECN #4831		XH	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE TIMING DIAGRAM

FAMILY CODES 81, 82

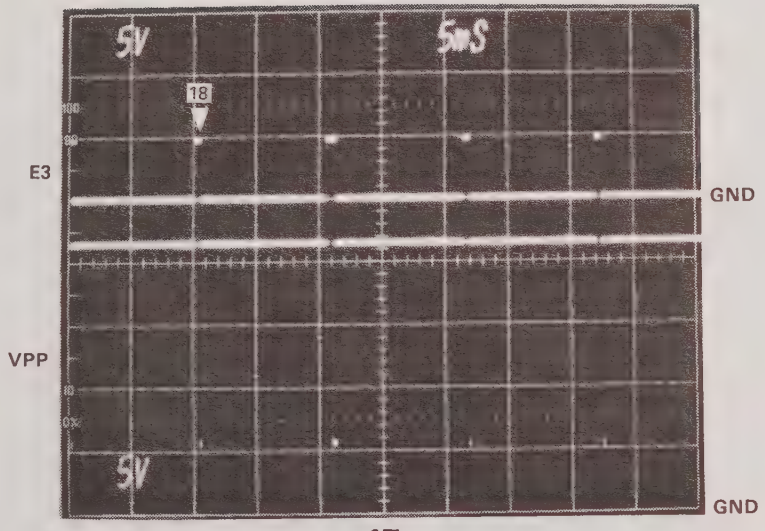
DRAWN BY:

CHECKED BY:

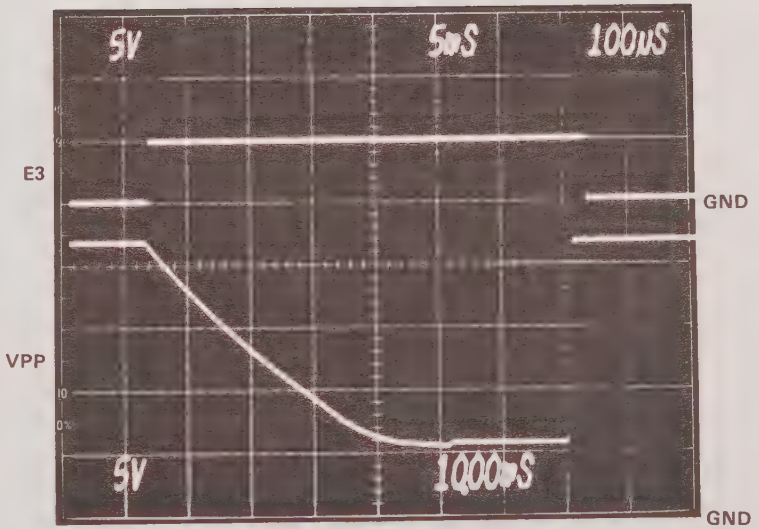
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 3/4



17

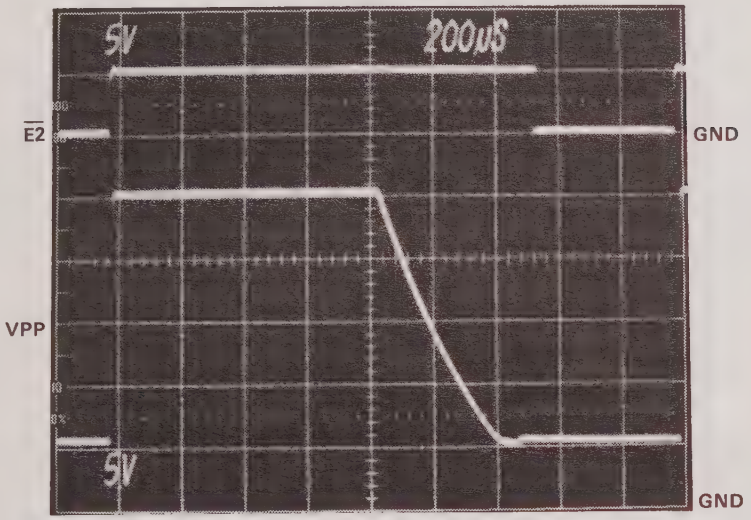


18

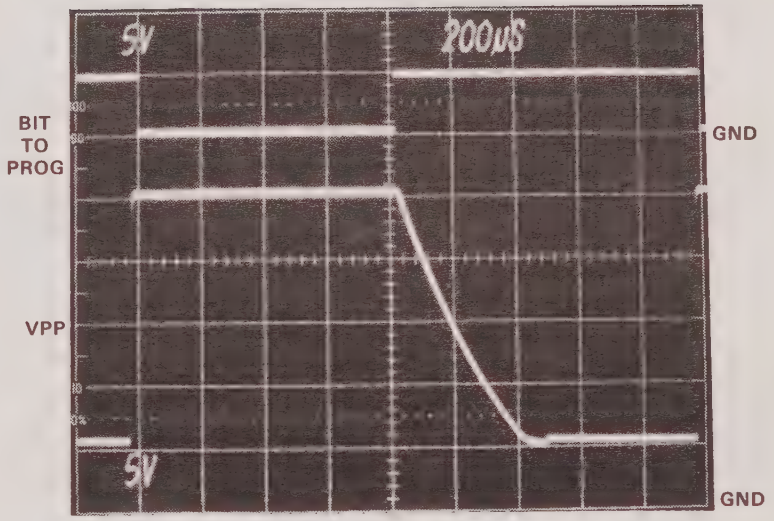
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ	11/82
		ECN #4831		ZF	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

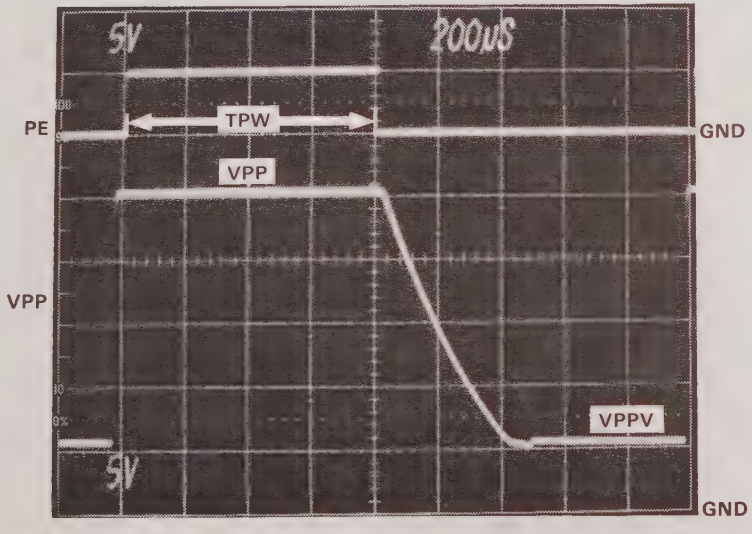
TITLE: TIMING DIAGRAM FAMILY CODES 81, 82		DRAWN BY: KC CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE:		SHEET 4/4


5V
200uS
E2
GND
VPP
5V
GND

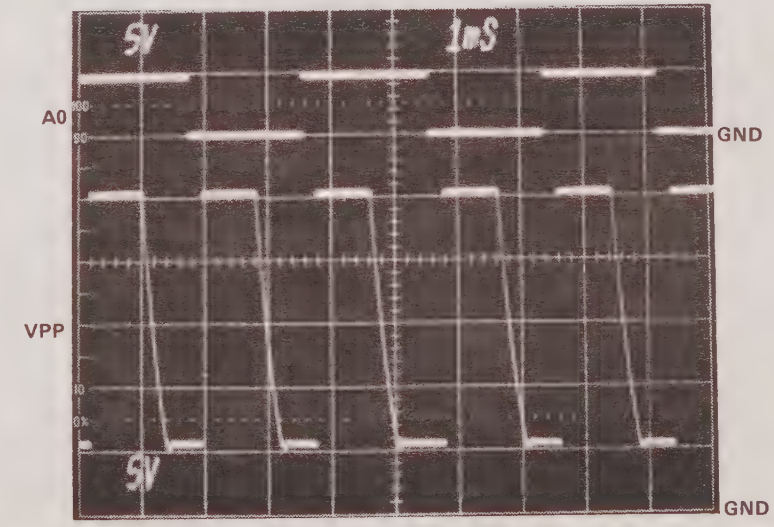
1


5V
200uS
BIT
TO
PROG
GND
VPP
5V
GND

2


5V
200uS
PE
TPW
GND
VPP
VPP
VPPV
5V
GND

3


5V
1mS
A0
GND
VPP
5V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	800			µs	
	TR	5			ns	
	TEP	1			sec	
	TF	5			ns	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 83.*
2. *Load RAM with hex 01 for Family 84, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photo 7 is the erase waveform.*

REVISIONS

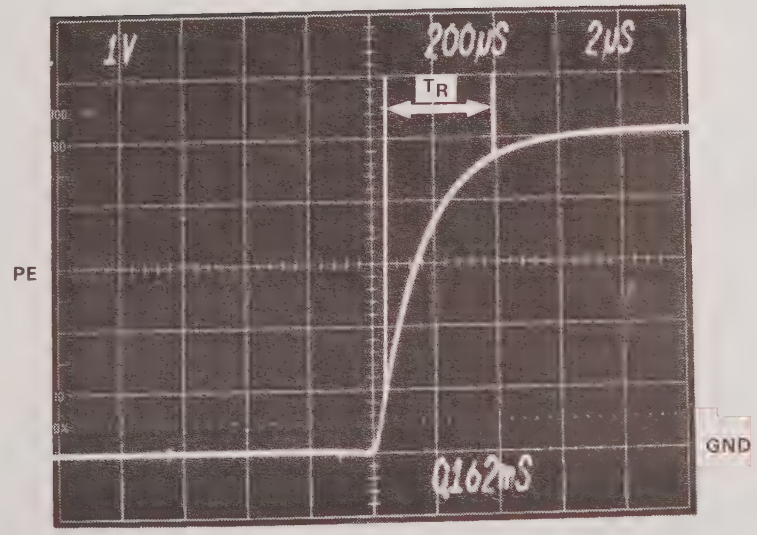
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		XH	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

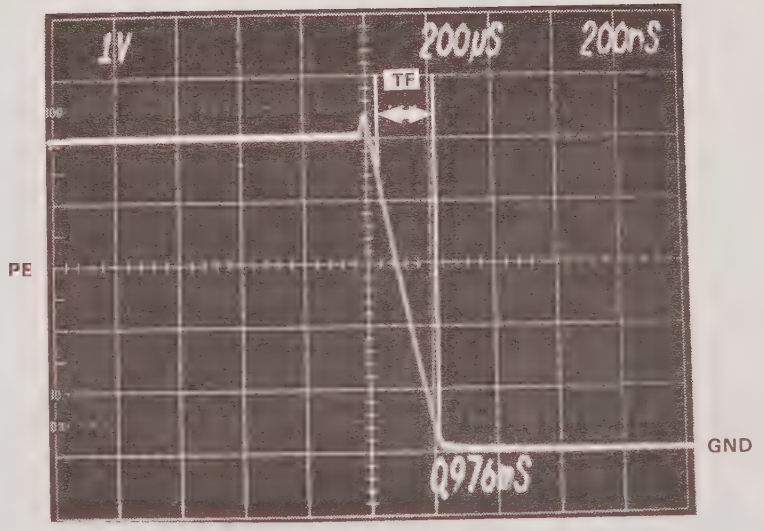
TITLE: TIMING DIAGRAM — FAMILY CODES 83, 84	DRAWN BY:
	CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

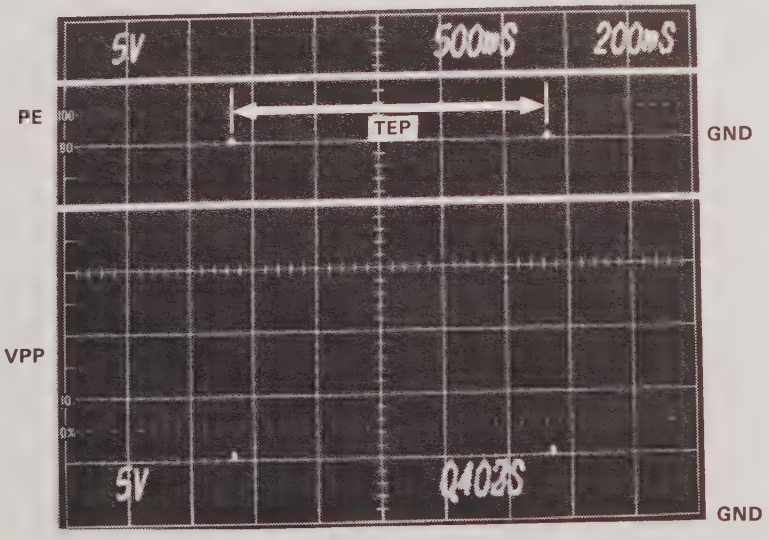
SCALE | SHEET 1/2


1V
200µS
2µS
TR
PE
GND
Q162mS

5


1V
200µS
200nS
TF
PE
GND
Q976mS

6

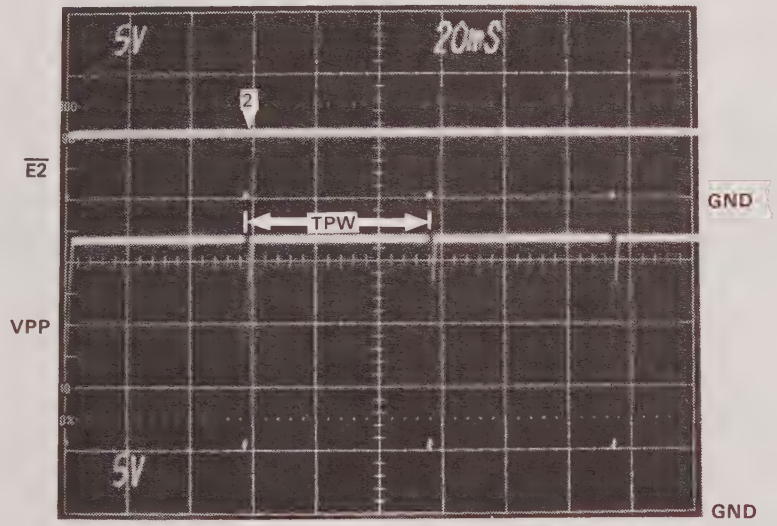

5V
500mS
200mS
PE
TEP
GND
VPP
5V
Q402S
GND

7

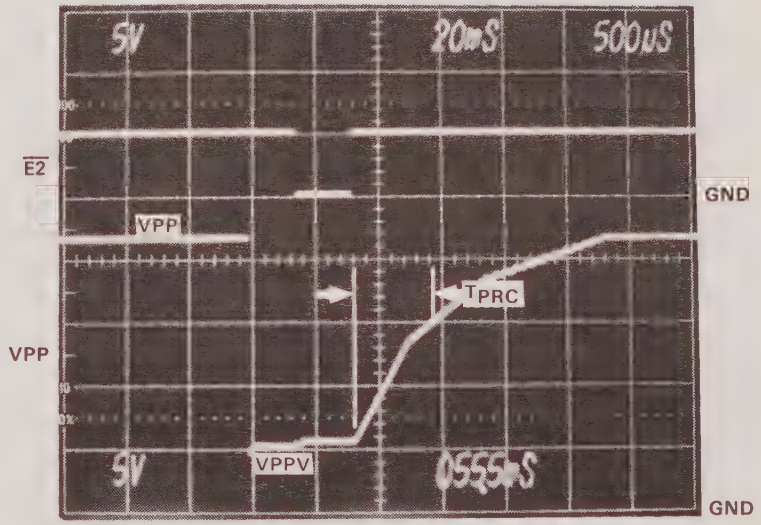
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		E.J.Z.	11/82
		ECN #4831		XX	5/83

DATA I/O ISSAQUAH, WA

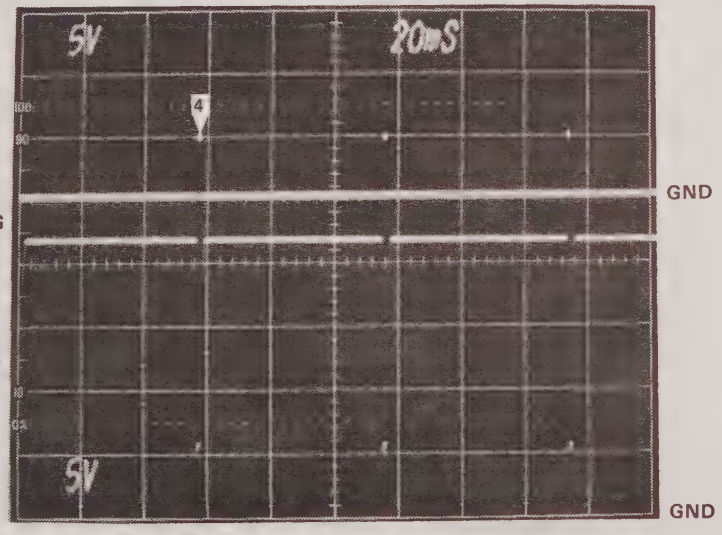
TITLE: TIMING DIAGRAM FAMILY CODES 83, 84		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2


5V
20mS
2
E2
TPW
GND
VPP
5V
GND

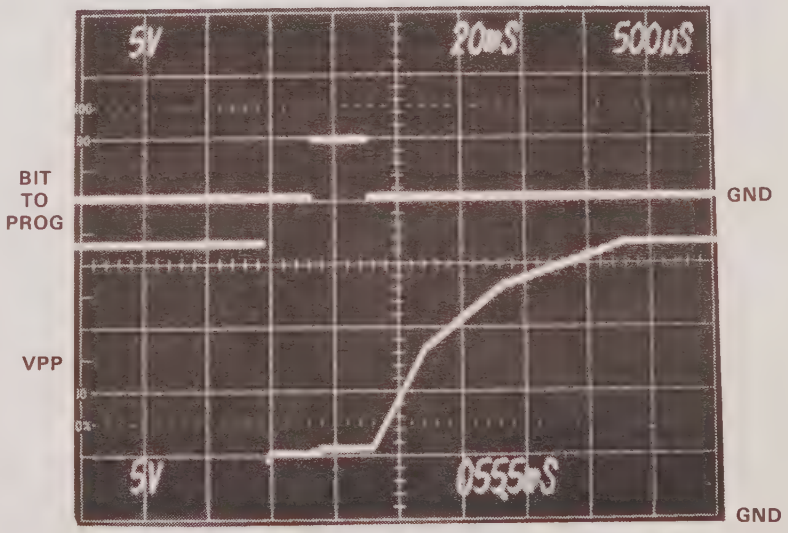
1


5V
20mS
500uS
E2
GND
VPP
TPRC
VPP
5V
VPPV
GND

2


5V
20mS
4
BIT
TO
PROG
GND
VPP
5V
GND

3


5V
20mS
500uS
BIT
TO
PROG
GND
VPP
5V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	20.0	21.0	22.0	V	
	VPPV	4.0	5.0	6.0	V	
	VEE	9.0		15.0	V	
	TPW	50		70	ms	
	T_{PRC}	450	600	750	µs	See note 3
	T_F			100	µs	
	Reject		2		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 85.*
2. *Load RAM with hex 01 for Family 86, and bit-to-prog waveform becomes bit-no-prog.*
3. *TPRC is measured from 6V to 15.5V.*
4. *Photos 8 and 9 are erase waveforms.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ.	11/82
		ECN #4831		XH	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 85, 86

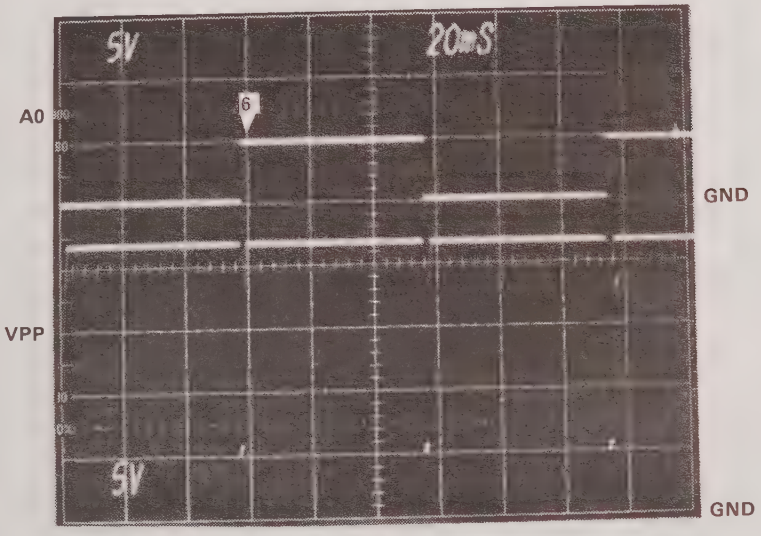
DRAWN BY:

CHECKED BY:

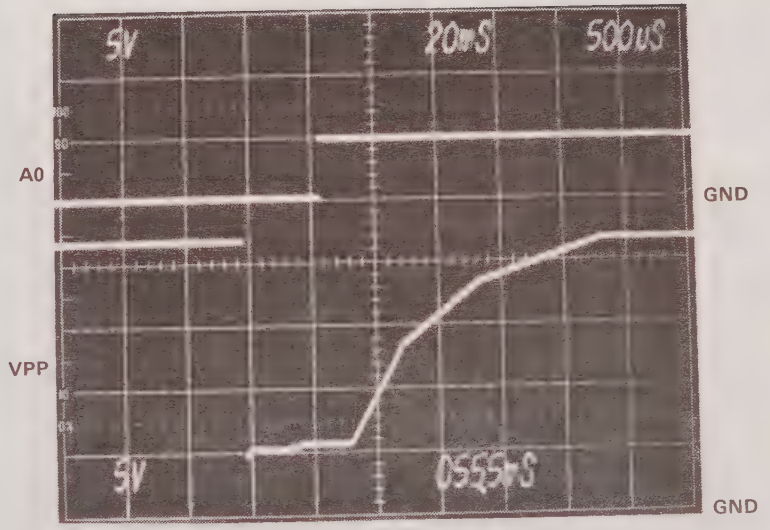
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

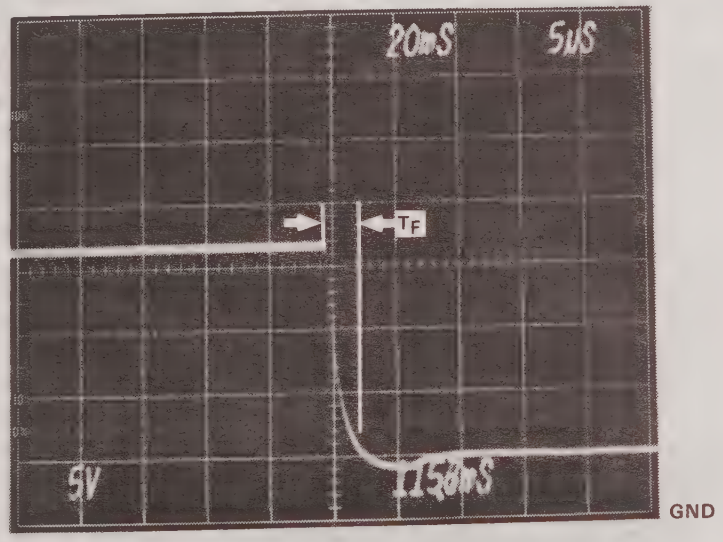
SHEET 1/2


5V
20mS
A0
6
GND
VPP
5V
GND

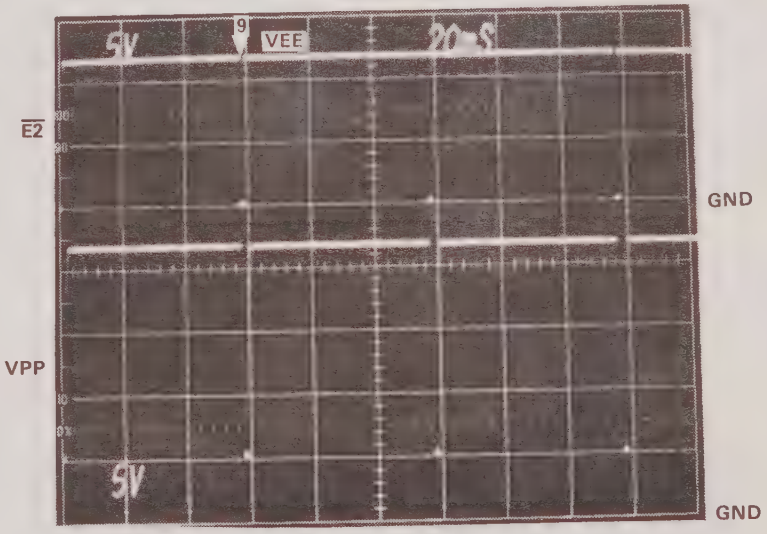
5


5V
20mS
500uS
A0
GND
VPP
5V
GND

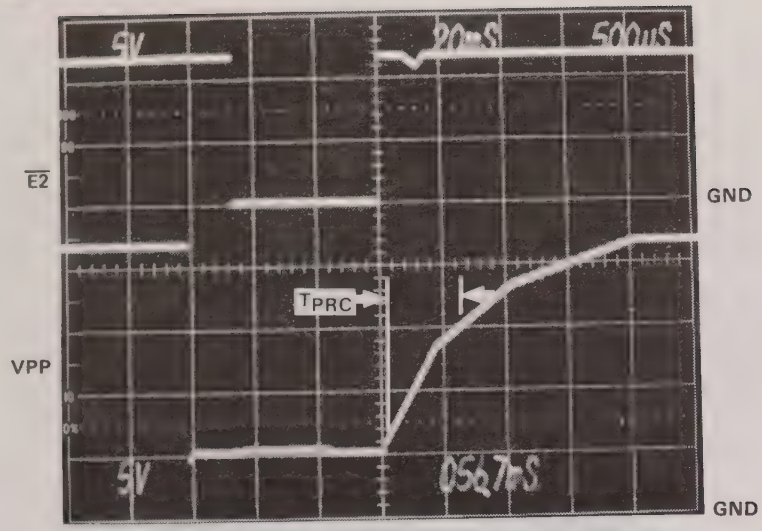
6


20mS
5uS
TF
VPP
5V
GND

7


5V
9
VEE
E2
GND
VPP
5V
GND

8



REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		XH	5/83
		ECN #5023		CTZ	3/84

DATA I/O ISSAQUAH, WA

TITLE TIMING DIAGRAM

FAMILY CODES 85, 86

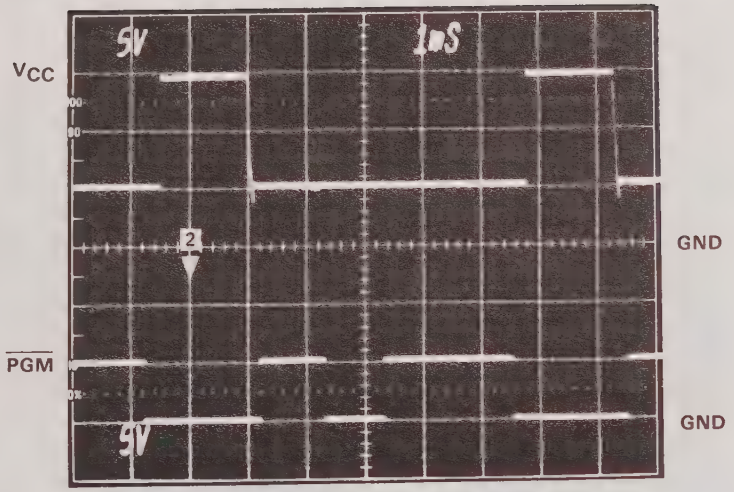
DRAWN BY: [signature]

CHECKED BY:

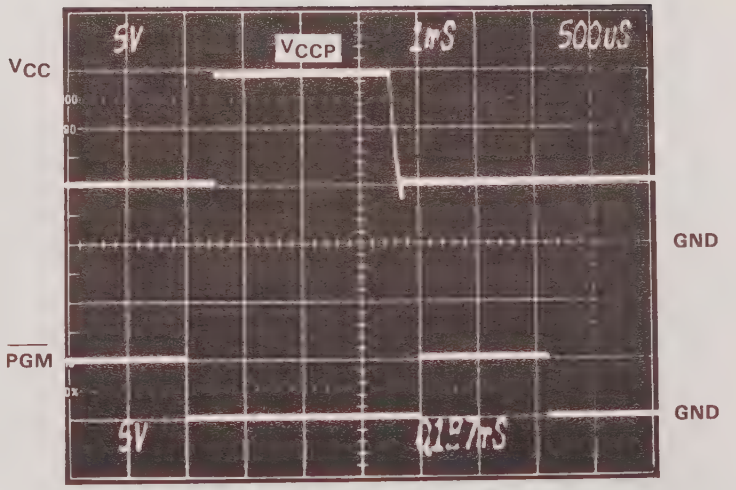
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

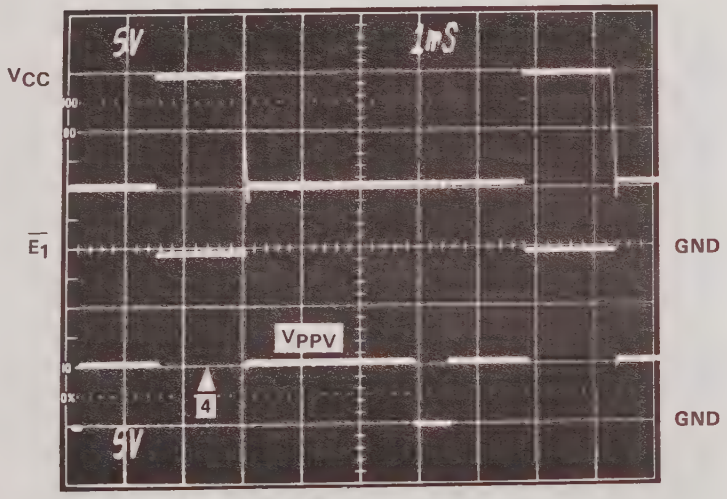
SHEET 2/2


5V
1mS
VCC
2
GND
PGM
GND
5V

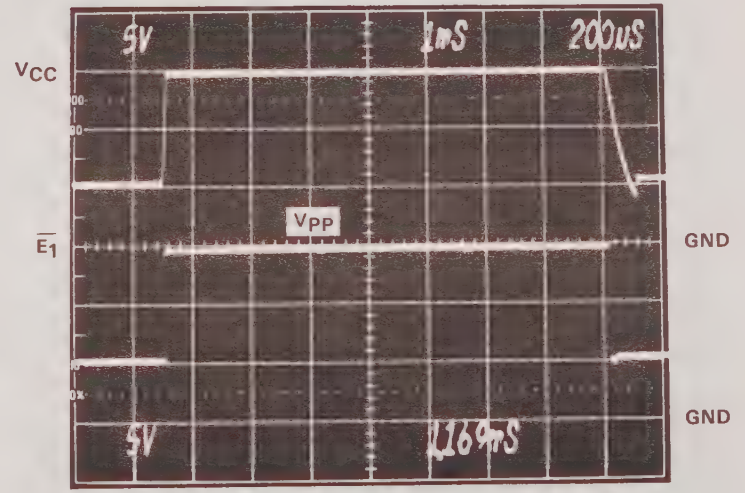
1


5V
VCCP
1mS
500uS
VCC
GND
PGM
GND
5V

2


5V
1mS
VCC
GND
E1
VPPV
4
GND
5V

3


5V
1mS
200uS
VCC
VPP
E1
GND
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	13.5	14.0	14.0	V	
	V_{OP}	12.0	14.0	14.3	V	
	V_{PP}	12.0	14.0	14.3	V	
	V_{PPV}	4.75	5.0	5.25	V	
	t_{pw}	0.9	1	1.1	ms	
	t_r					N.A.
	t_{cp}	475	500	525	μs	
	t_f					N.A.
	Reject		8		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	3.9	4.0	4.1	V	
	V_{REF}	0.3	0.4	0.5	V	701-1655/TP2
	HIGH LOAD	6.2	6.7	7.2	V	701-1655/TP4
	LOW LOAD	6.2	6.7	7.2	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.9	6.0	6.1	V	
	V_{REF}	2.3	2.4	2.5	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	7.5	8.0	8.5	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 88.*
2. *Load RAM with hex 01 for Family 87.*
3. *Photo 8 shows reject count.*

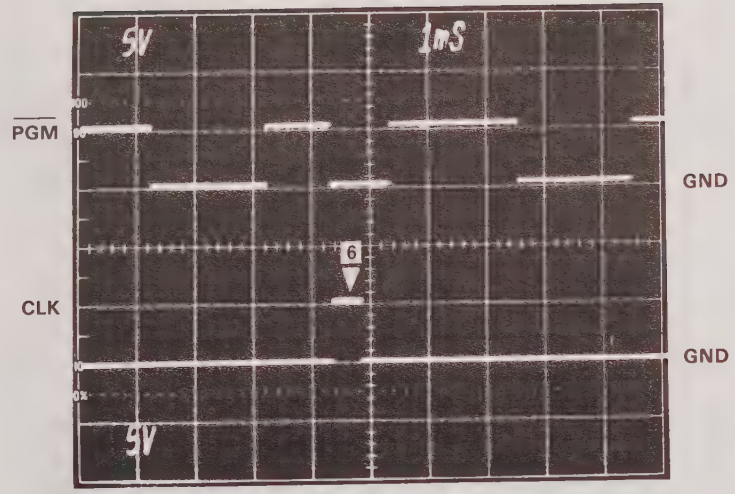
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	3/84

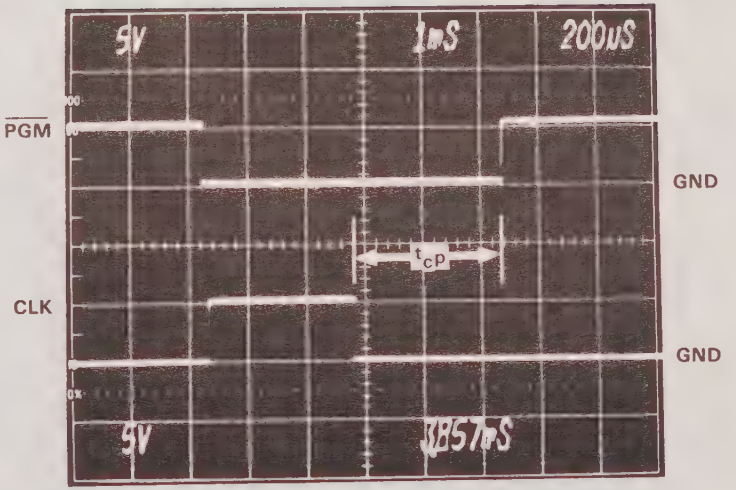
TIMING DIAGRAM

FAMILY CODES 87, 88

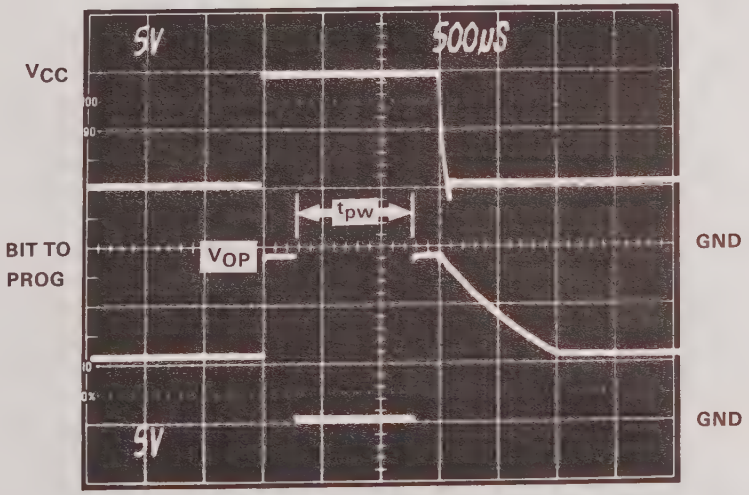
DATA I/O


5V
1mS
PGM
GND
6
CLK
GND
5V

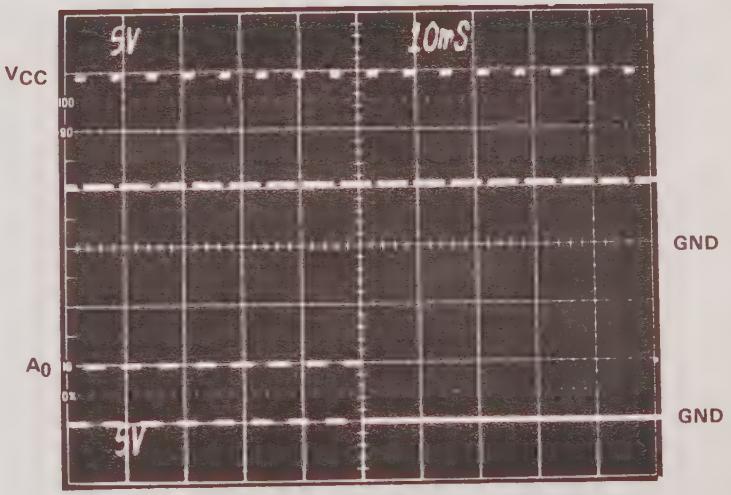
5


5V
1mS
200uS
PGM
GND
tcp
CLK
GND
5V

6


5V
500uS
VCC
tpw
BIT TO
PROG
VOP
GND
GND
5V

7


5V
10mS
VCC
GND
A0
GND
5V

8

B-183
981-0001

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	3/84

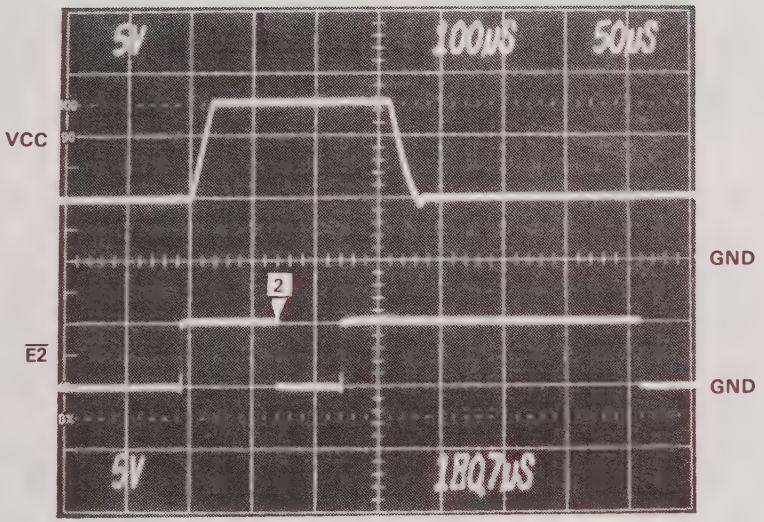
Sheet 2 of 2

TIMING DIAGRAM

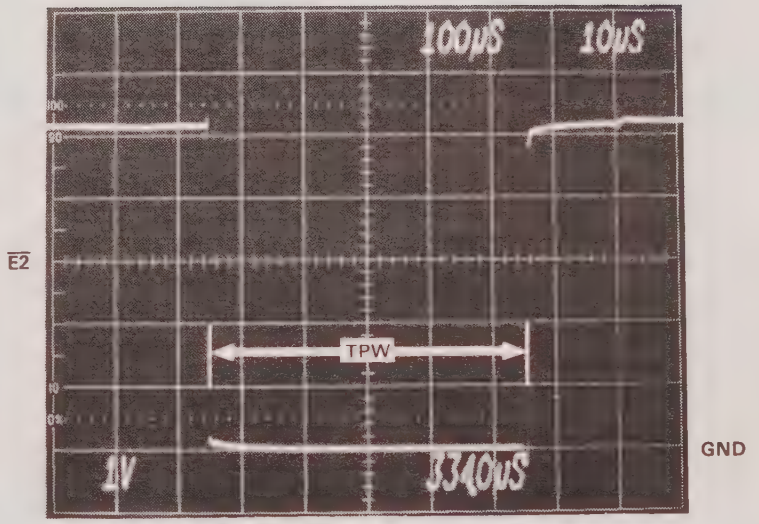
FAMILY CODES 87, 88

DATA I/O

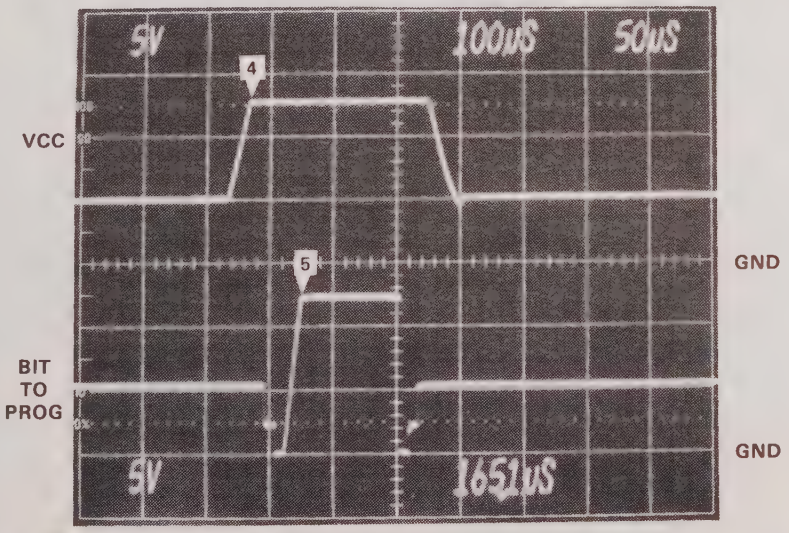
0526/1282


5V
100uS
50uS
VCC
GND
2
E2
GND
5V
1807uS

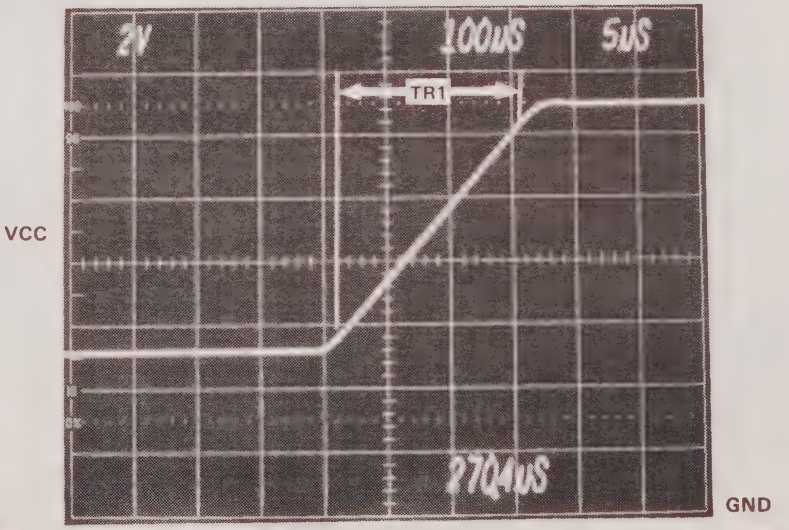
1


100uS
10uS
E2
TPW
GND
1V
3340uS

2


5V
100uS
50uS
4
VCC
GND
5
BIT
TO
PROG
GND
5V
1651uS

3


2V
100uS
5uS
TR1
VCC
GND
2704uS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	12.5	12.5	13.0	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	11.5	12.0	12.5	V	
	TPW	40	50	60	µs	
	TR1	5		20	µs	
	TR2	10		20	µs	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	0.4	0.5	0.6	V	701-1655/TP2
	High Load	17.5	18.5	19.5	V	701-1655/TP4
	Low Load	17.5	18.5	19.5	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	2.3	2.4	2.5	V	701-1655/TP2
	High Load	6.0	7.0	8.0	V	701-1655/TP4
	Low Load	6.0	7.0	8.0	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 91.*
2. *Load RAM with hex 01 for Family 92.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.F.J.	11/82
		ECN #4831		JCH	5/83
		ECN #5023		CTJ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 91, 92

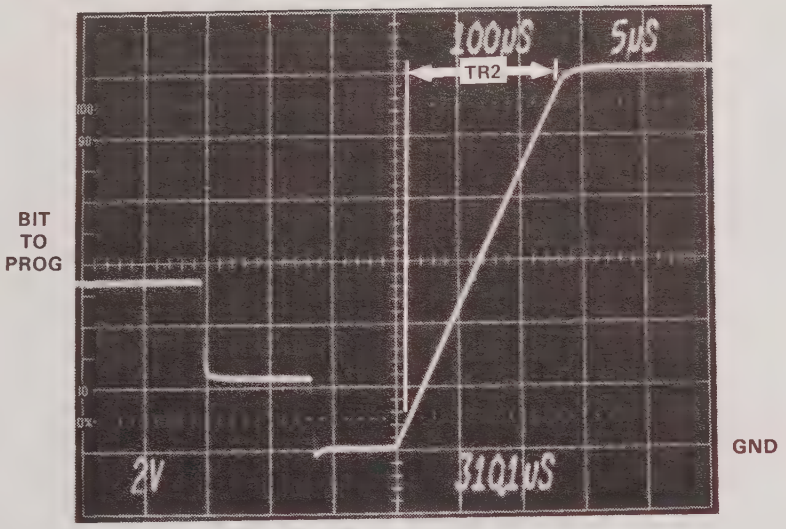
DRAWN BY:

CHECKED BY:

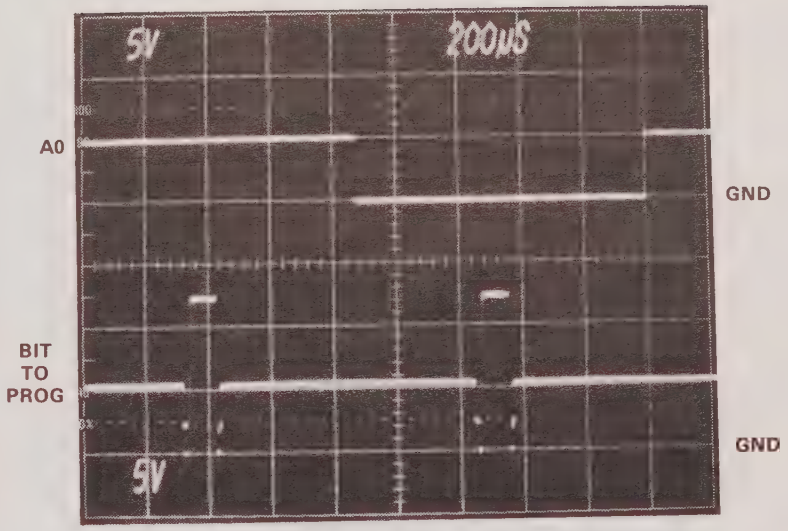
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 1/2


100uS
5uS
TR2
BIT
TO
PROG
GND
2V
310uS

5

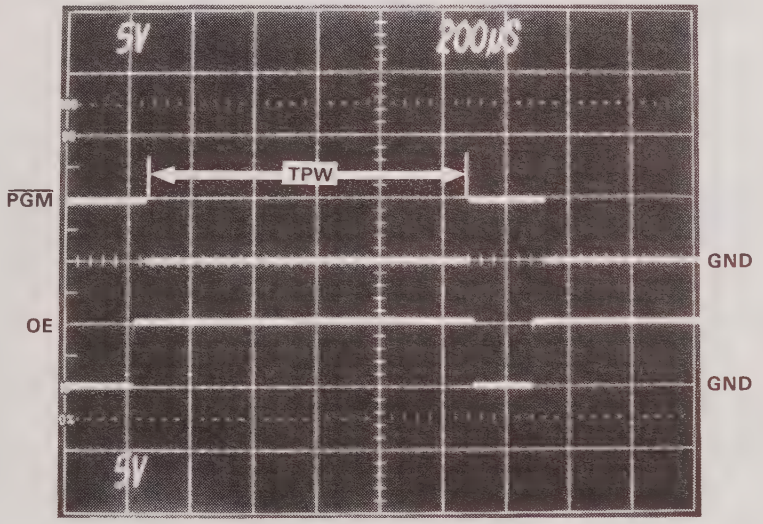

5V
200uS
A0
GND
BIT
TO
PROG
GND
5V

6

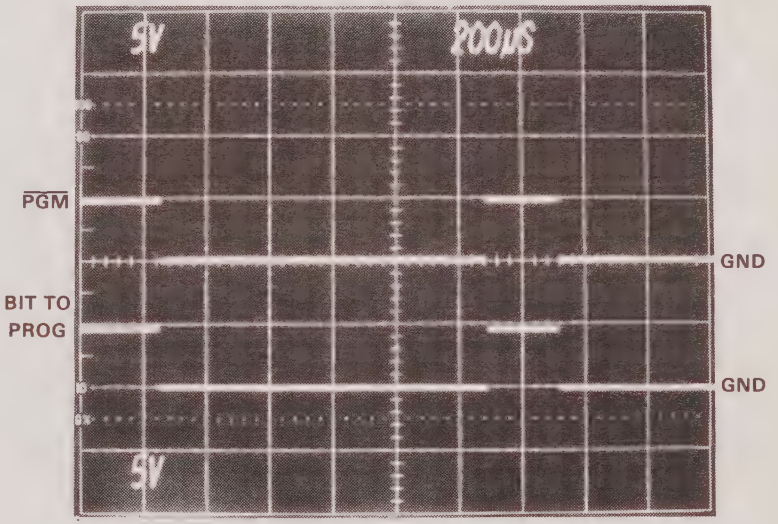
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		KR	5/83

DATA I/O ISSAQUAH, WA

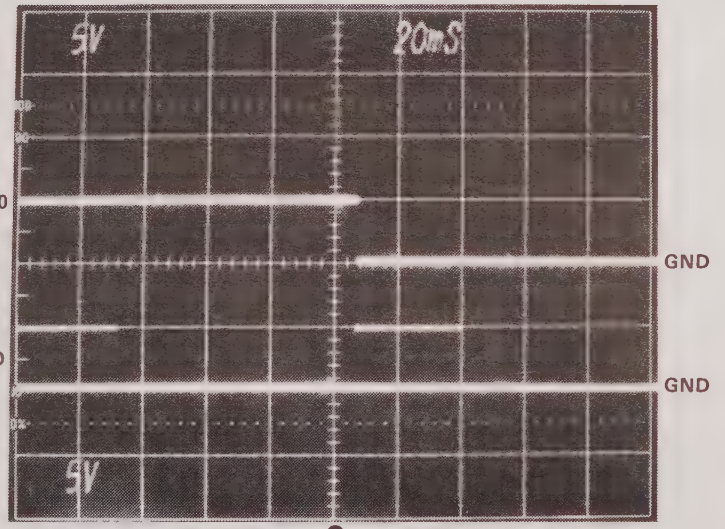
TITLE: TIMING DIAGRAM		DRAWN BY:
FAMILY CODES 91, 92		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE:		SHEET 2/2


5V
200µS
TPW
PGM
GND
OE
GND
5V

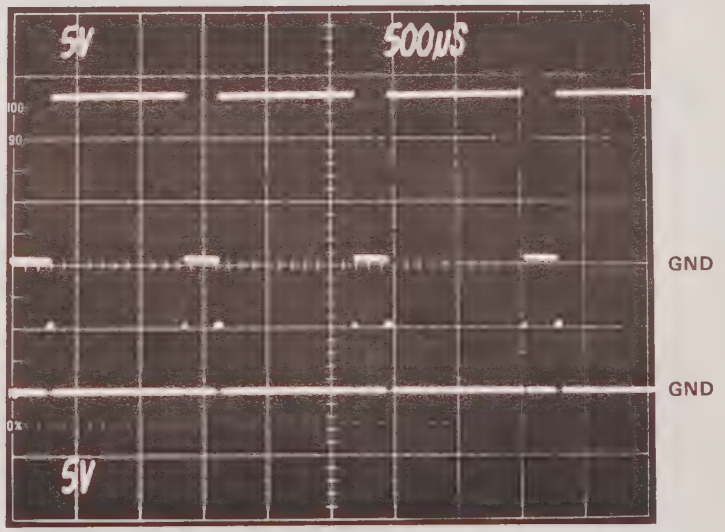
1


5V
200µS
PGM
GND
BIT TO
PROG
GND
5V

2


5V
20mS
A0
GND
BIT TO
PROG
GND
5V

3


5V
500µS
VPP
GND
PE
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.00	6.25	V	Not shown
	VOP					NA
	VPP	12.2	12.5	12.8	V	Not shown
	VPPV					NA
	TPW	0.95	1.0	1.05	ms	
	TR					NA
	TF					NA
	Reject		25		Pulses	
	Overprogram		1		Pulse	See note 3
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

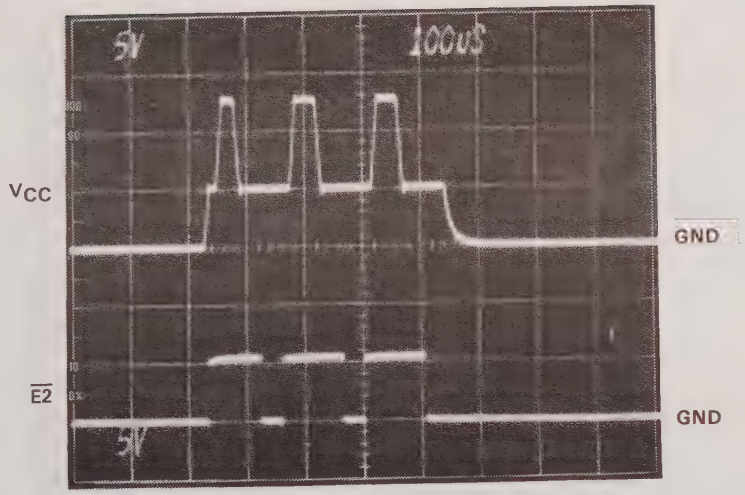
1. *Load RAM with hex FE for Family 93.*
2. *Load RAM with hex 01 for Family 94, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The overprogram pulse is 3 ms times the number of programming pulses required to program the location.*
4. *Photo 4 is for Pinout 24.*

REVISIONS

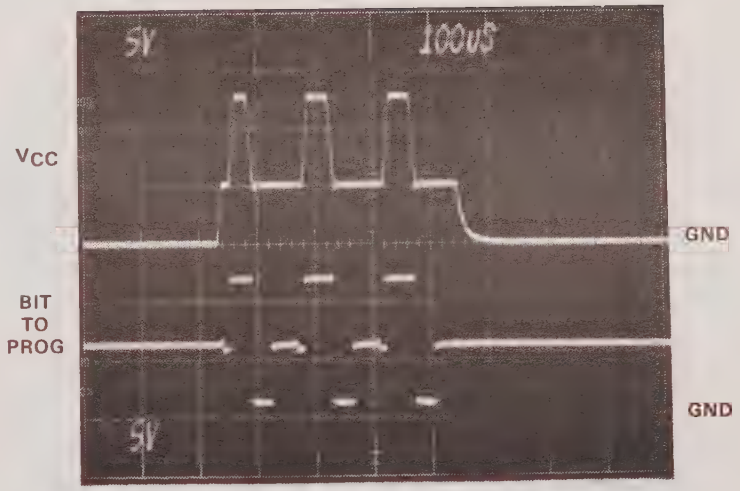
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		XH	5/83
		ECN #5023		CTZ	3/84

DATA I/O

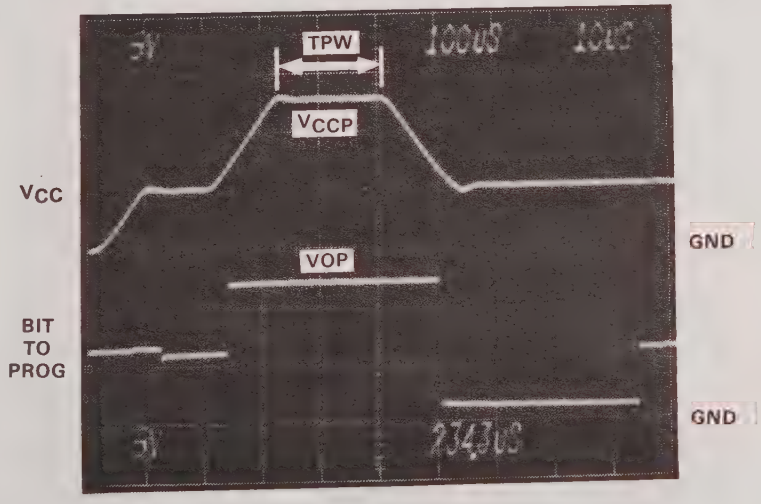
TITLE: TIMING DIAGRAM FAMILY CODES 93, 94		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 1


5V
100uS
VCC
GND
E2
GND
5V

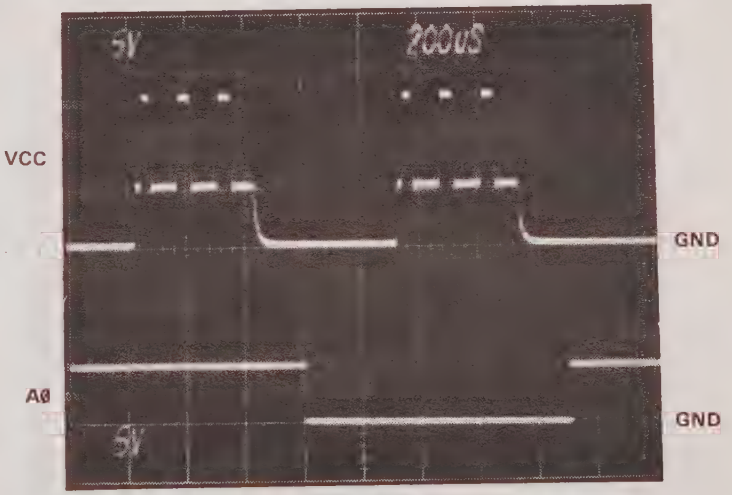
1


5V
100uS
VCC
GND
BIT
TO
PROG
GND
5V

2


5V
TPW
100uS
10uS
VCCP
VCC
GND
VOP
BIT
TO
PROG
GND
5V
734uS

3


5V
200uS
VCC
GND
A0
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	12.0	12.5	13.0	V	
	V_{OP}	11.5	12.0	12.5	V	
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	10		22	μs	See Note 5
	t_r					N.A.
	t_f					N.A.
	Reject		3		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	V_{CC}	4.4	4.5	4.6	V	
	V_{REF}	0.7	0.8	0.9	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	16.9	17.4	17.9	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.4	5.5	5.6	V	
	V_{REF}	2.3	2.4	2.5	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	18.5	19.0	19.5	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family A1.*
2. *Load RAM with hex 01 for Family A2.*
3. *Load V_{CC} with 100Ω, 2W resistor.*
4. *Load "Bit to Program" with 3.3KΩ, ¼-W resistor.*
5. *First pulse TPW equals 10-22 μs; pulses 2 and 3 are equal to 20-32 μs.*

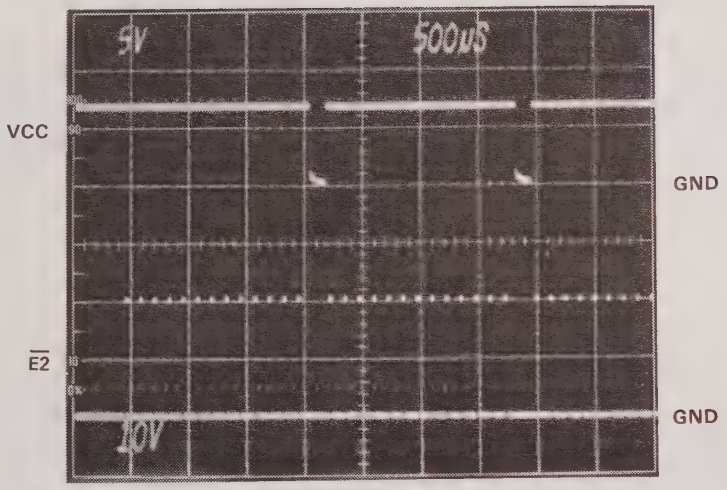
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	3/84

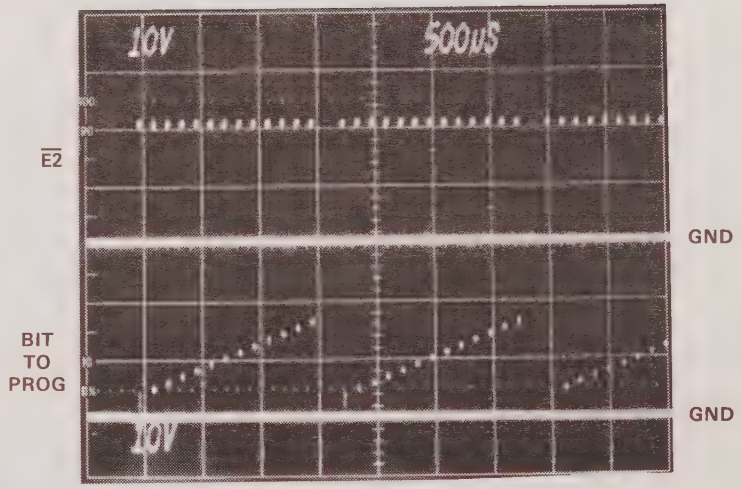
TIMING DIAGRAM

FAMILY CODES A1, A2

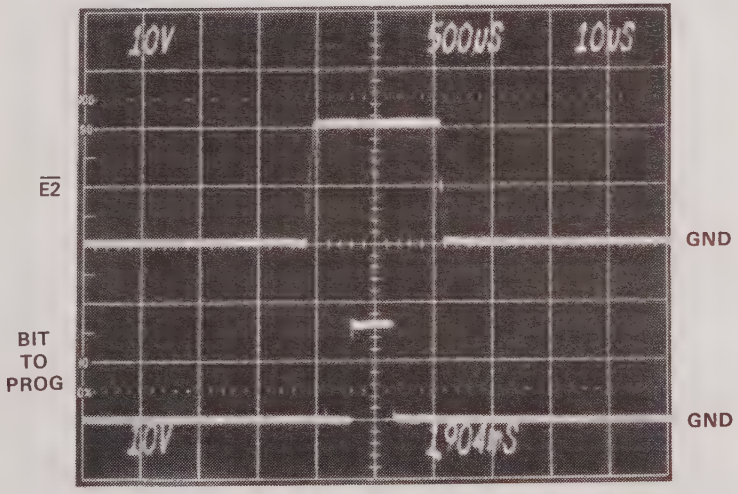
DATA I/O


5V
500uS
VCC
GND
E2
GND
10V

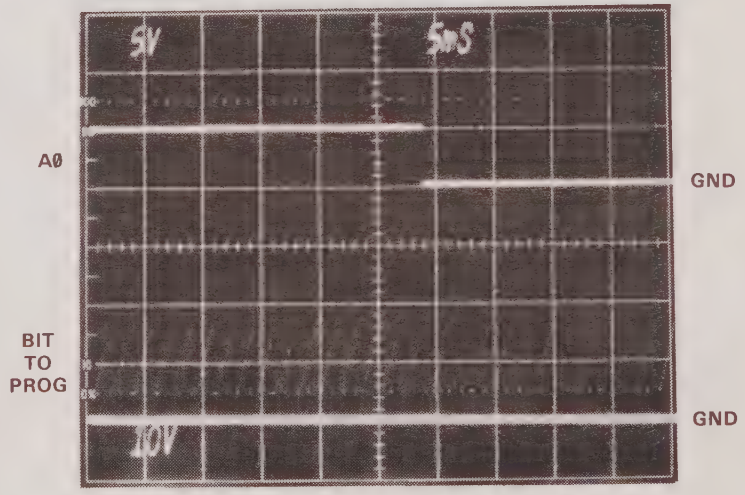
1


10V
500uS
E2
GND
BIT
TO
PROG
GND
10V

2


10V
500uS
10uS
E2
GND
BIT
TO
PROG
GND
10V

3


5V
5mS
A0
GND
BIT
TO
PROG
GND
10V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	6.3	6.5	6.7	V	
	VPP	19.5	20.0	20.5	V	
	VOP max	15.5	16.0	16.5	V	See Note 4
	VOP min	3.5	4.0	4.5	V	See Note 4
	TPW	6.5	7.0	7.5	μs	See Note 5
	Reject		16		Series	See Note 6
	Overprogram		1		Pulse	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	1.4	1.5	1.6	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.4	V	701-1655/TP4
	LOW LOAD	17.2	18.2	19.2	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	1.4	1.5	1.6	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.4	V	701-1655/TP4
	LOW LOAD	17.2	18.2	19.2	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family A3.*
2. *Load RAM with hex 01 for Family A4*
3. *Load VCC with a 100Ω, 2-watt resistor.*
4. *01 is loaded with a 100Ω, 2-watt resistor. A series of program pulses is applied. The program pulses begin at VOP min. and increase in magnitude to VOP max. or until the bit programs.*
5. *TPW is measured using the tallest pulse of the series.*
6. *Reject count is 16 program pulse series.*

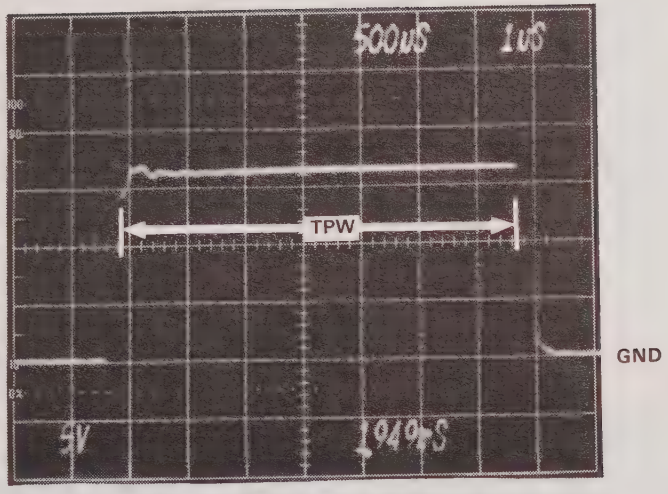
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

TIMING DIAGRAM

FAMILY CODES A3, A4

DATA I/O



5

REVISIONS

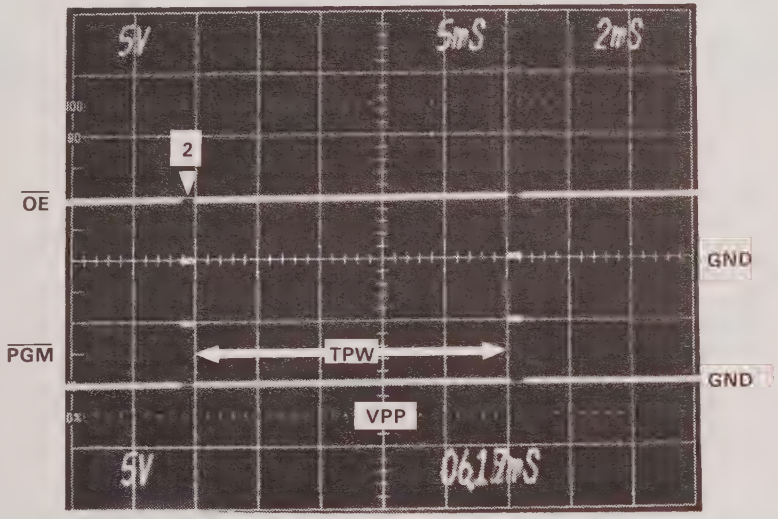
LTR	DESCRIPTION	P.E.	DATE

Sheet 2 of 2

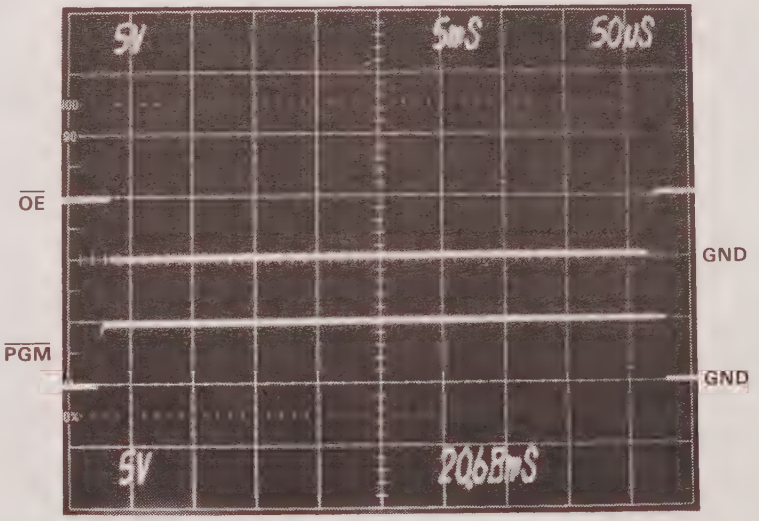
TIMING DIAGRAM

FAMILY CODES A3, A4

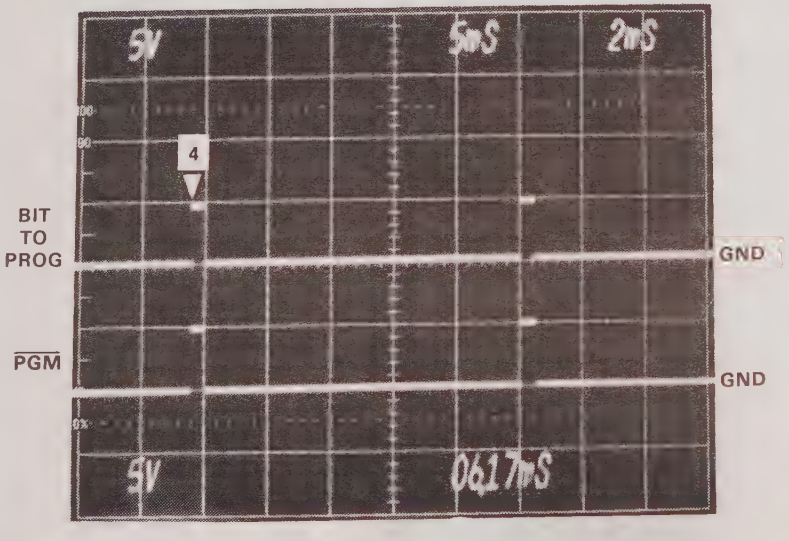
DATA I/O

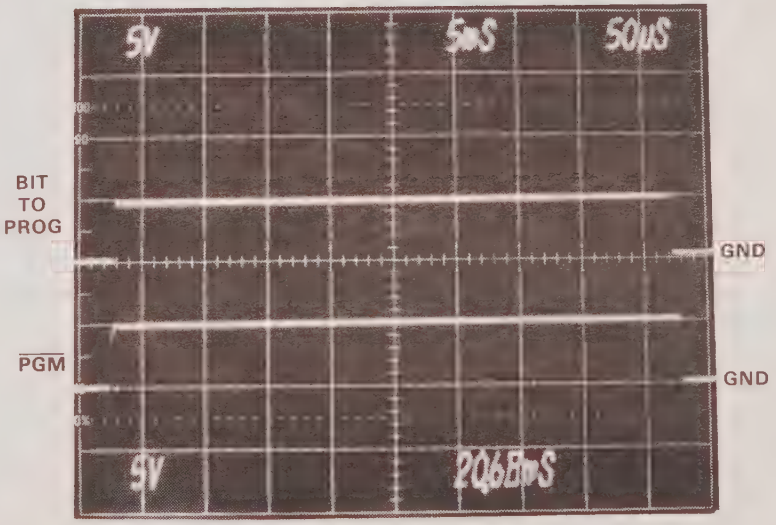

5V
5mS
2mS
2
OE
GND
PGM
TPW
GND
VPP
5V
0613mS

1


5V
5mS
50uS
OE
GND
PGM
GND
5V
2Q6BmS

2


5V
5mS
2mS
4
BIT
TO
PROG
GND
PGM
GND
5V
0617mS


5V
5mS
50uS
BIT
TO
PROG
GND
PGM
GND
5V
2Q6BmS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.5	5.0	5.5	V	
	VPP	0.0	0.0	0.8	V	
	VEE	12.0	14.5	21.0	V	
	TPW	5.0	10.0	15.0	ms	
	TR				NA	
	TF				NA	
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.7	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.5	5.5	6.5	V	701-1655/TP4
	Low Load	4.5	5.5	6.5	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	6.8	7.8	8.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family A5.*
2. *Load RAM with hex 01 for Family A6, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photos 6 and 7 are erase waveforms.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.J.	11/82
		ECN #4831		JH	5/83
		ECN #5023		CJJ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES A5, A6

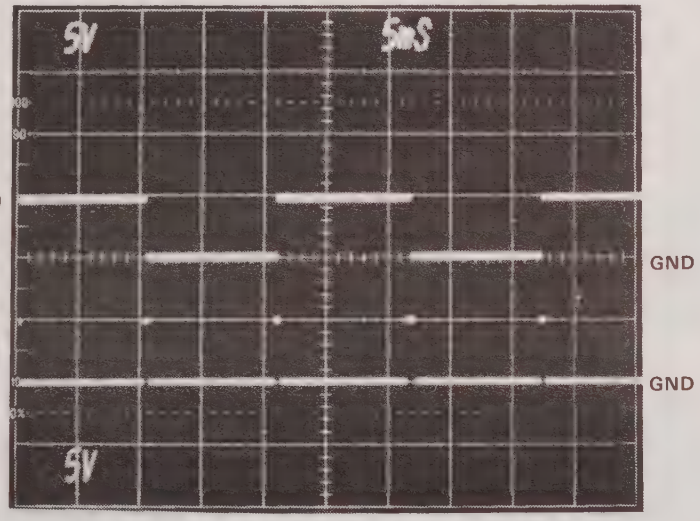
DRAWN BY:

CHECKED BY: JH

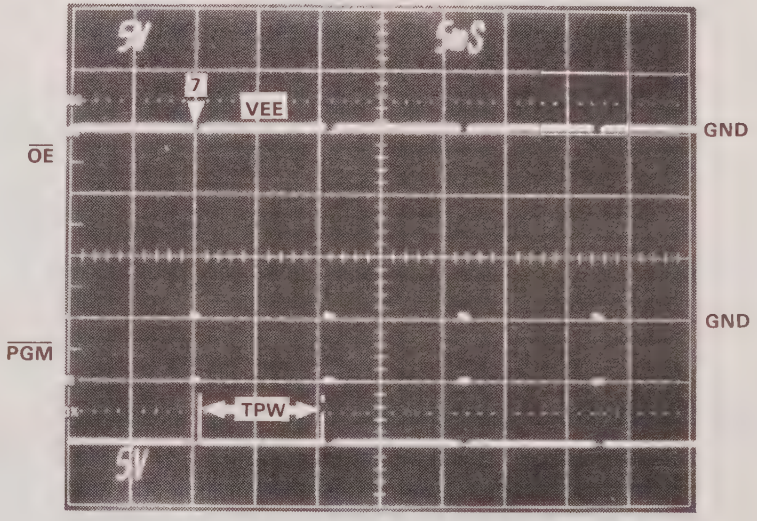
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

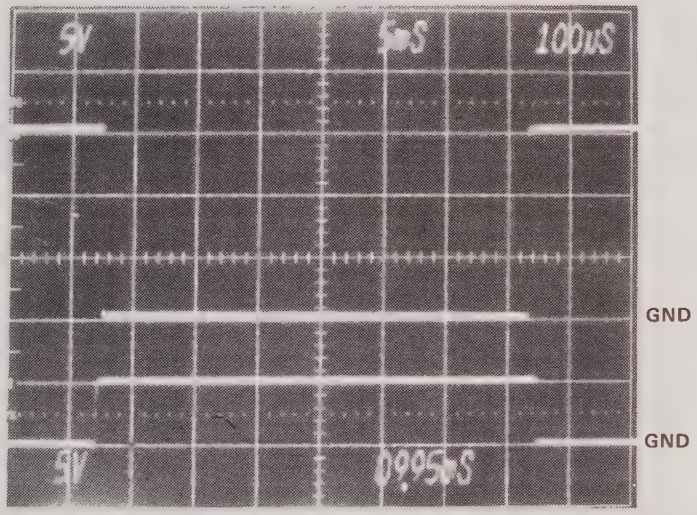
SHEET 1/2


5V
5mS
A0
GND
PGM
GND
5V

5


5V
5mS
7
VEE
GND
OE
GND
PGM
TPW
5V

6

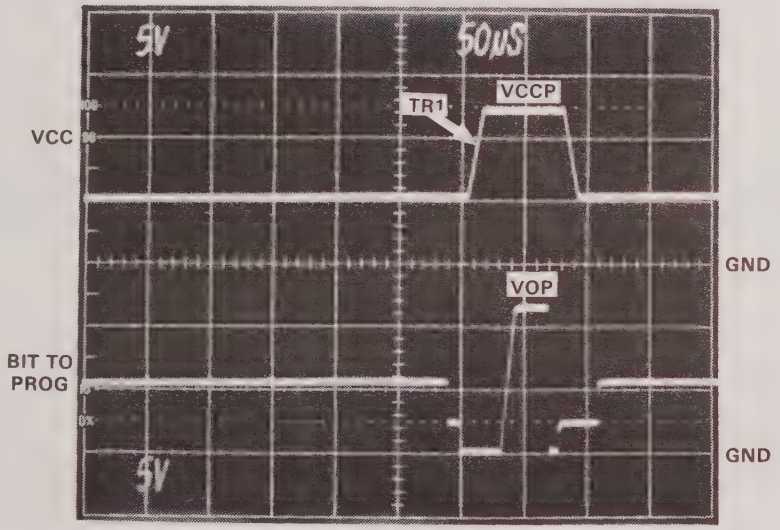

5V
5mS
100uS
OE
GND
PGM
GND
5V
0.995mS

7

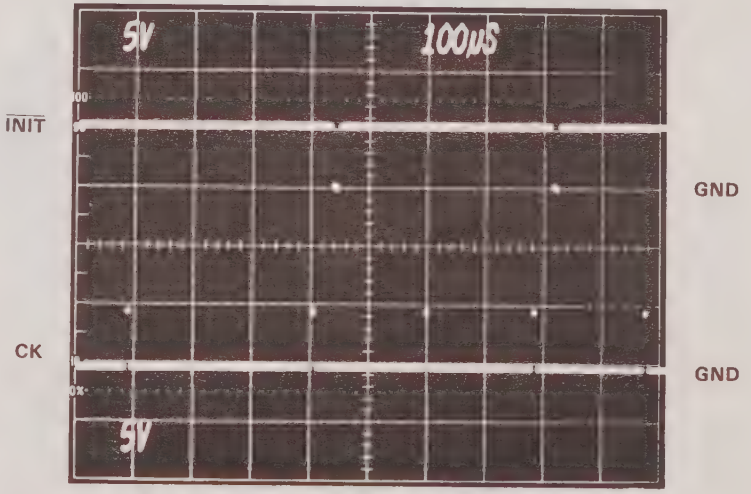
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.73	11/82
		ECN #4831		XX	5/83
		ECN #5023		C7Z	3/84

DATA I/O ISSAQUAH, WA

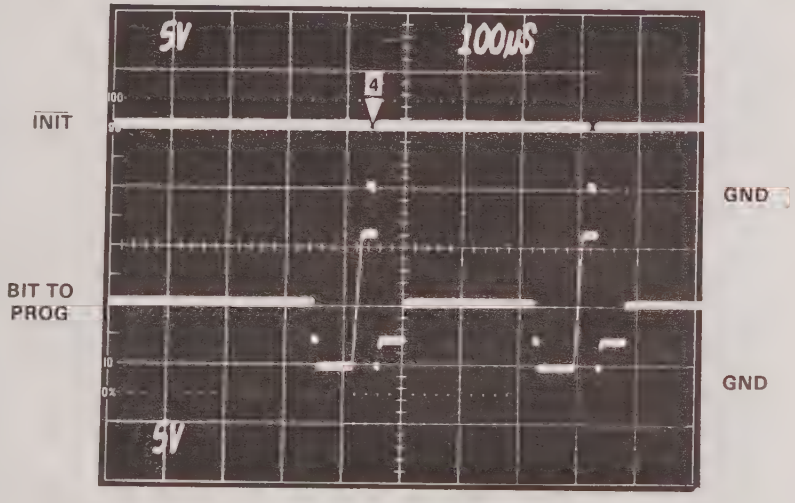
TITLE: TIMING DIAGRAM FAMILY CODES A5, A6		DRAWN BY: kee CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2


5V
50µS
VCC
TR1
VCCP
GND
VOP
BIT TO PROG
GND
5V

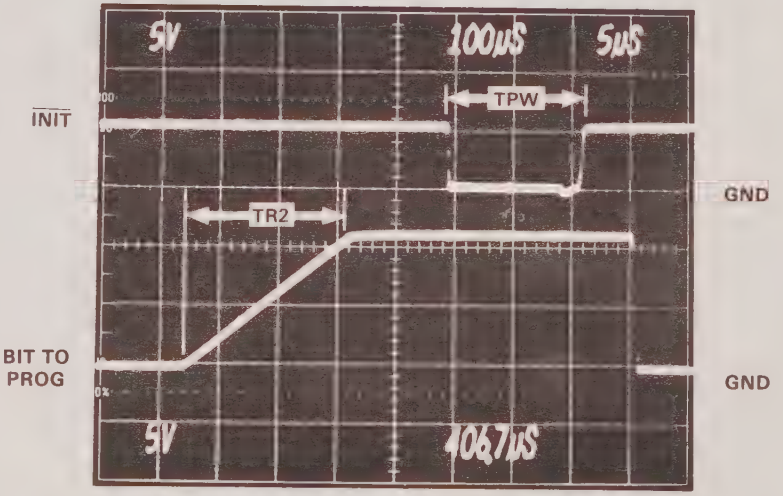
1


5V
100µS
INIT
GND
CK
GND
5V

2


5V
100µS
4
INIT
GND
BIT TO PROG
GND
5V

3


5V
100µS
5µS
TPW
INIT
GND
TR2
BIT TO PROG
GND
5V
1067µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	11.6	11.8	12.0	V	
	VOP	10.5	11.0	11.5	V	
	VPP					NA
	VPPV					NA
	TPW	9.0	10.0	11.5	µs	
	TR1	1.0		20.0	µs	See note 3
	TR2	1.0		15.0	µs	
	TF					NA
	Reject		10		Pulses	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.1	4.2	4.3	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	7.0	8.0	9.0	V	701-1655/TP4
	Low Load	7.0	8.0	9.0	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	3.4	3.5	3.6	V	701-1655/TP2
	High Load	8.3	9.3	10.3	V	701-1655/TP4
	Low Load	8.3	9.3	10.3	V	701-1655/TP3

NOTES

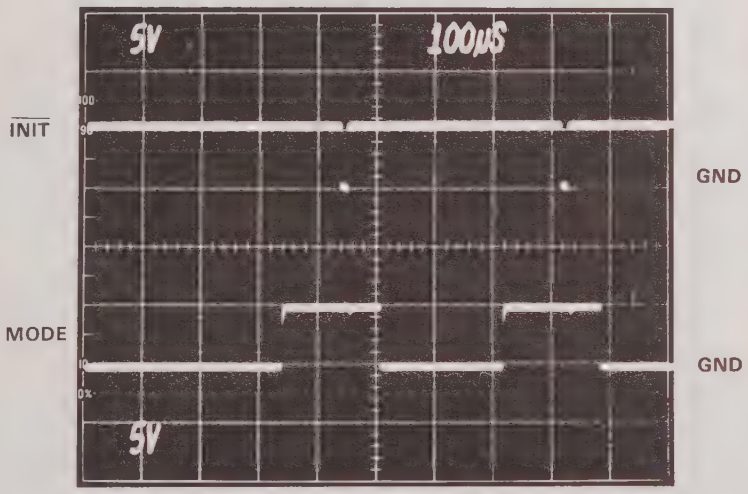
1. *Load RAM with hex FE for Family A9.*
2. *Load RAM with hex 01 for Family AA.*
3. *Load V_{CC} with a 330 Ω, ½-watt resistor.*

REVISIONS

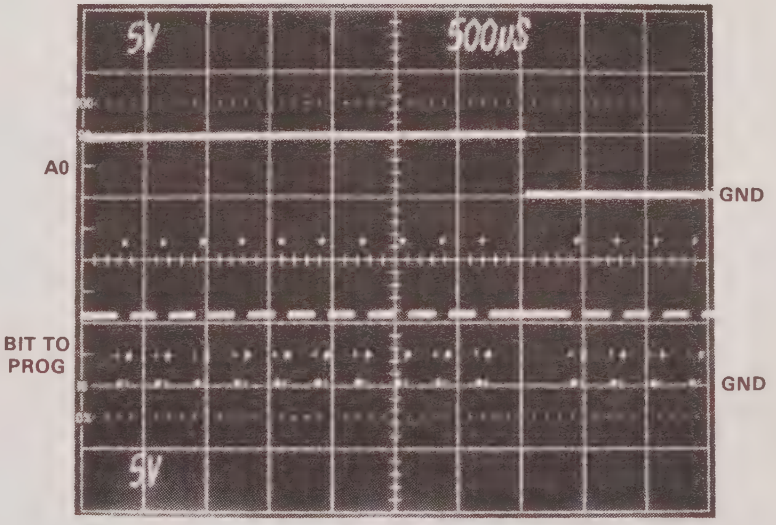
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		YH	5/83
		ECN #5023		CTJ	3/84

DATA I/O

TITLE: TIMING DIAGRAM — FAMILY CODES A9, AA		DRAWN BY:
		CHECKED BY: YH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 2



5

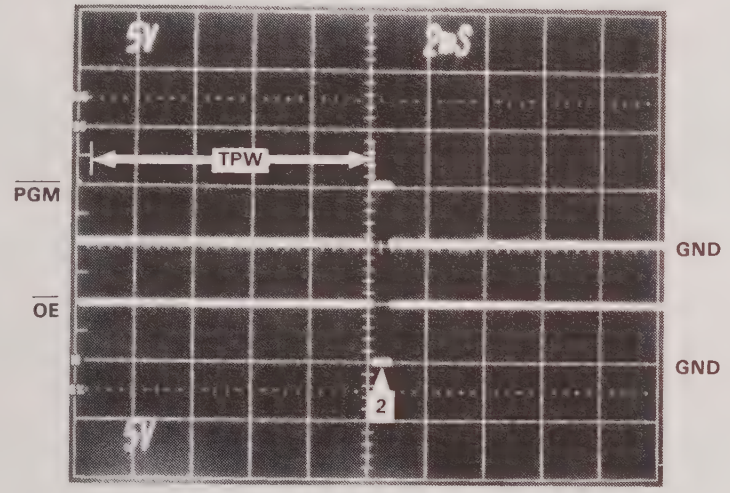


6

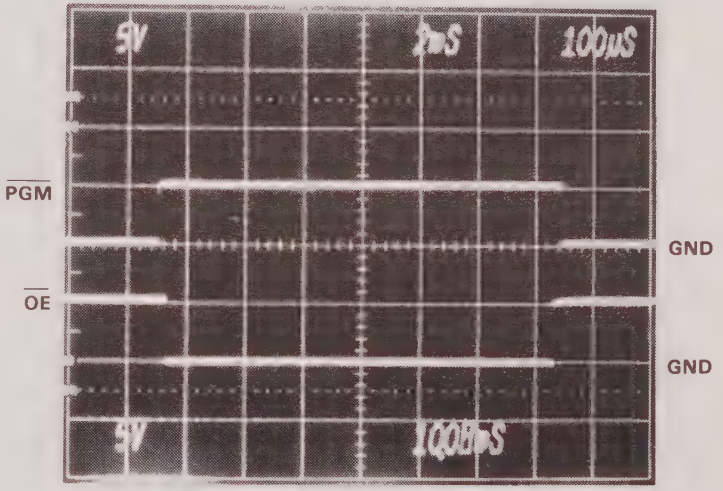
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		24	5/83
		ECN #5023		C78	3/84

DATA I/O

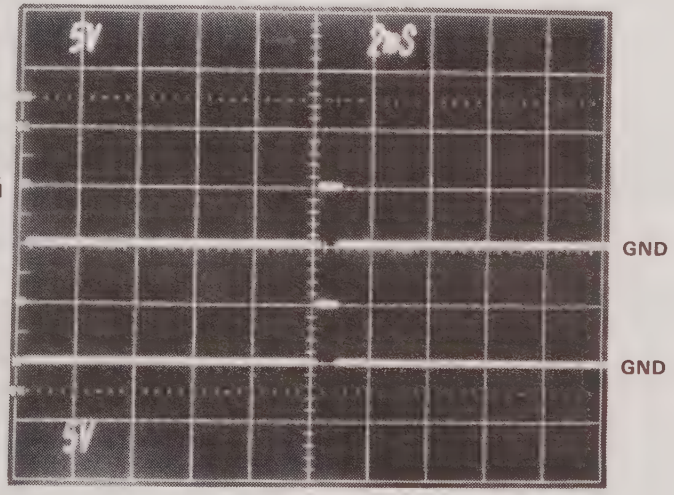
TITLE: TIMING DIAGRAM FAMILY CODES A9, AA		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2


5V
2mS
TPW
PGM
GND
OE
GND
2
5V

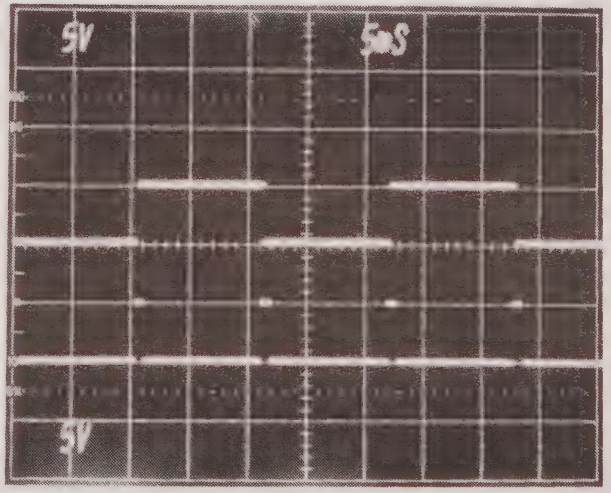
1


5V
2mS
100µS
PGM
GND
OE
GND
5V
100mS

2


5V
2mS
PGM
GND
BIT
TO
PROG
GND
5V

3


5V
5mS
AO
GND
PGM
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	9.5	10.0	10.5	ms	
	t_r					N.A.
	t_{ew}	9.5	10.0	10.5	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	5.0	5.5	6.0	V	701-1655/TP4
	LOW LOAD	5.0	5.5	6.0	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	7.3	7.8	8.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family AB.*
2. *Photos 5 to 8 are chip erase waveforms.*

REVISIONS

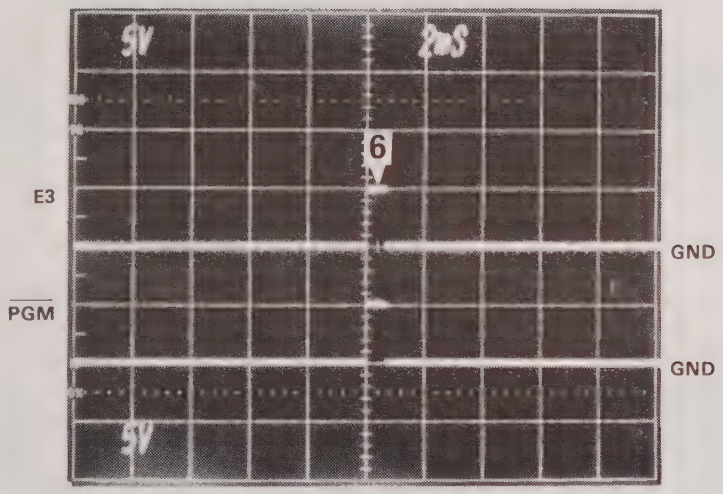
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	C73	3/84

Sheet 1 of 2

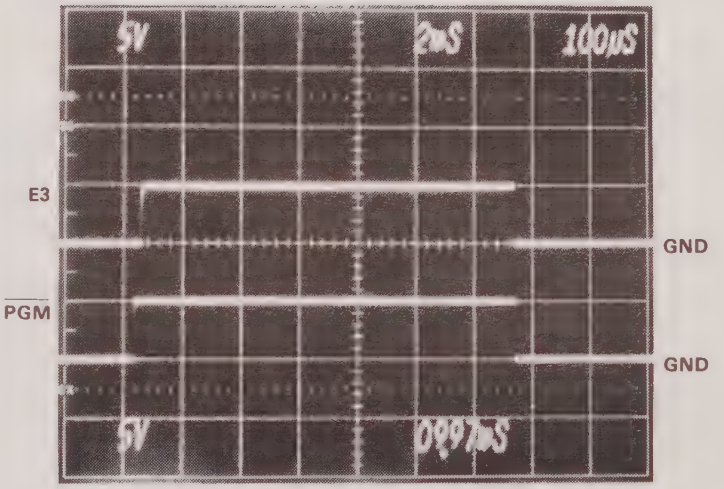
TIMING DIAGRAM

FAMILY CODES AB, AC

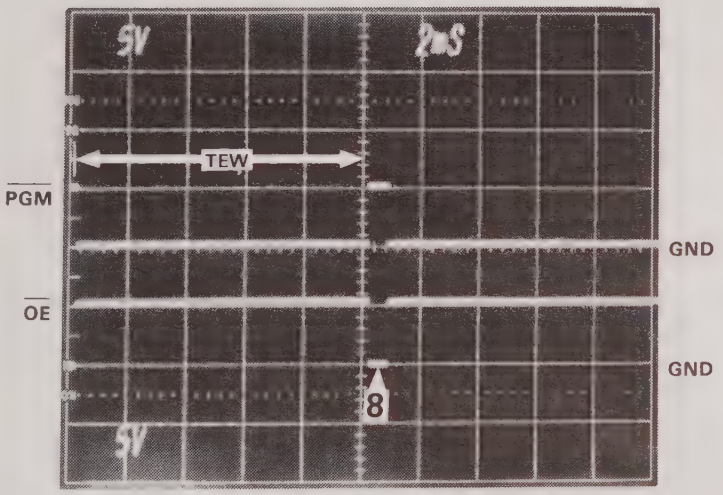
DATA I/O


5V
2mS
6
E3
GND
PGM
GND
5V

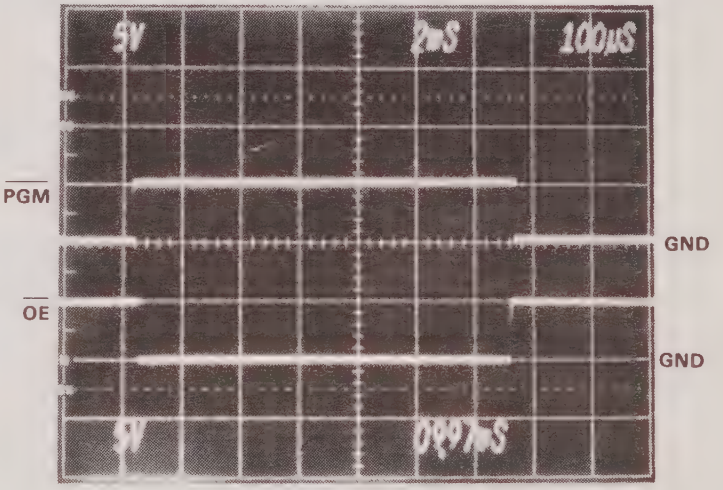
5


5V
2mS
100µS
E3
GND
PGM
GND
5V

6


5V
2mS
TEW
PGM
GND
OE
GND
8
5V

7


5V
2mS
100µS
PGM
GND
OE
GND
5V

8

REVISIONS

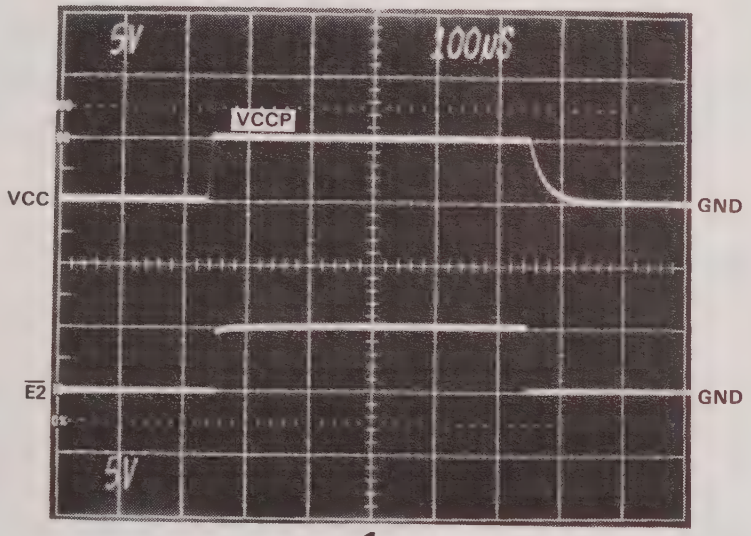
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

Sheet 2 of 2

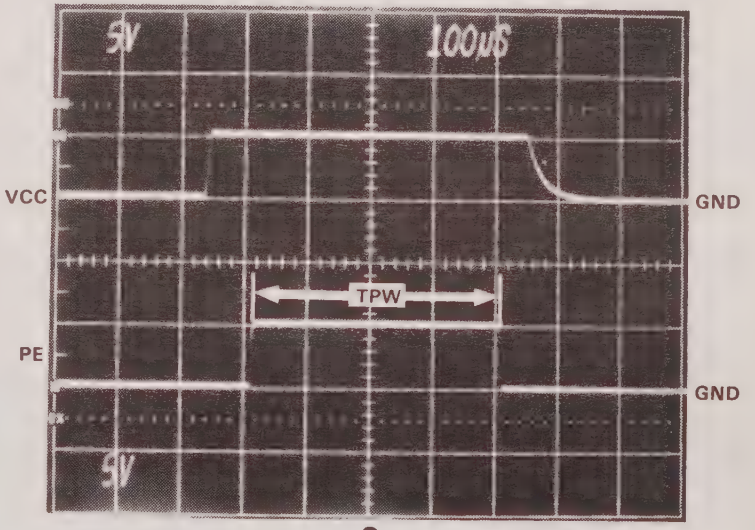
TIMING DIAGRAM

FAMILY CODES AB, AC

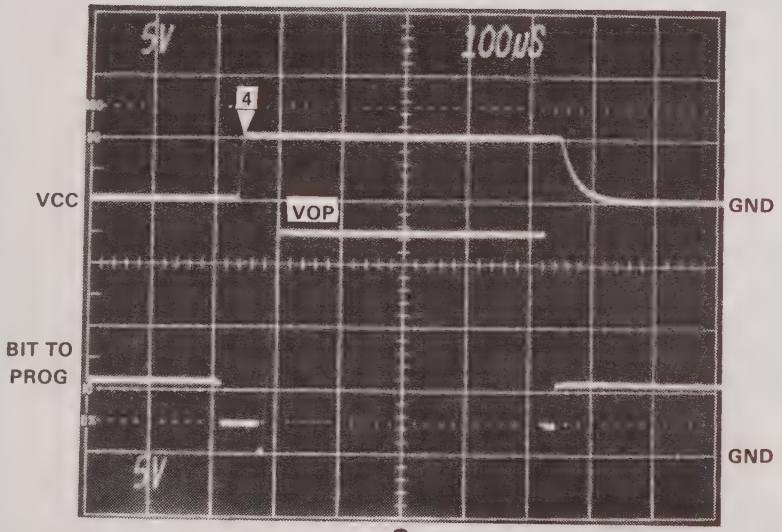
DATA I/O


5V
100uS
VCCP
VCC
GND
E2
GND
5V

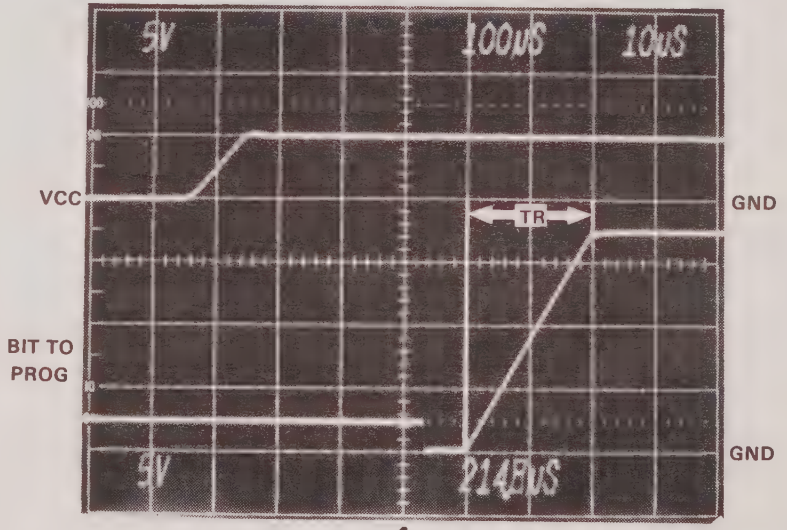
1


5V
100uS
VCC
GND
TPW
PE
GND
5V

2


5V
100uS
4
VCC
VOP
GND
BIT TO
PROG
GND
5V

3


5V
100uS
10uS
VCC
GND
TR
BIT TO
PROG
GND
5V
214uS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	
	VOP	16.0	17.0	18.0	V	
	VPP					NA
	VPPV					NA
	TPW	300	400	500	µs	
	TR	10		50	µs	
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	1.4	1.5	1.6	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.6	5.1	5.6	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	1.4	1.5	1.6	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.6	5.1	5.6	V	701-1655/TP3

NOTES

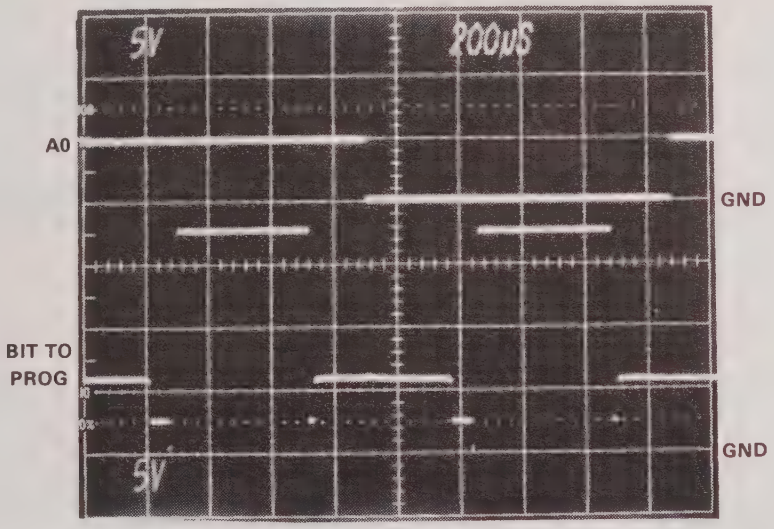
1. *Load RAM with hex FE for Family AD.*
2. *Load RAM with hex 01 for Family AE.*
3. *Load V_{CC} with a 330Ω, ½-watt resistor.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		XH	5/83
		ECN #5023		CTB	3/84

DATA I/O

TITLE: TIMING DIAGRAM FAMILY CODES AD, AE	DRAWN BY:
	CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193
DRAWING NO.: 33-950-0059	
SCALE	SHEET 1 of 2

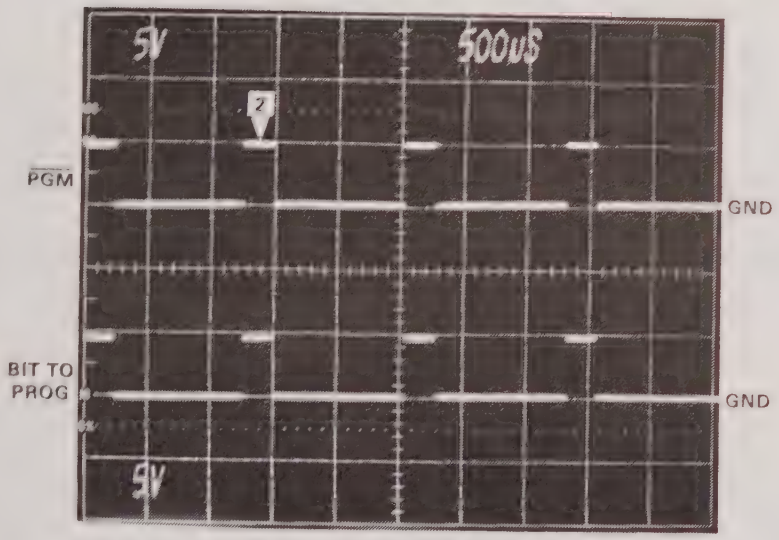


5

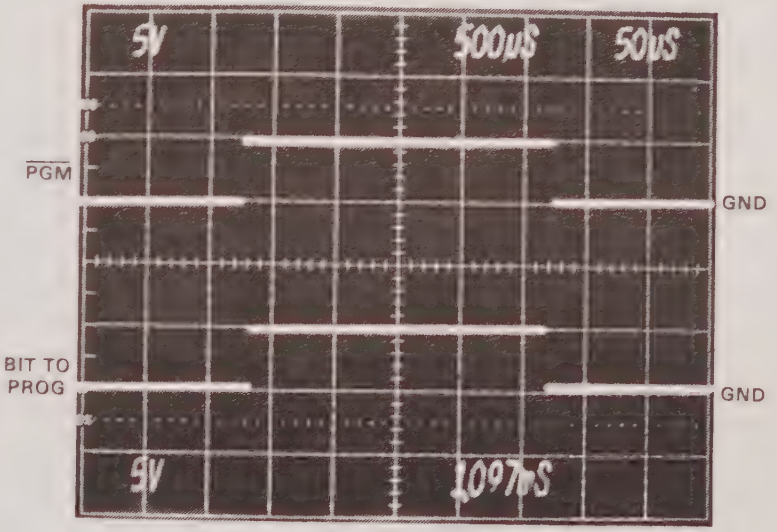
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		XH	5/83
		ECN #5023		CTJ	3/84

DATA I/O

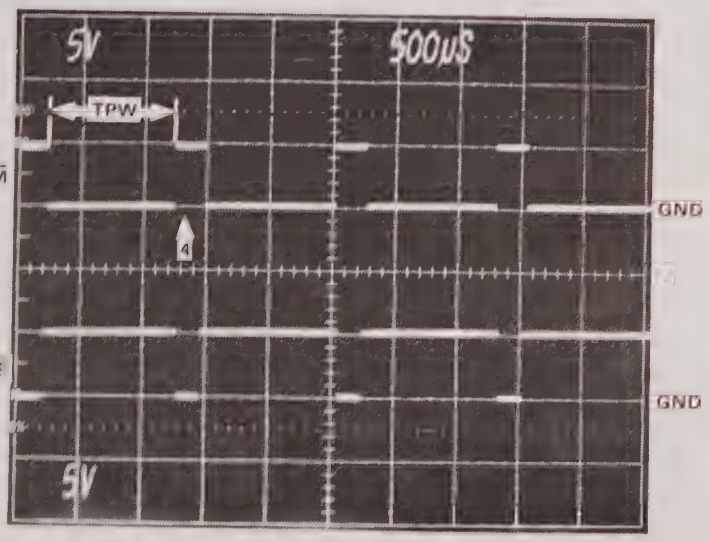
TITLE: TIMING DIAGRAM FAMILY CODES AD, AE		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2


5V
500µS
2
PGM
GND
BIT TO PROG
GND
5V

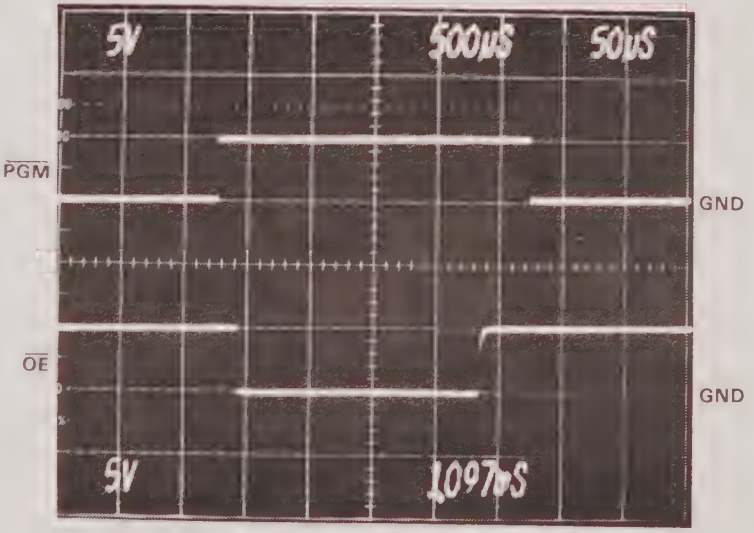
1


5V
500µS
50µS
PGM
GND
BIT TO PROG
GND
5V
1097µS

2


5V
500µS
TPW
PGM
4
GND
OE
GND
5V

3


5V
500µS
50µS
PGM
GND
OE
GND
5V
1097µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.75	6.0	6.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	21.0	21.5	22.0	V	Not shown
	V_{PPV}					N.A.
	t_{pw}	0.95	1.0	1.05	ms	
	t_r					N.A.
	t_f					N.A.
	Reject		25		PULSE	
	Overprogram		1		PULSE	See note 3
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family AF.*
2. *Load RAM with hex 01 for Family BO and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The overprogram pulse is 2 ms long; see photos 6 and 7.*

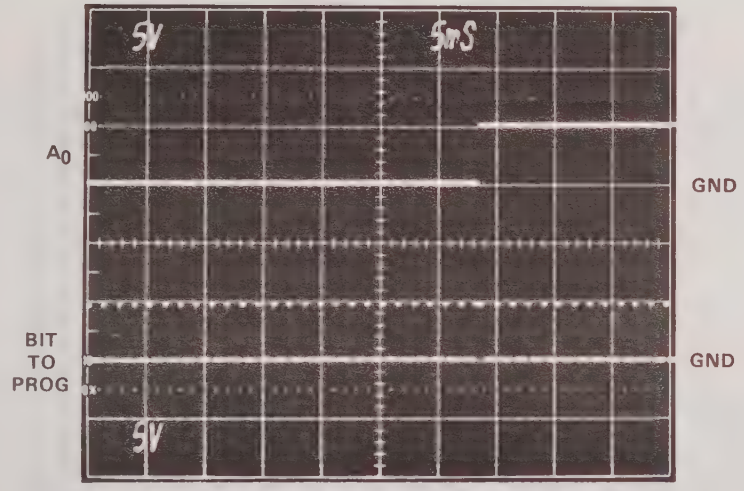
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTB	3/84

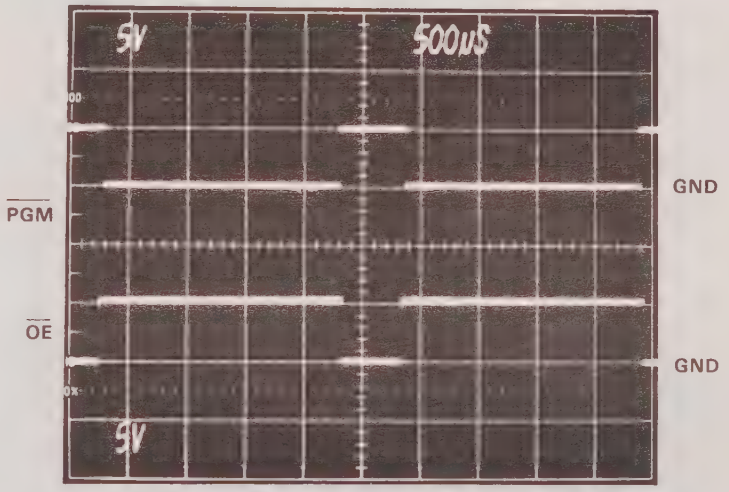
TIMING DIAGRAM

FAMILY CODES AF, BO

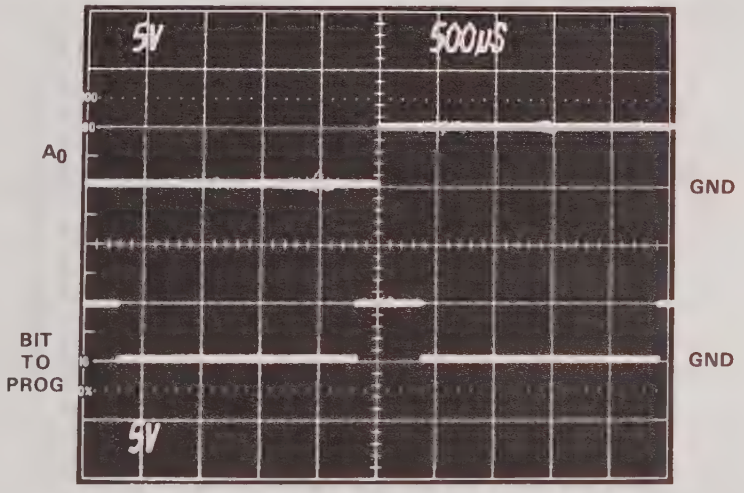
DATA I/O


5V
5mS
A0
GND
BIT
TO
PROG
GND
5V

5


5V
500µS
PGM
GND
OE
GND
5V

6


5V
500µS
A0
GND
BIT
TO
PROG
GND
5V

7

B-215
981-0001

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

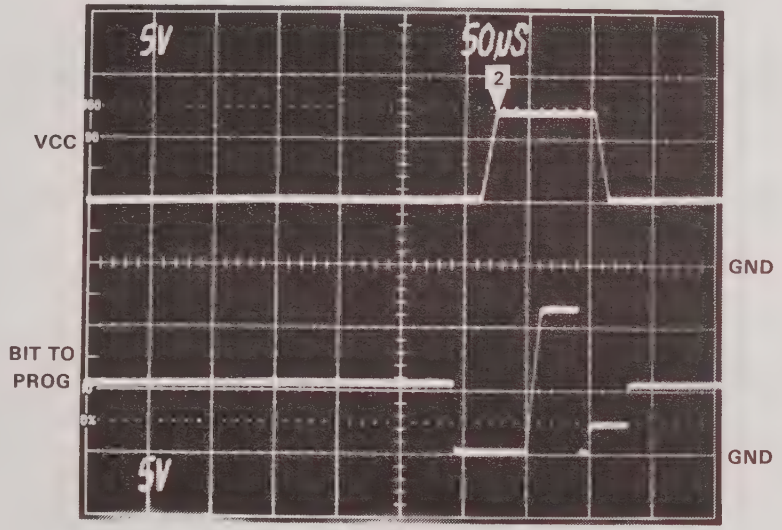
Sheet 2 of 2

TIMING DIAGRAM

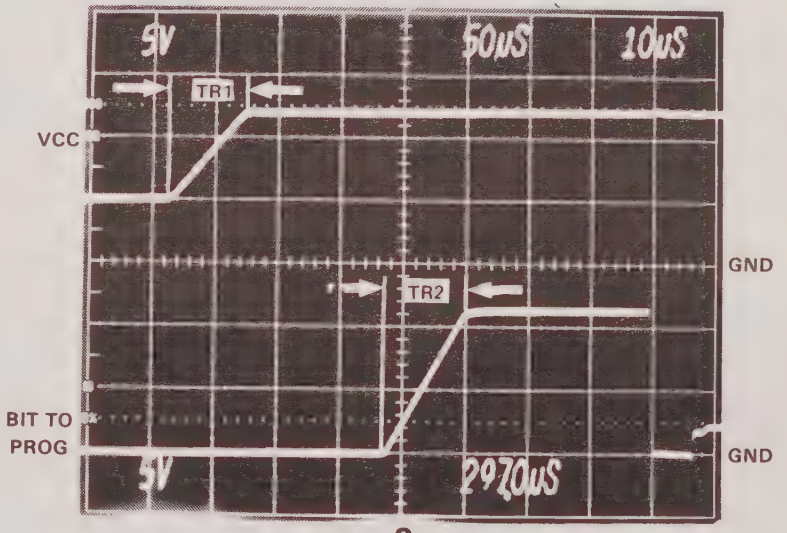
FAMILY CODES AF, BO

DATA I/O

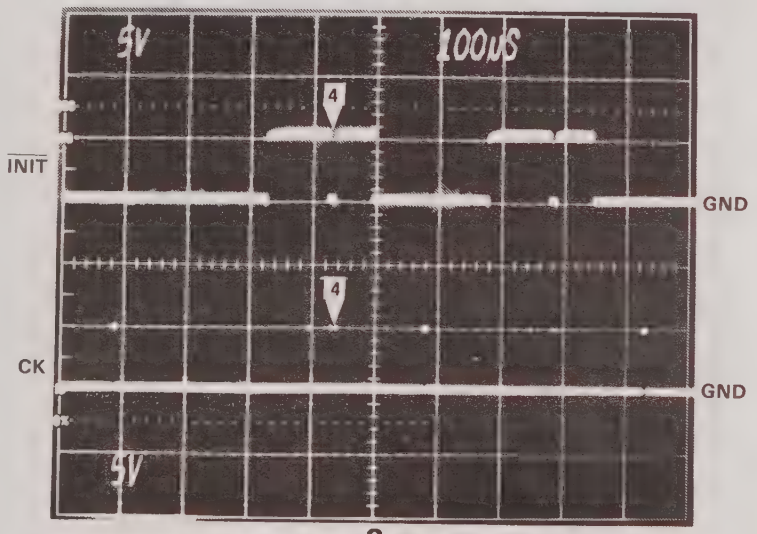
0526 1282


5V
50uS
2
VCC
GND
BIT TO
PROG
GND
5V

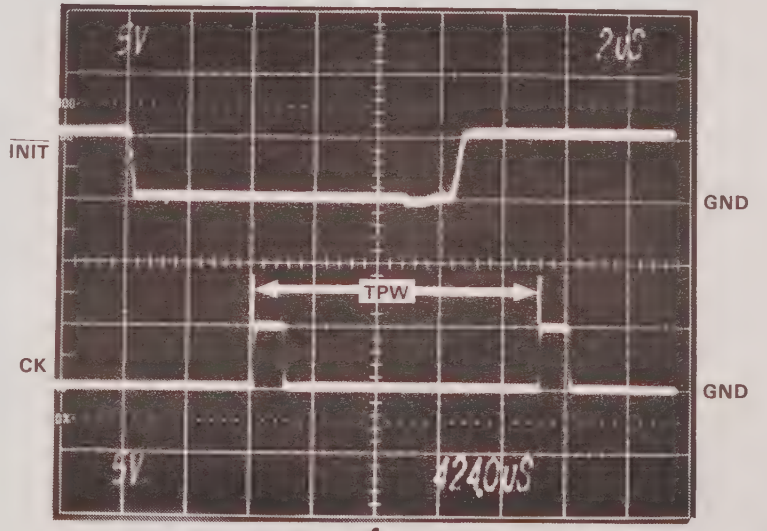
1


5V
50uS
10uS
TR1
VCC
GND
TR2
BIT TO
PROG
GND
5V
2970uS

2


5V
100uS
4
INIT
GND
4
CK
GND
5V

3


5V
2uS
INIT
GND
TPW
CK
GND
5V
4240uS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	11.6	11.8	12.0	V	
	VOP	10.5	11.0	11.5	V	
	VPP					NA
	VPPV					NA
	TPW	9.0	10.0	11.5	μs	
	TR1	1.0		20.0	μs	See note 3
	TR2	1.0		15.0	μs	
	TF					NA
	Reject		10		Pulses	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.1	4.2	4.3	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	7.0	8.0	9.0	V	701-1655/TP4
	Low Load	7.0	8.0	9.0	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	3.4	3.5	3.6	V	701-1655/TP2
	High Load	8.3	9.3	10.3	V	701-1655/TP4
	Low Load	8.3	9.3	10.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family B1.*
2. *Load RAM with hex 01 for Family B2.*
3. *Load V_{CC} with a 330 Ω, ½-watt resistor.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		KH	5/83
		ECN #5023		CTZ	3/84

DATA I/O

TITLE: TIMING DIAGRAM

FAMILY CODES B1, B2

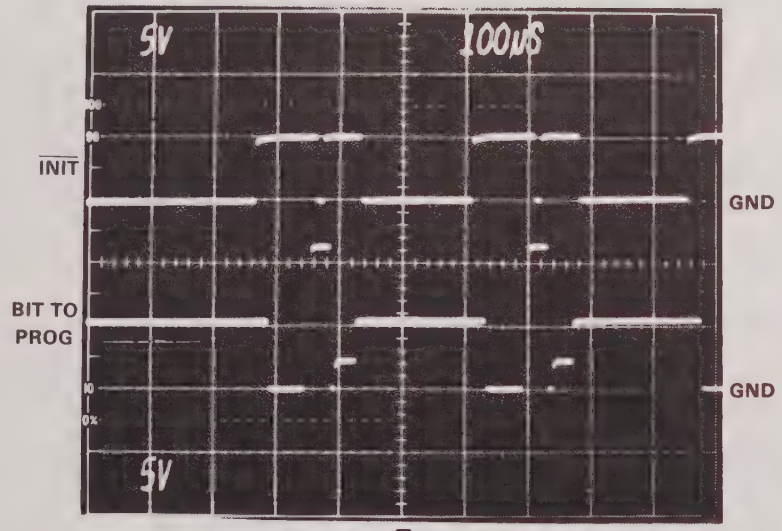
DRAWN BY:

CHECKED BY: KH

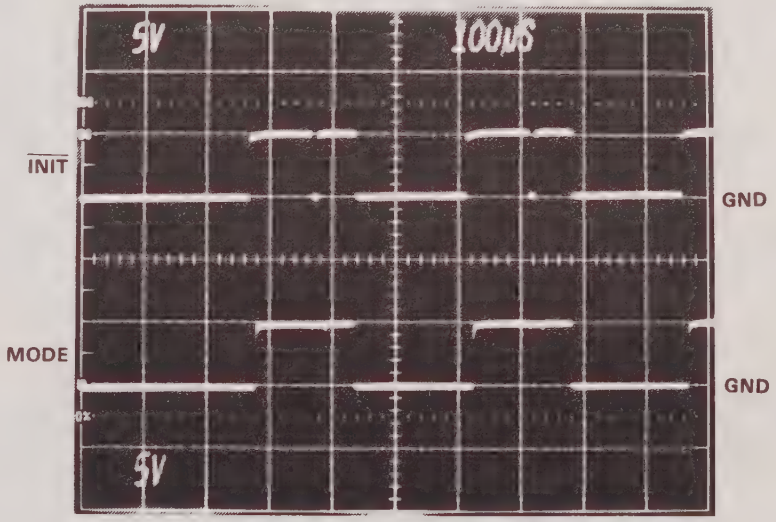
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

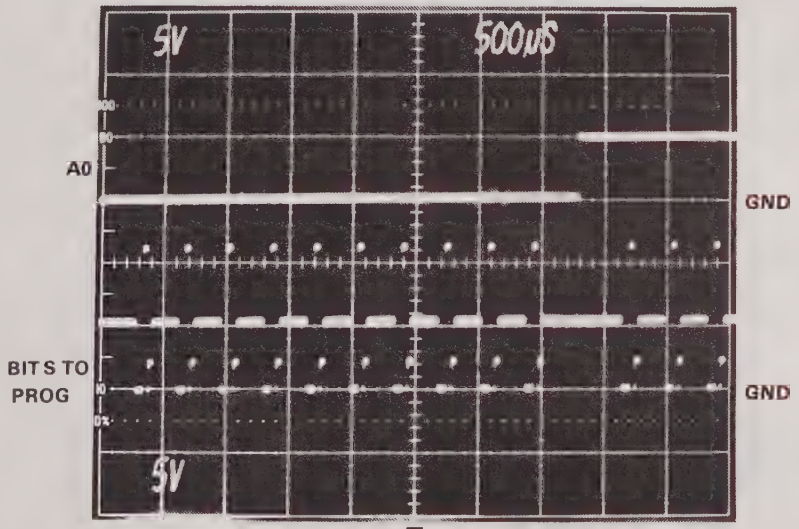
SHEET 1 of 2


5V
100µS
INIT
GND
BIT TO
PROG
GND
5V

5


5V
100µS
INIT
GND
MODE
GND
5V

6


5V
500µS
A0
GND
BIT S TO
PROG
GND
5V

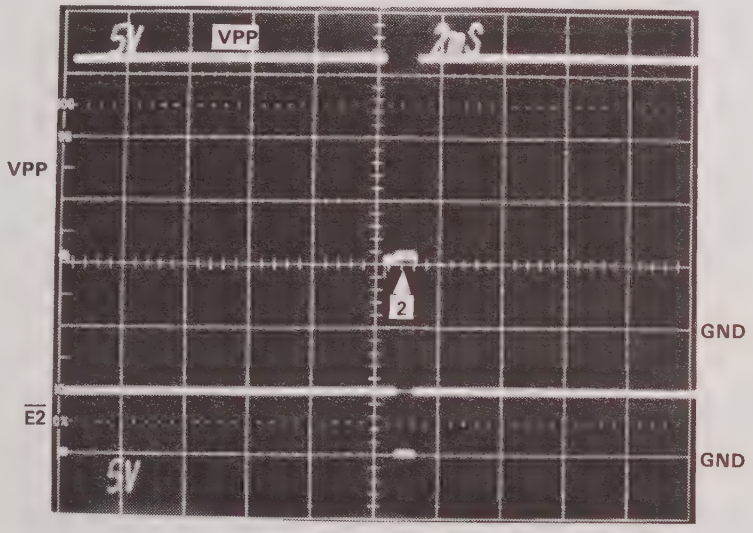
7

B-219
981-0001

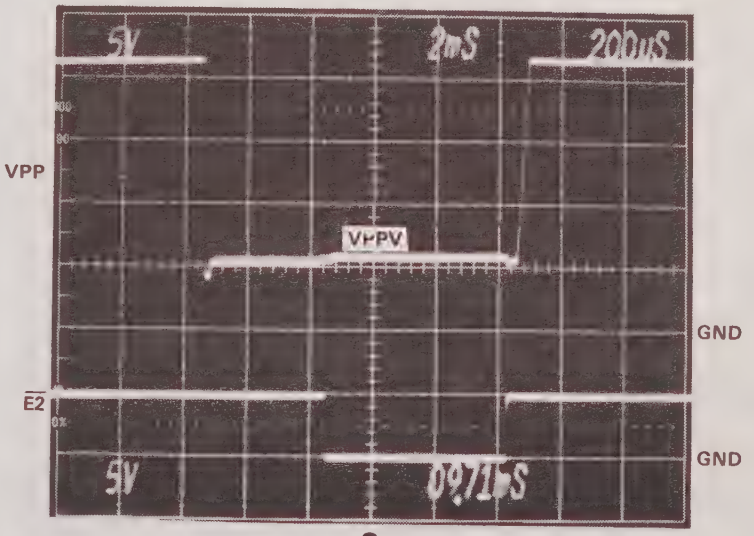
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		XH	5/83
		ECN #5023		CTZ	3/84

DATA I/O

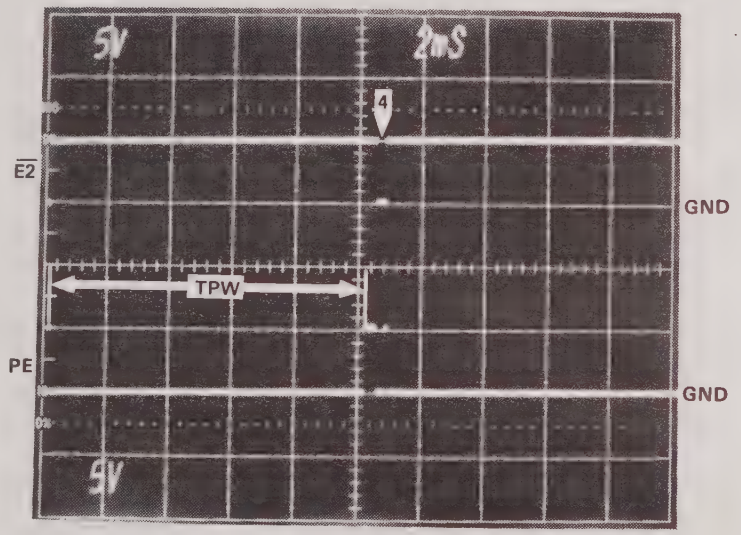
TITLE: TIMING DIAGRAM FAMILY CODES B1, B2		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2


5V
VPP
2mS
VPP
2
GND
E2
GND
5V

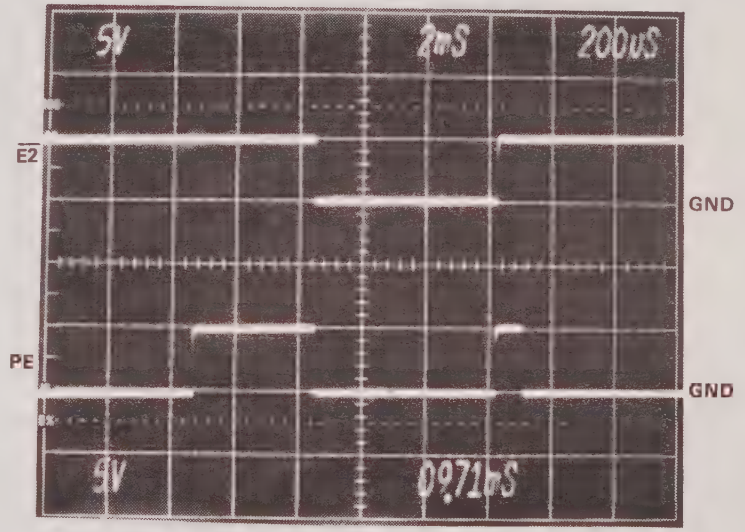
1


5V
2mS
200uS
VPP
VPPV
GND
E2
GND
5V
09.71uS

2


5V
2mS
4
E2
GND
TPW
PE
GND
5V

3


5V
2mS
200uS
E2
GND
PE
GND
5V
09.71uS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not shown
	VOP					NA
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.0	5.25	V	
	VEE	9.0	12.0	15.0	V	
	TPW	9.0		15.0	ms	
	TR					NA
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

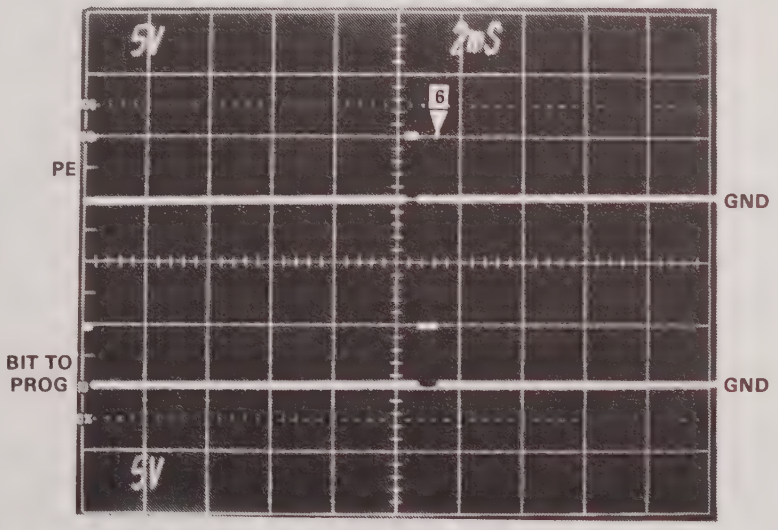
1. *Load RAM with hex FE for Family B3.*
2. *Load RAM with hex 01 for Family B4 and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Chip erase waveforms are photos 8 and 9.*
4. *Byte erase waveforms are photos 10 and 11.*

REVISIONS

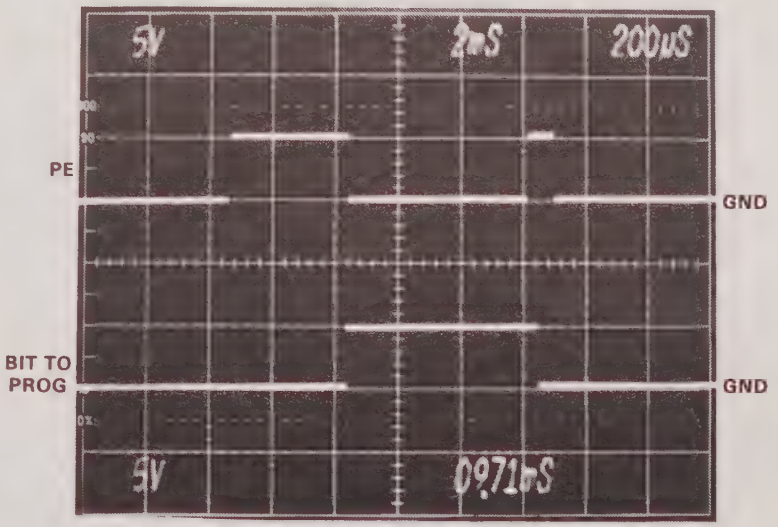
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		JA	5/83
		ECN #5023		CTZ	3/84

DATA I/O

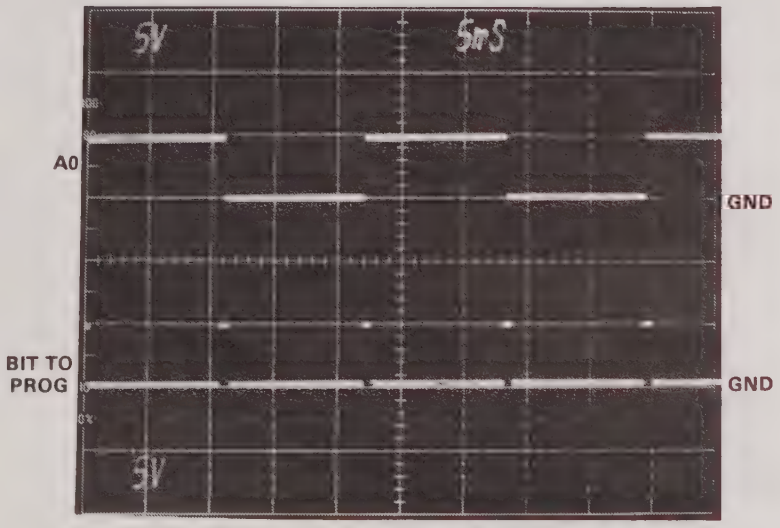
TITLE: TIMING DIAGRAM FAMILY CODES B3, B4		DRAWN BY:
		CHECKED BY: ZH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 3


5V
2mS
6
PE
GND
BIT TO
PROG
GND
5V

5


5V
2mS
200uS
PE
GND
BIT TO
PROG
GND
5V
0971mS

6

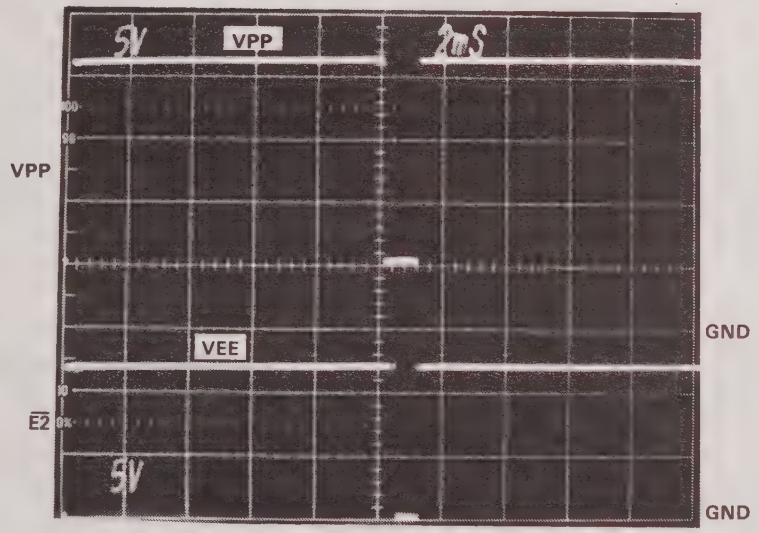

5V
5mS
A0
GND
BIT TO
PROG
GND
5V

7

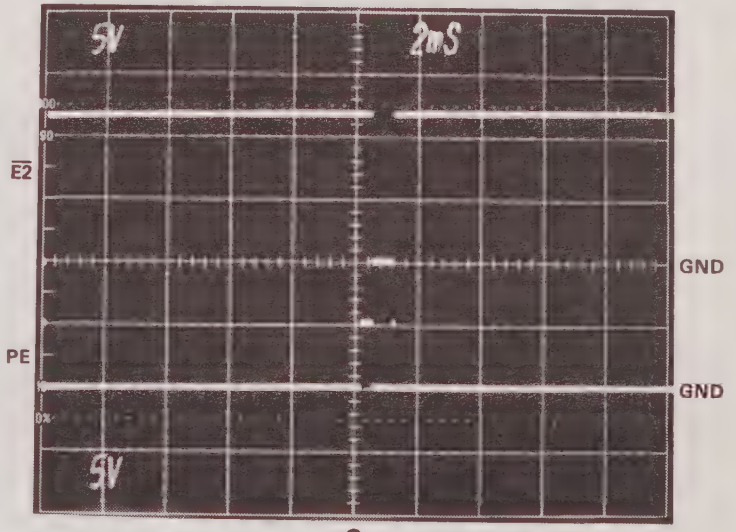
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831			
		ECN #5023	D	CTB	3/84

DATA I/O

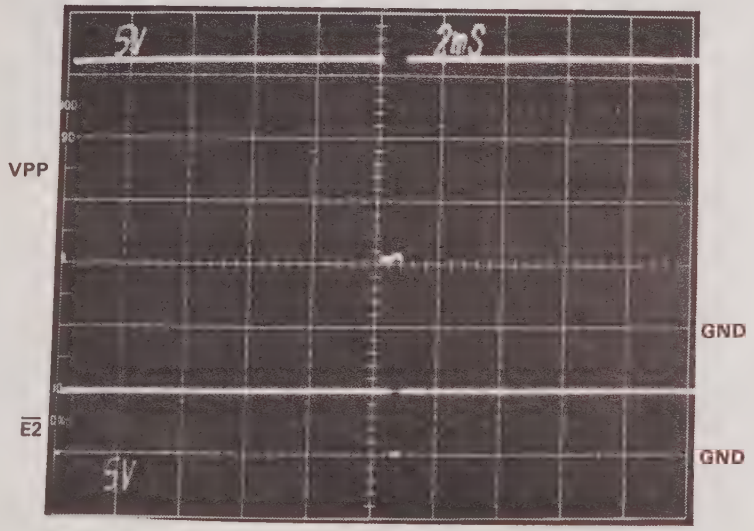
TITLE: TIMING DIAGRAM FAMILY CODES B3, B4		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 3


5V
VPP
2mS
VPP
VEE
GND
E2
5V
GND

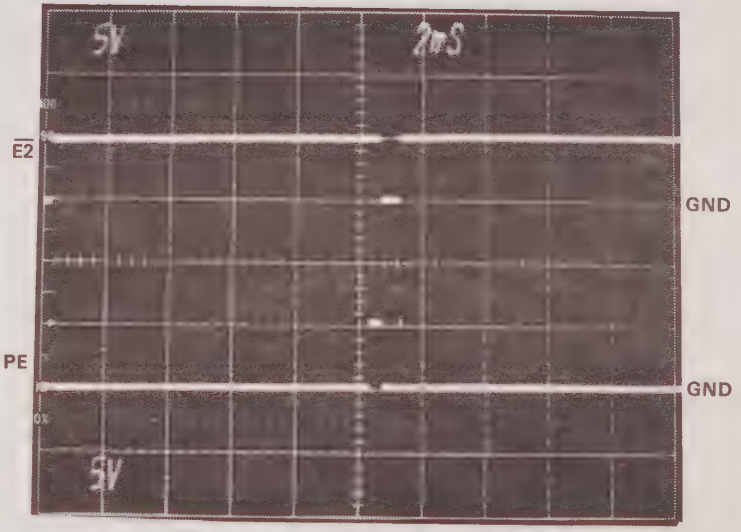
8


5V
2mS
E2
GND
PE
GND
5V

9


5V
2mS
VPP
GND
E2
GND
5V

10

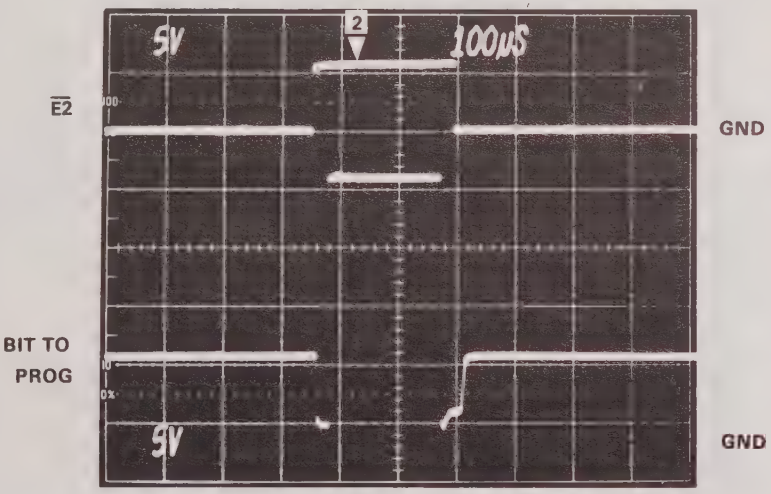

5V
2mS
E2
GND
PE
GND
5V

11

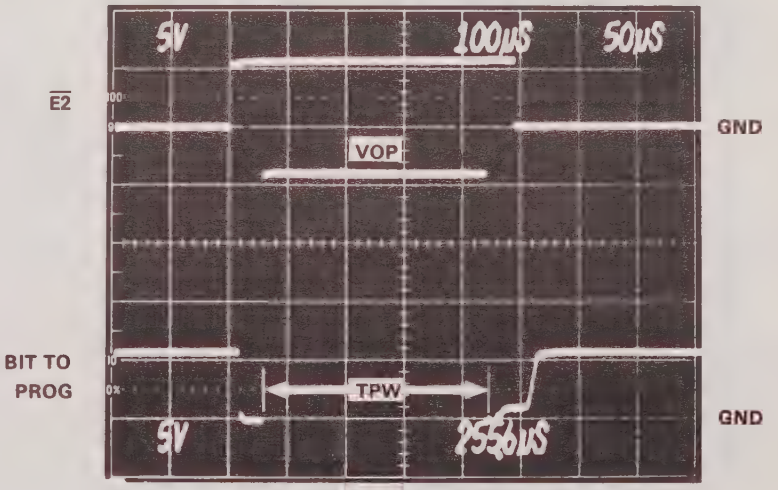
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		XH	5/83
		ECN #5023		CTZ	3/84

DATA I/O

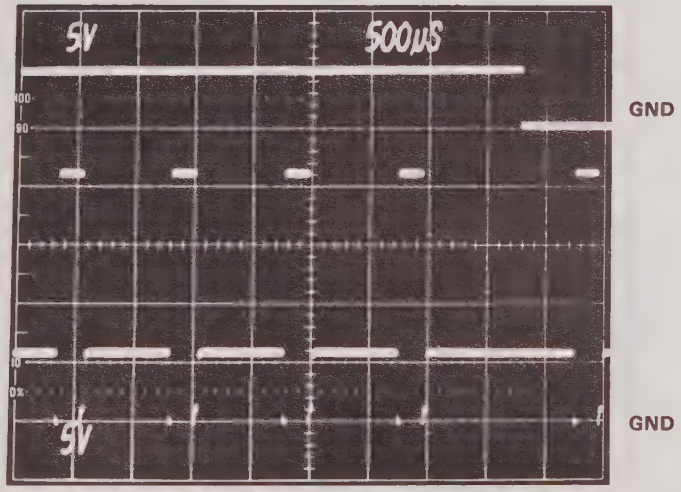
TITLE: TIMING DIAGRAM FAMILY CODES B3, B4		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 3 of 3


5V
2
100µS
E2
GND
BIT TO
PROG
5V
GND

1


5V
100µS
50µS
E2
GND
VOP
BIT TO
PROG
TPW
5V
GND

2


5V
500µS
A0
GND
BIT TO
PROG
5V
GND

3

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not shown
	VOP	20.0	20.5	21.0	V	
	VPP					NA
	VPPV					NA
	TPW	180	190	200	μs	At 10V Level
	TR					NA
	TF					NA
	Reject		4		Pulses	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.3	4.4	4.5	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	24.3	25.3	26.3	V	701-1655/TP4
	Low Load	24.3	25.3	26.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	6.3	6.8	7.3	V	701-1655/TP4
	Low Load	6.3	6.8	7.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family B5.*
2. *Load RAM with hex 01 for Family B6.*

REVISIONS

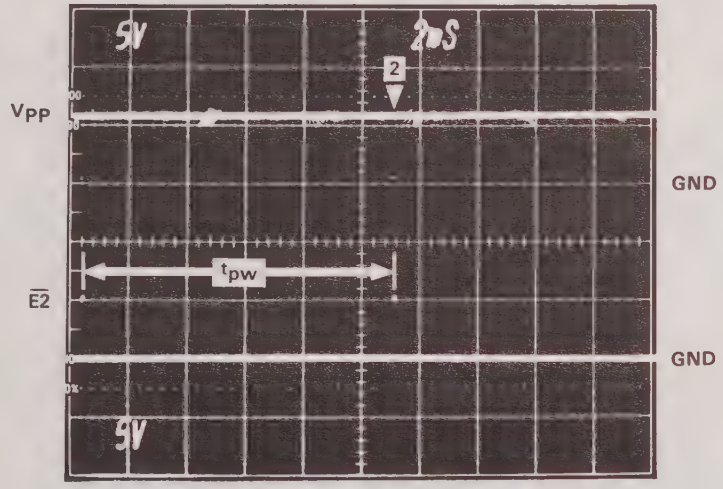
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		KH	[illegible]
		ECN #5023		C73	3/84

DATA I/O

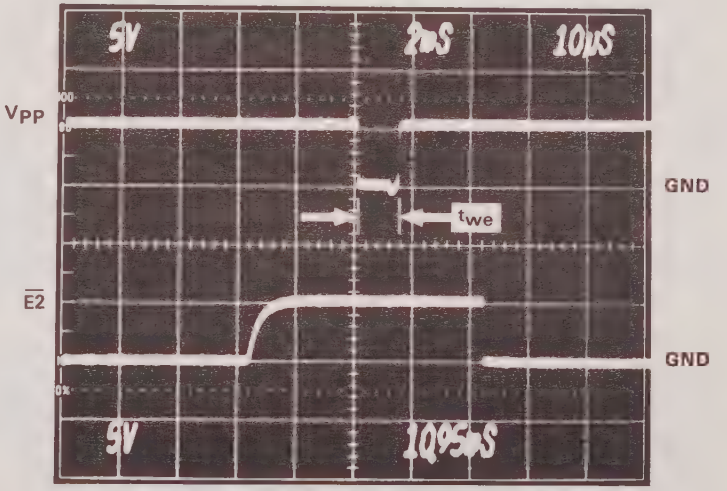
TITLE	DRAWN BY:
TIMING DIAGRAM FAMILY CODES B5, B6	CHECKED BY: KH

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

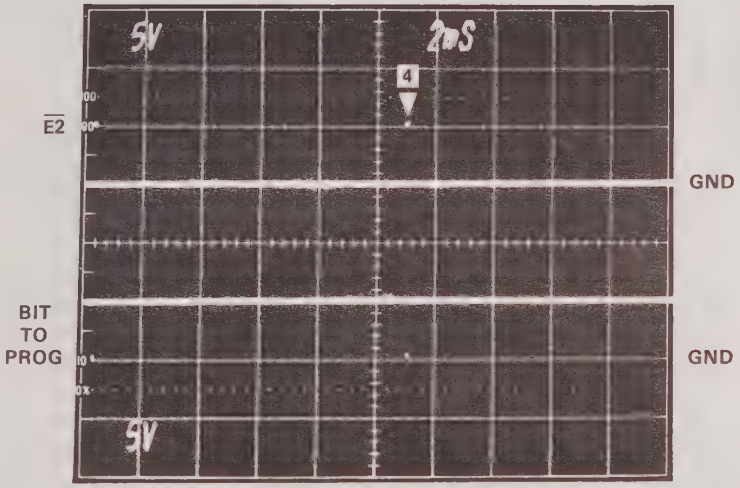
SCALE | SHEET 1 of 1


5V
2mS
2
VPP
GND
E2
tpw
GND
5V

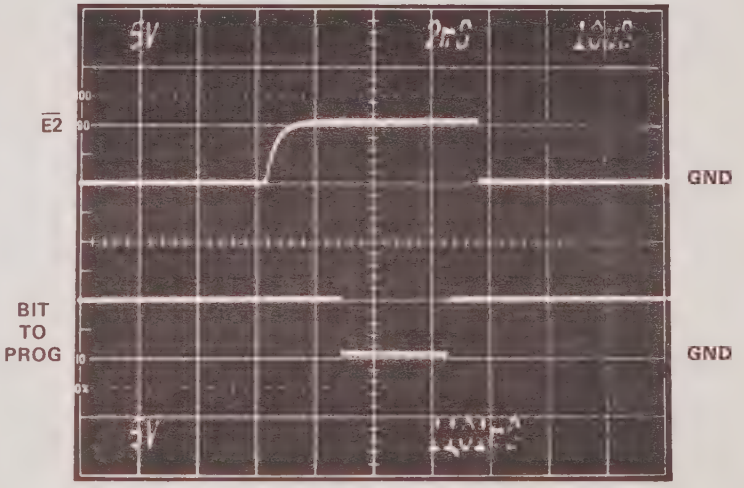
1


5V
2mS
10µS
VPP
GND
twe
E2
GND
5V
1Q95mS

2


5V
2mS
4
E2
GND
BIT
TO
PROG
GND
5V

3


5V
2mS
E2
GND
BIT
TO
PROG
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{EP}	20.5	21.0	21.5	V	
	V_{EE}	11.5	12.0	12.5	V	
	t_{we}	150			ns	
	t_{pw}	9	10		ms	
	t_r					N.A.
	t_{ew}	9.0	10	15	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.3	0.4	0.5	V	701-1655/TP2
	HIGH LOAD	4.7	5.2	5.7	V	701-1655/TP4
	LOW LOAD	4.7	5.2	5.7	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.3	2.4	2.5	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	6.5	7.0	7.5	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family B7.*
2. *Load RAM with hex 01 for Family B8.*
3. *Photo 6 shows erase pulse.*

B-229
981-0001

REVISIONS

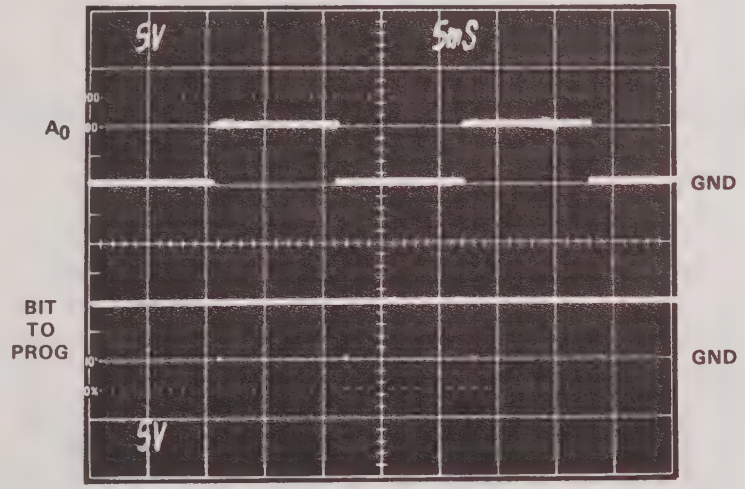
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

Sheet 1 of 2

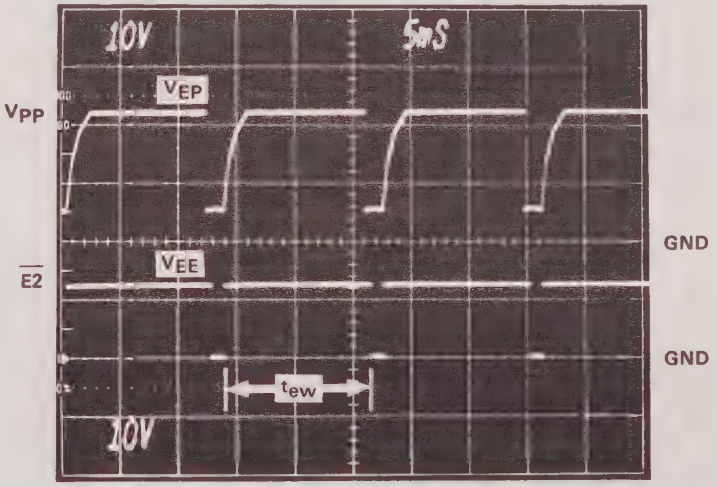
TIMING DIAGRAM

FAMILY CODES B7, B8

DATA I/O


5V
5mS
A_0
GND
BIT
TO
PROG
GND
5V

5


10V
5mS
V_{PP}
V_{EP}
GND
$\overline{E2}$
V_{EE}
GND
t_{ew}
10V

6

B-231
981-0001

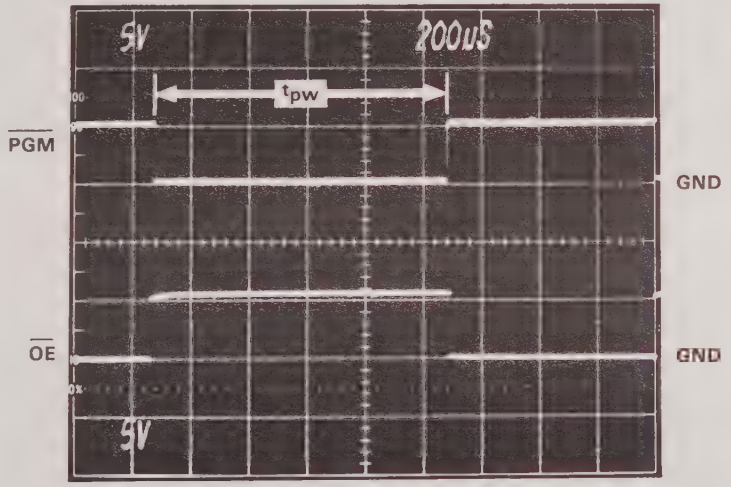
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

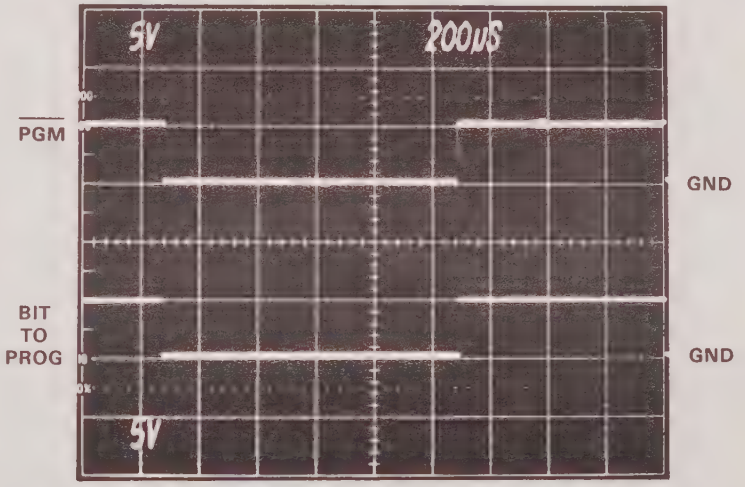
TIMING DIAGRAM

FAMILY CODES B7, B8

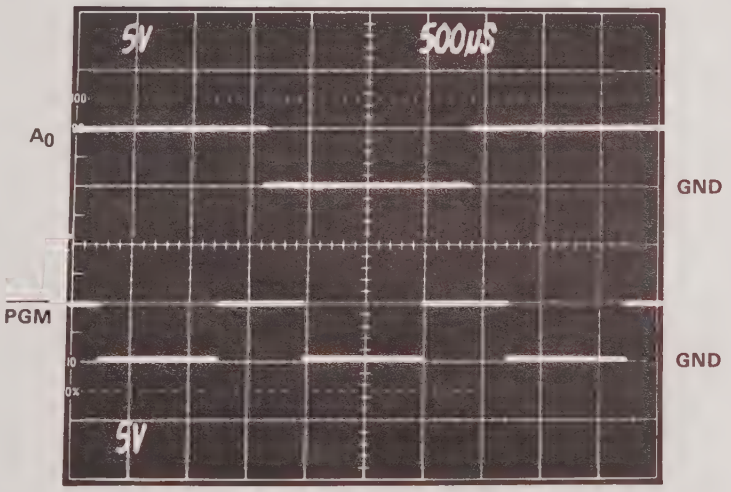
DATA I/O


5V
200µS
tpw
PGM
GND
OE
GND
5V

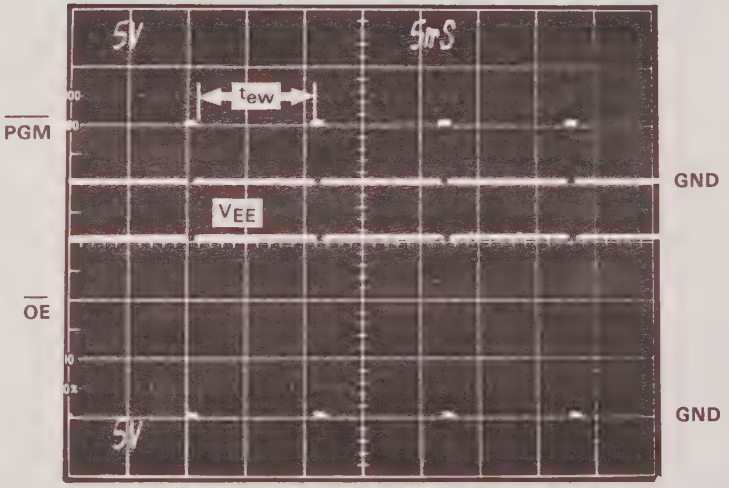
1


5V
200µS
PGM
GND
BIT
TO
PROG
GND
5V

2


5V
500µS
A0
GND
PGM
GND
5V

3


5V
5mS
tew
PGM
GND
VEE
OE
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{EE}	14.0	14.5	15.0	V	
	t_{pw}	0.95	1.0	1.05	ms	
	t_r					N.A.
	t_{ew}	9.5	10.0	10.5	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.5	4.6	4.7	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	5.0	5.5	6.0	V	701-1655/TP4
	LOW LOAD	5.0	5.5	6.0	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.3	5.4	5.5	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	7.3	7.8	8.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family B9.*
2. *Photo 4 is chip erase.*

REVISIONS

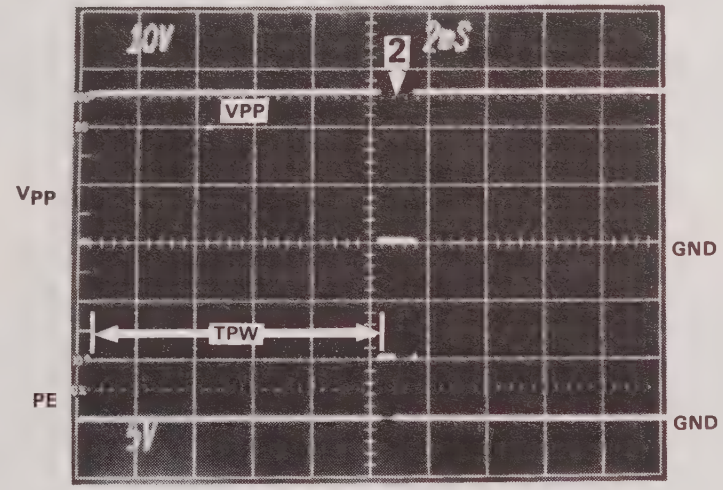
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

Sheet 1 of 1

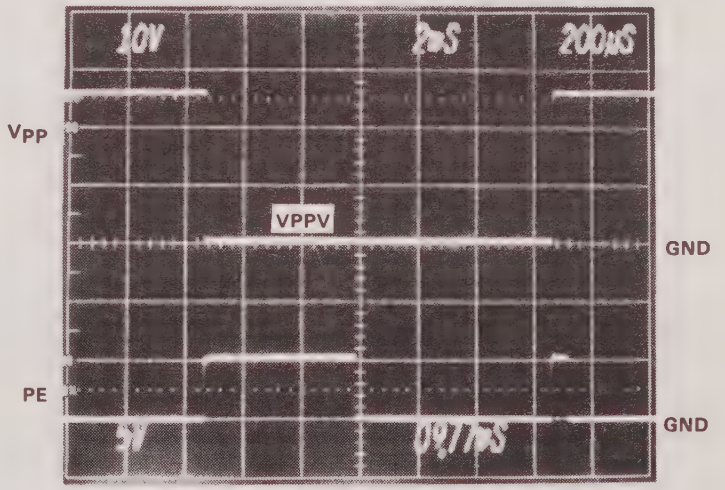
TIMING DIAGRAM

FAMILY CODES B9, BA

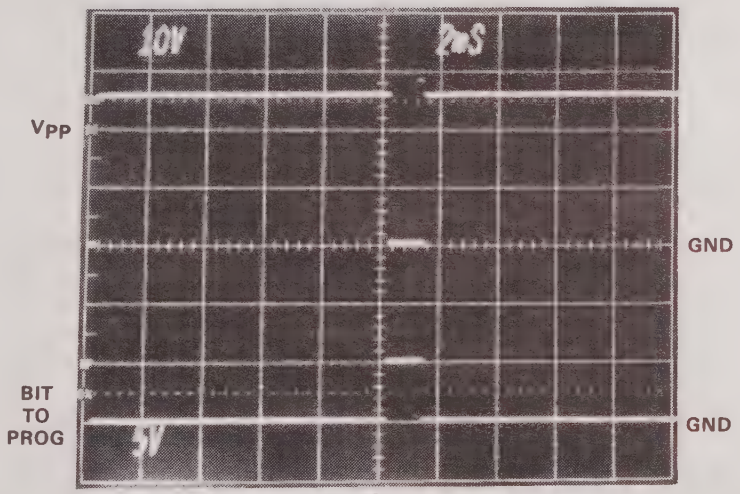
DATA I/O


10V
2
2mS
VPP
VPP
GND
TPW
PE
GND
5V

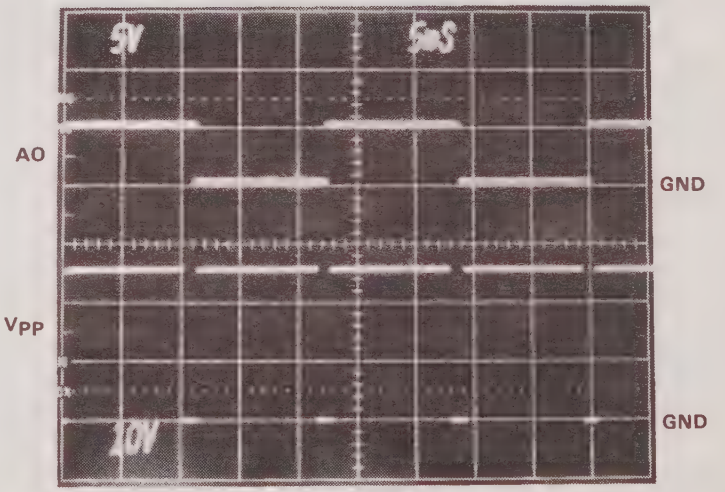
1


10V
2mS
200uS
VPP
VPPV
GND
PE
GND
5V

2


10V
2mS
VPP
GND
BIT
TO
PROG
GND
5V

3


5V
5mS
AO
GND
VPP
GND
10V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	24.5	25.0	25.5	V	
	V_{PPV}	0.0	0.0	0.5	V	
	t_{pw}	9.5	10.0	10.5	ms	
	t_r					N.A.
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family BD.*
2. *Photo 5 is for Pinout 23.*
3. *Photo 6 is for Pinouts 25 and 30.*

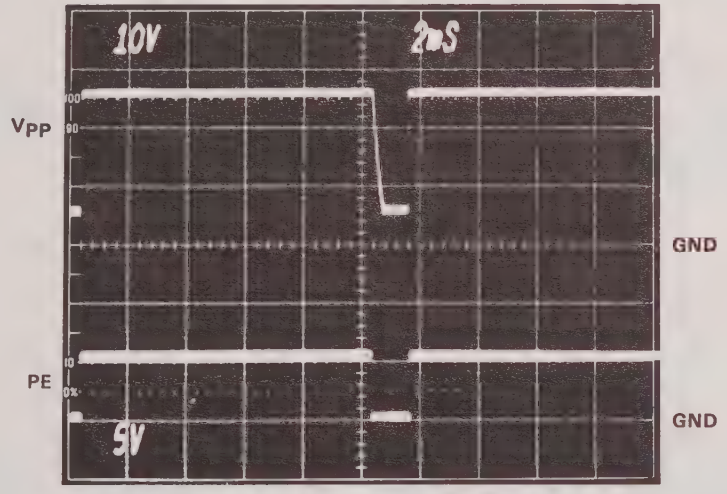
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	3/84

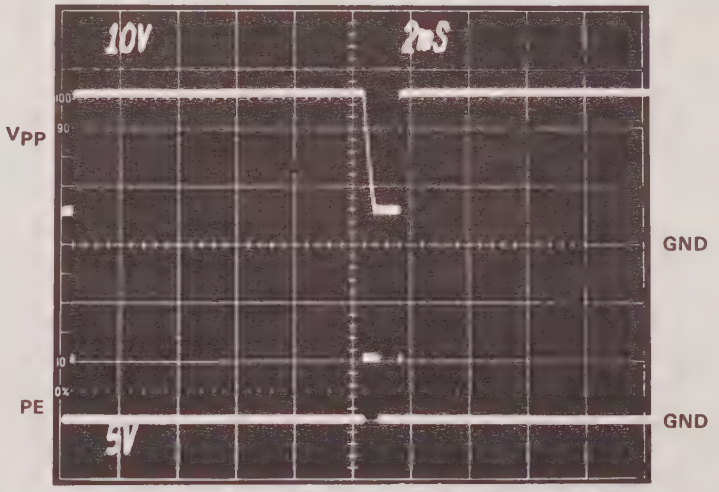
TIMING DIAGRAM

FAMILY CODES BD, BE

DATA I/O


10V
2mS
VPP
100
90
GND
PE
10
0%
GND
5V

5


10V
2mS
VPP
100
90
GND
PE
10
0%
GND
5V

6

B-237
981-0001

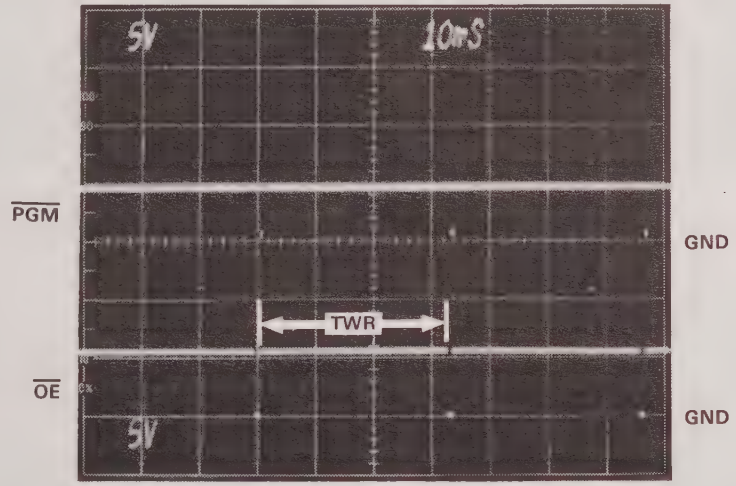
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTB	3/84

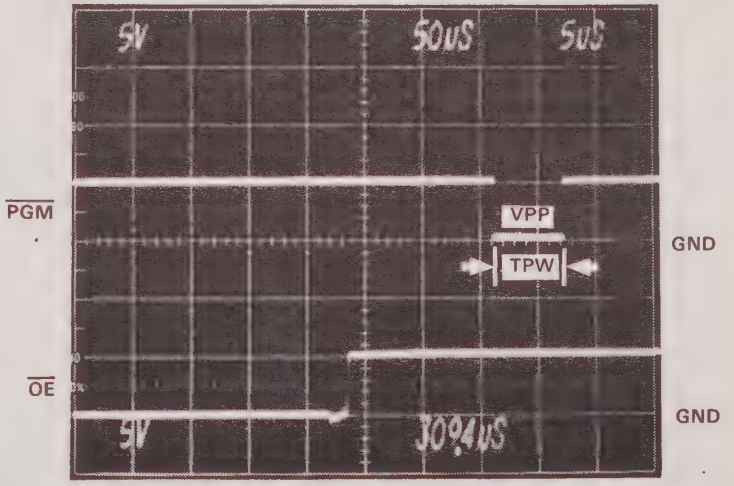
TIMING DIAGRAM

FAMILY CODES BD, BE

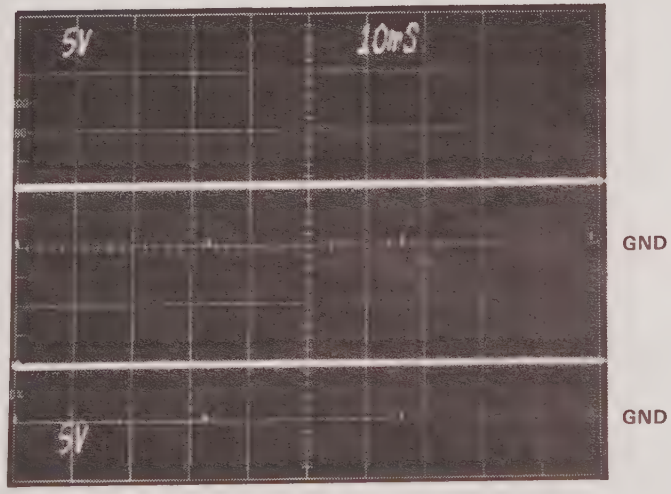
DATA I/O


5V
10mS
PGM
GND
TWR
OE
GND
5V

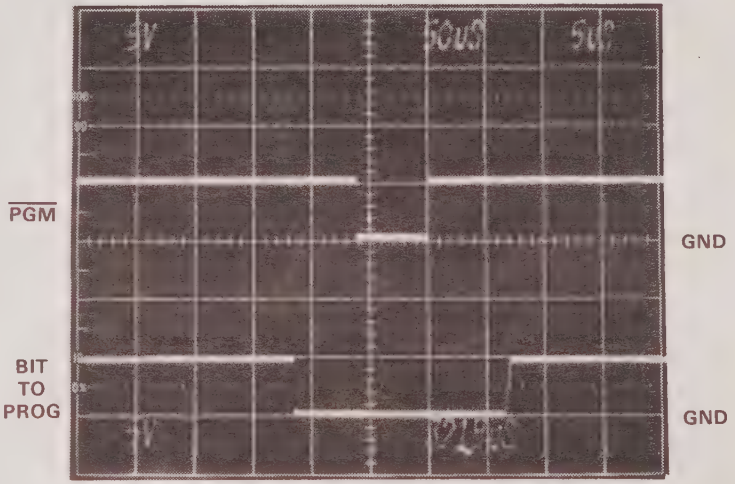
1


5V
50uS
5uS
PGM
VPP
TPW
GND
OE
GND
5V
30.4uS

2


5V
10mS
PGM
GND
BIT
TO
PROG
GND
5V

3


5V
50uS
PGM
GND
BIT
TO
PROG
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	0.0	0.0	0.8	V	
	V_{PPV}					N.A.
	t_{pw}	100			ns	
	t_r					N.A.
	t_{wr}	30			ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family BF.*
2. *Load pin 1 with a 330 Ω, ½-watt resistor to observe TWR in photos 1, 3 and 5.*

REVISIONS

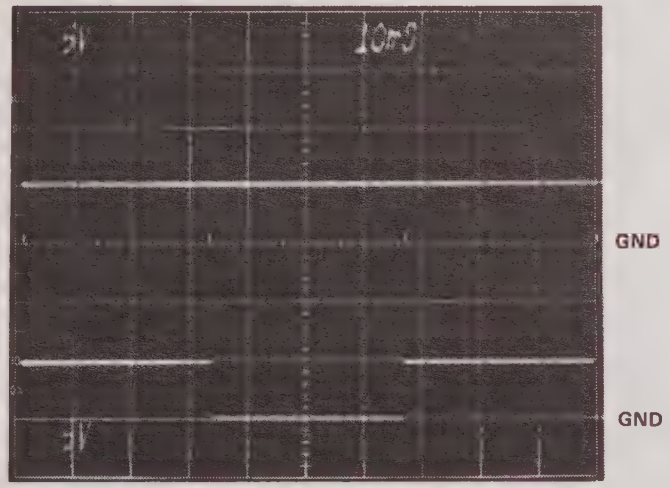
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CJJ	3/84

Sheet 1 of 2

TIMING DIAGRAM

FAMILY CODES BF, CO

DATA I/O



5

B-241
981-0001

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

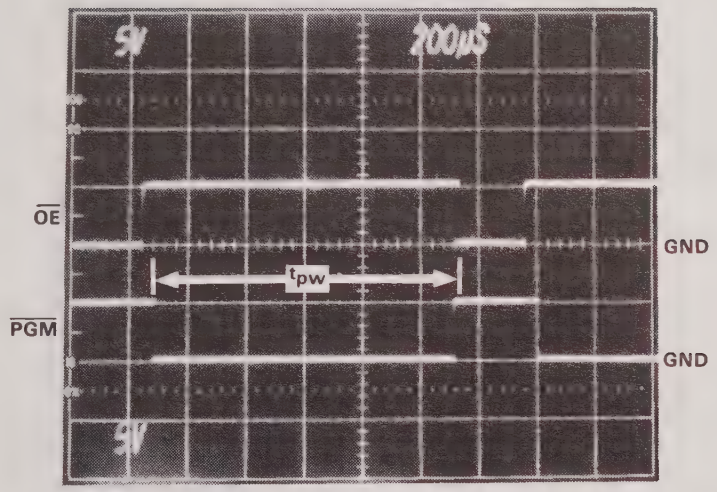
Sheet 2 of 2

TIMING DIAGRAM

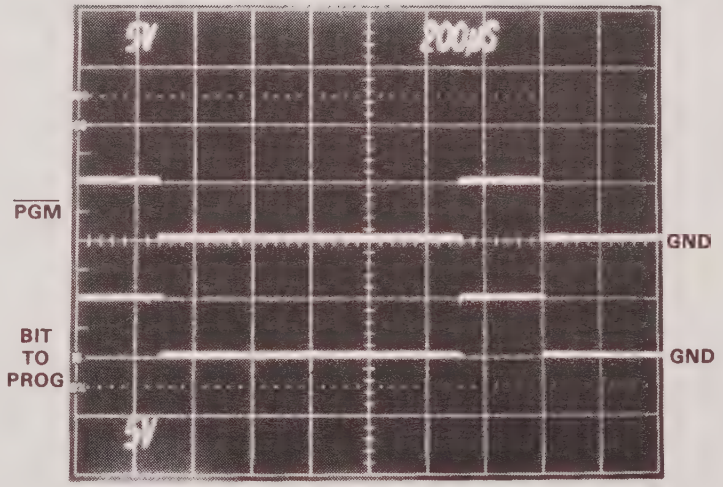
FAMILY CODES BF, CO

DATA I/O

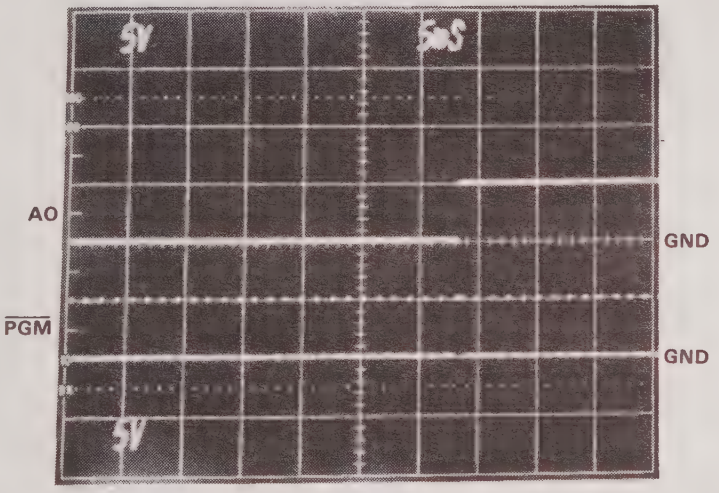
0526/1282


5V
200μS
OE
GND
t_{pw}
PGM
GND
5V

1


5V
200μS
PGM
GND
BIT
TO
PROG
GND
5V

2


5V
5mS
AO
GND
PGM
GND
5V

3

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.75	6.0	6.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	12.5	13.0	13.5	V	Not shown
	V_{PPV}					N.A.
	t_{pw}	0.95	1.0	1.05	ms	
	t_r					N.A.
	t_f					N.A.
	Reject		25		PULSE	
	Overprogram		1		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. Load RAM with hex FE for Family C1.

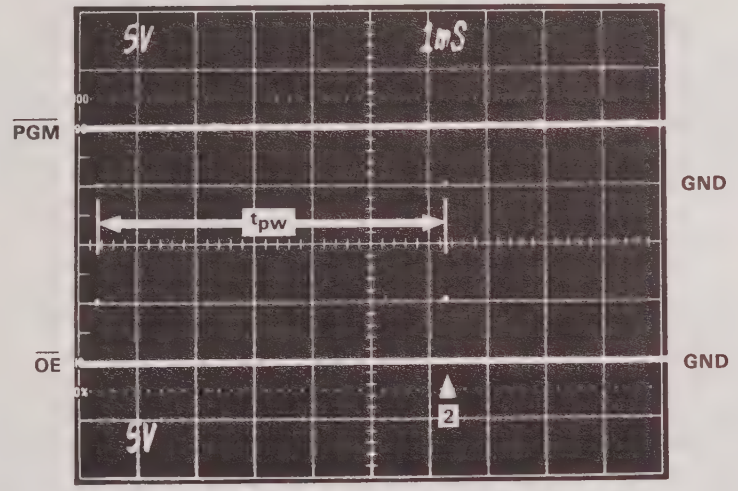
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

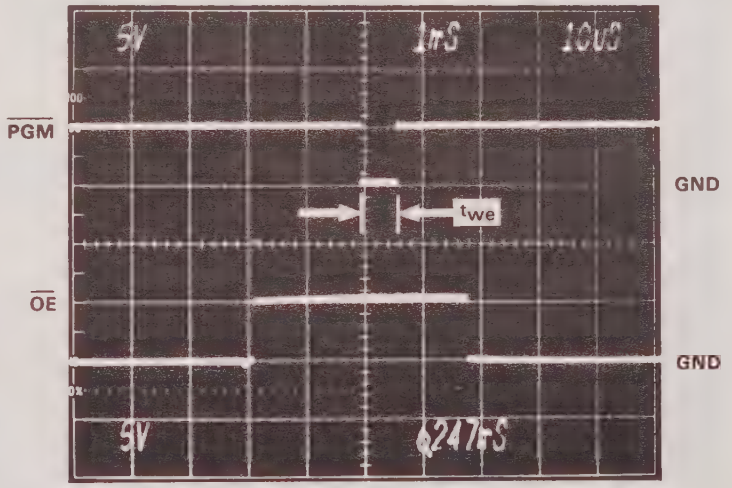
TIMING DIAGRAM

FAMILY CODES C1, C2

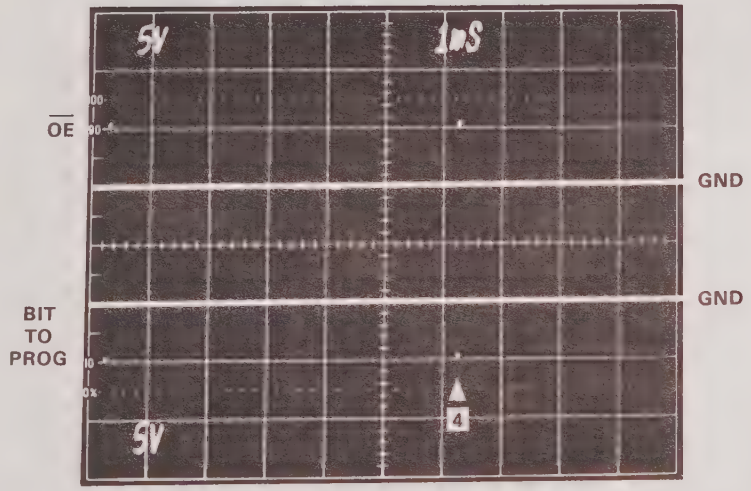
DATA I/O


5V
1mS
PGM
GND
t_{pw}
OE
GND
2
5V

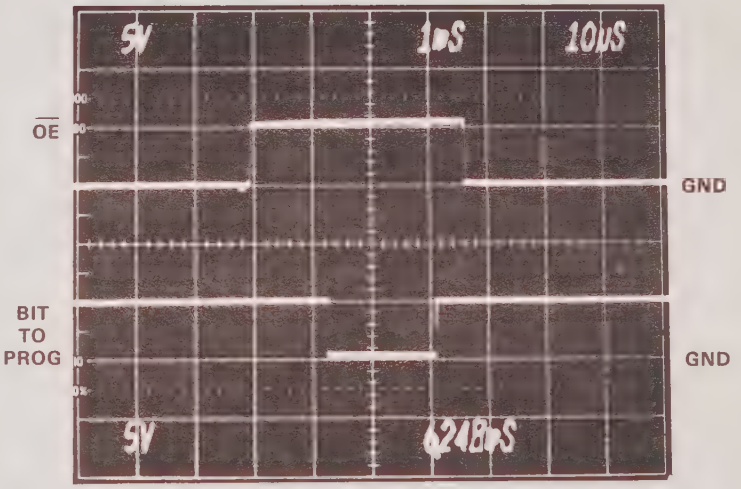
1


5V
1mS
10uS
PGM
GND
t_{we}
OE
GND
5V
6247FS

2


5V
1mS
OE
GND
BIT
TO
PROG
GND
4
5V

3


5V
1mS
10uS
OE
GND
BIT
TO
PROG
GND
5V
6248FS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{EE}	14.5	15.0	15.5	V	
	t_{we}	150			ns	
	t_{pw}	0.1	5.0		ms	
	t_r					N.A.
	t_{ew}	150			ns	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.3	0.4	0.5	V	701-1655/TP2
	HIGH LOAD	4.7	5.2	5.7	V	701-1655/TP4
	LOW LOAD	4.7	5.2	5.7	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.3	2.4	2.5	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	6.5	7.0	7.5	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family C3.*
2. *Load RAM with hex 01 for Family C4.*
3. *Photos 6 and 7 show erase pulse.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTB	3/84

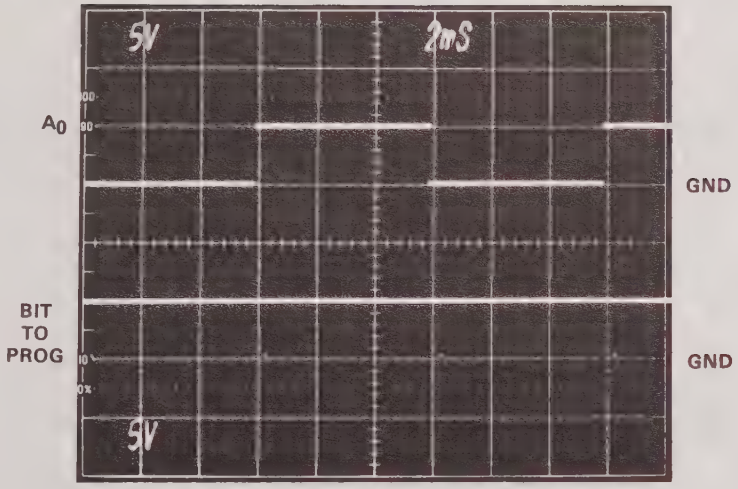
Sheet 1 of 2

TIMING DIAGRAM

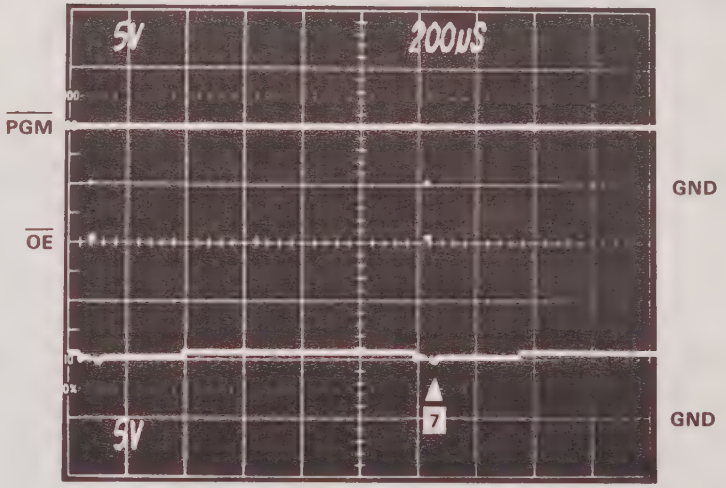
FAMILY CODES C3, C4

DATA I/O

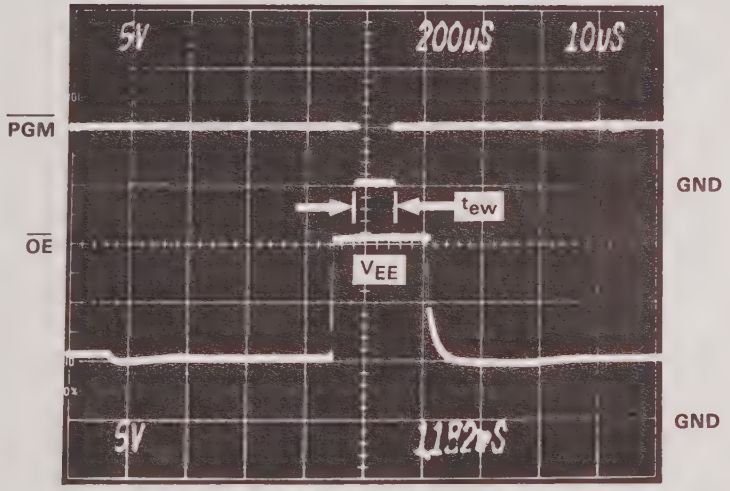
0526/1282


5V
2mS
A_0
GND
BIT
TO
PROG
GND
5V

5


5V
200uS
PGM
GND
OE
7
GND
5V

6


5V
200uS
10uS
PGM
GND
t_{ew}
OE
V_{EE}
GND
5V

7

B-247
981-0001

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	3/84

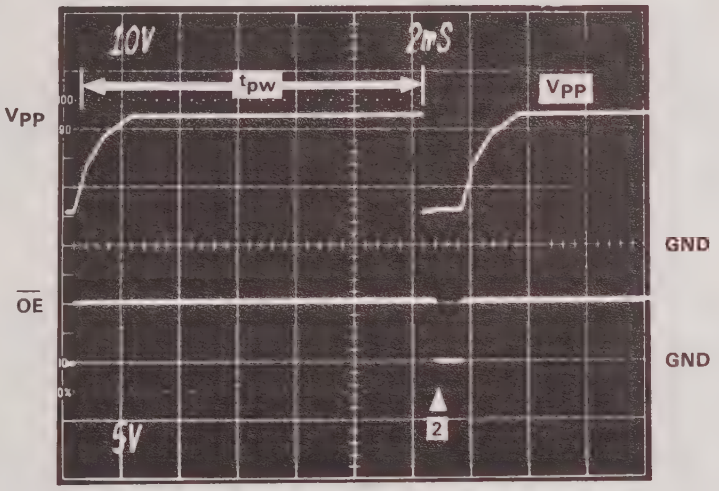
Sheet 2 of 2

TIMING DIAGRAM

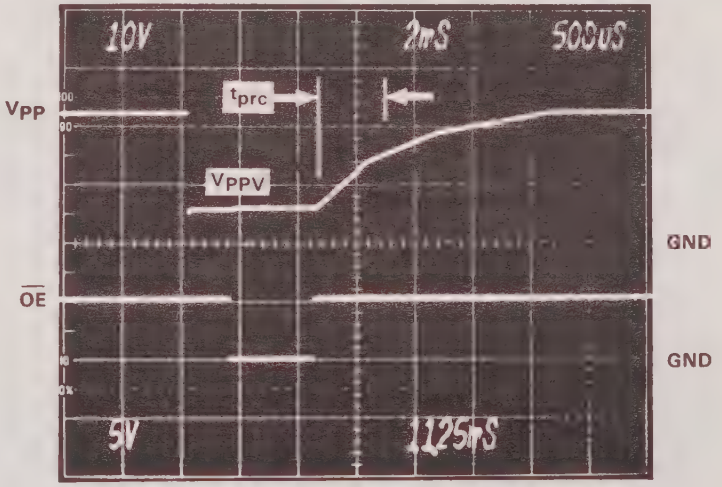
FAMILY CODES C3, C4

DATA I/O

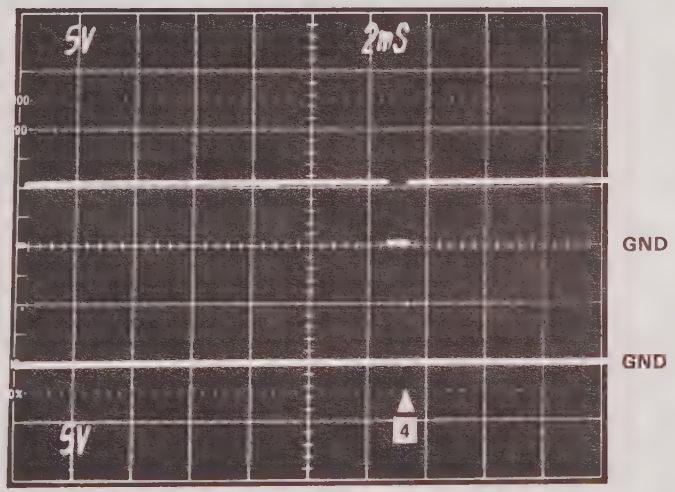
0526/1282


10V
2mS
tpw
VPP
VPP
GND
OE
GND
5V
2

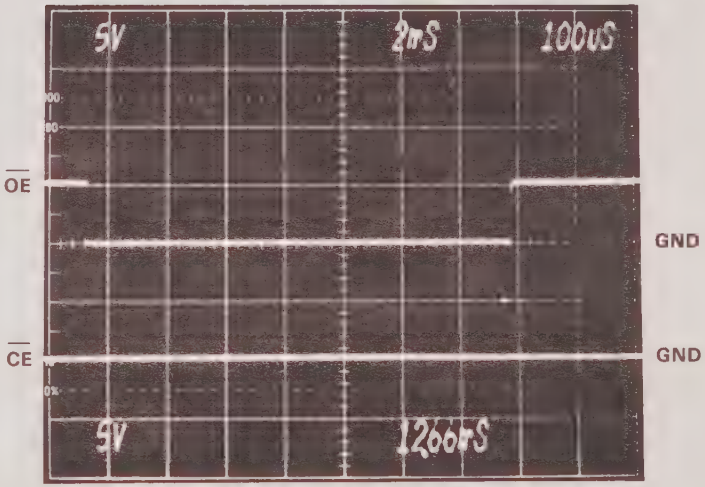
1


10V
2mS
500uS
VPP
tprc
VPPV
GND
OE
GND
5V
1125mS

2


5V
2mS
OE
GND
CE
GND
5V
4

3


5V
2mS
100uS
OE
GND
CE
GND
5V
1260mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	20.0	21.0	22.0	V	
	V_{PPV}	4.0	5.0	6.0	V	
	t_{prc}	450	600	750	μs	See note 3
	t_{pw}	9.0		15.0	ms	
	t_r					N.A.
	t_f			100	μs	
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family C7.*
2. *Load RAM with hex 01 for Family C8.*
3. *TPRC is measured from 6V to 15.5V.*

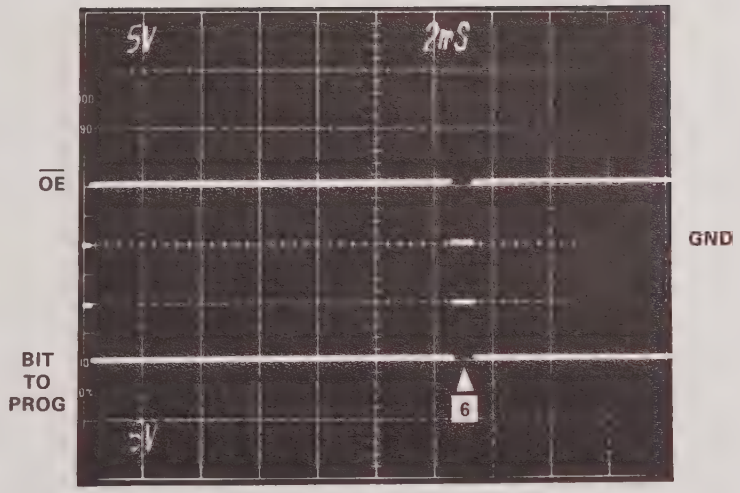
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	C73	3/84

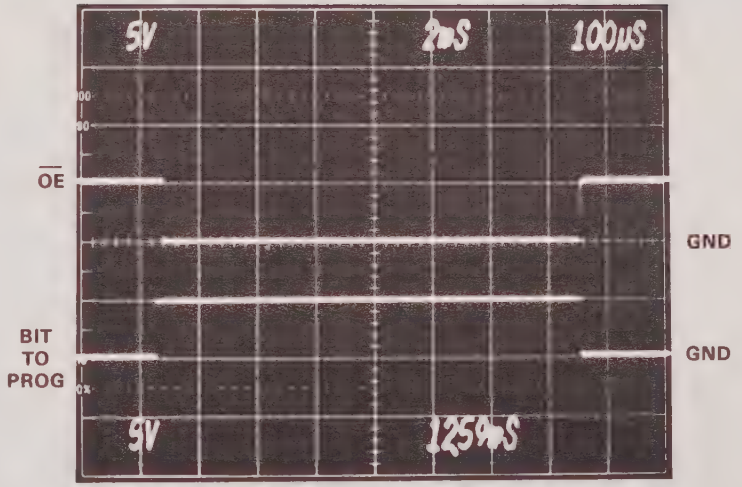
TIMING DIAGRAM

FAMILY CODES C7, C8

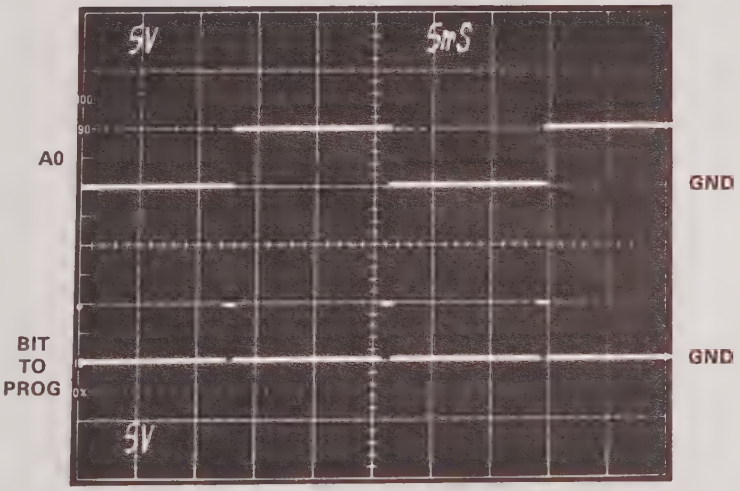
DATA I/O


5V
2mS
OE
GND
BIT
TO
PROG
6
5V

5


5V
2mS
100µS
OE
GND
BIT
TO
PROG
GND
9V
1259µS

6


5V
5mS
A0
GND
BIT
TO
PROG
GND
9V

7

B-251
981-0001

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

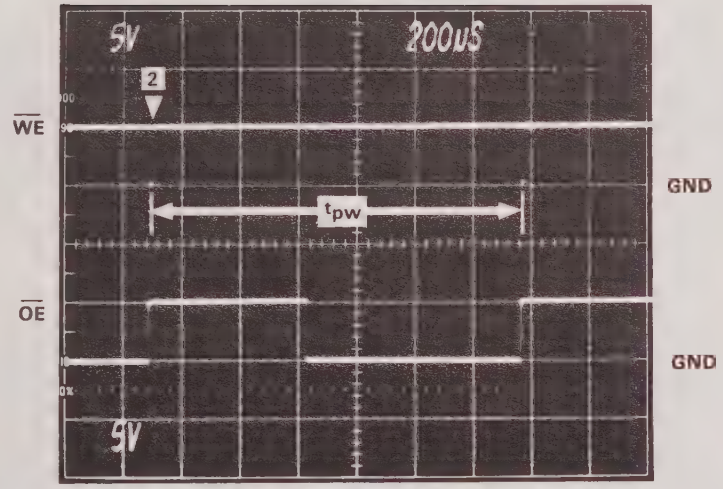
Sheet 2 of 2

TIMING DIAGRAM

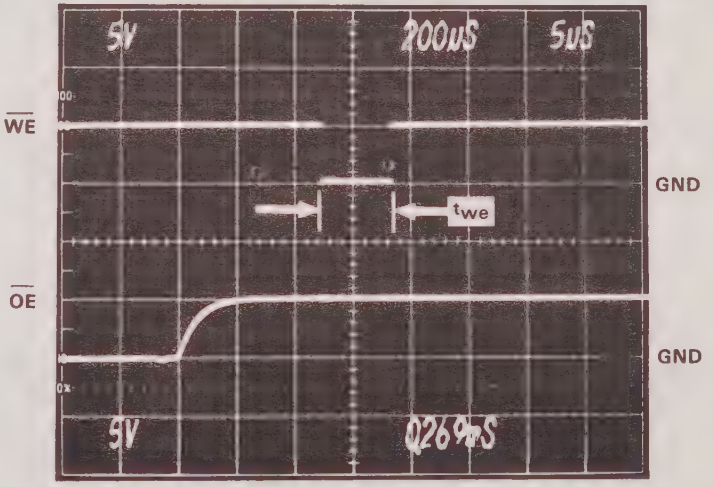
FAMILY CODES C7, C8

DATA I/O

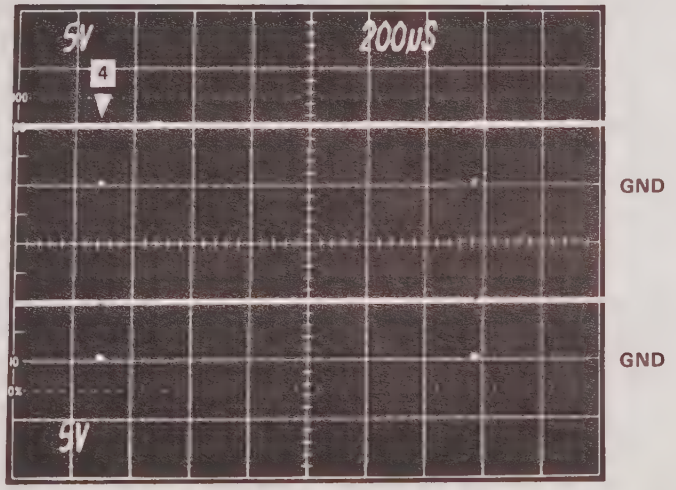
0526/1282


5V
200uS
2
WE
GND
t_{pw}
OE
GND
5V

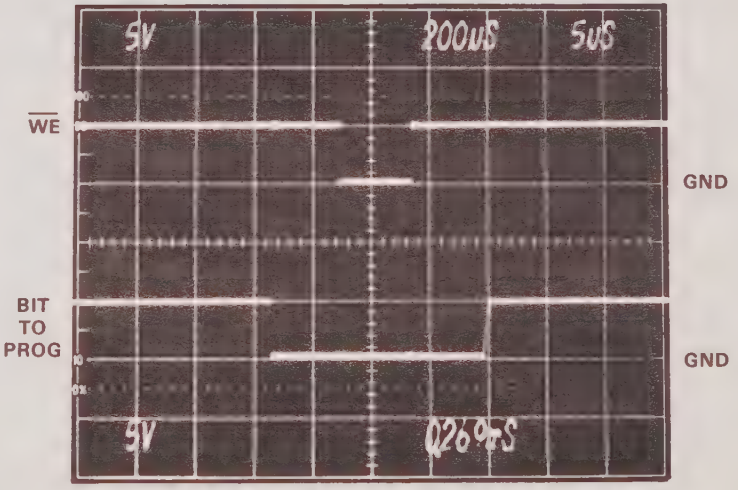
1


5V
200uS
5uS
WE
GND
t_{we}
OE
GND
5V
026.9uS

2


5V
200uS
4
WE
GND
BIT
TO
PROG
GND
5V

3


5V
200uS
5uS
WE
GND
BIT
TO
PROG
GND
5V
026.9uS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{EE}	11.5	12.0	12.5	V	
	t_{we}	70			ns	
	t_{pw}	1.0		25	ms	See note 3
	t_r					N.A.
	t_{ew}	10		12	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family C9.*
2. *Load RAM with hex 01 for Family CA.*
3. *Photo 1 shows min. TPW; photo 6 shows max. TPW (load pin 1 of socket with 100Ω, ¼W resistor to observe waveform photo 6).*
4. *Photo 7 is erase waveform.*

B-253
981-0001

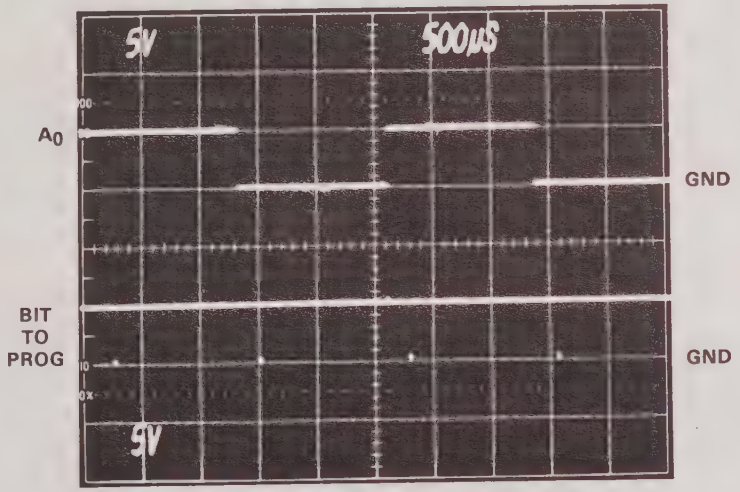
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	3/84

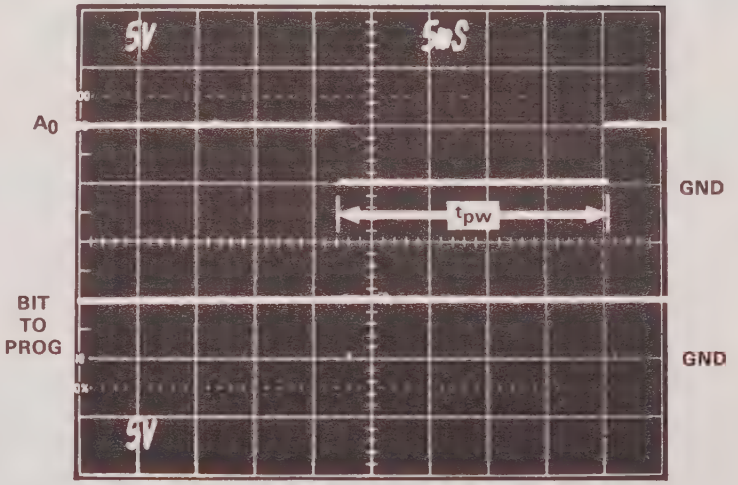
TIMING DIAGRAM

FAMILY CODES C9, CA

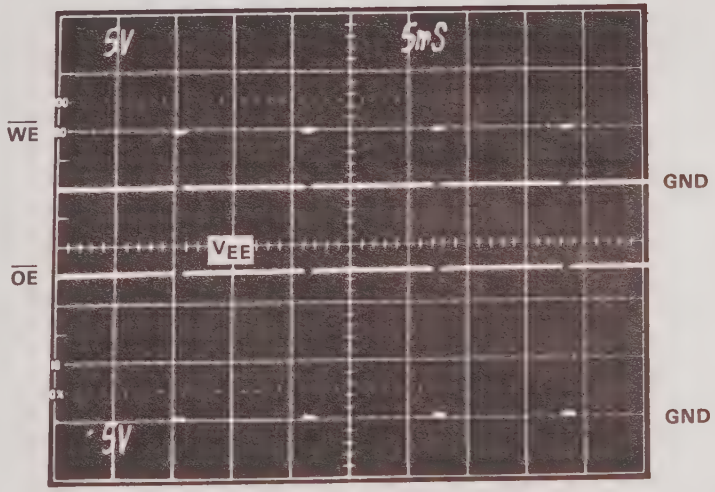
DATA I/O


5V
500µS
A0
GND
BIT
TO
PROG
GND
5V

5


5V
5mS
A0
GND
tpw
BIT
TO
PROG
GND
5V

6


5V
5mS
WE
GND
VEE
OE
GND
5V

7

B-255
981-0001

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	3/84

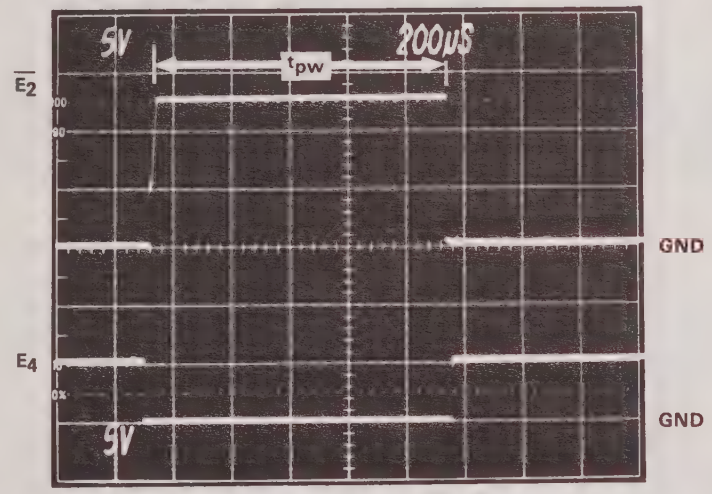
Sheet 2 of 2

TIMING DIAGRAM

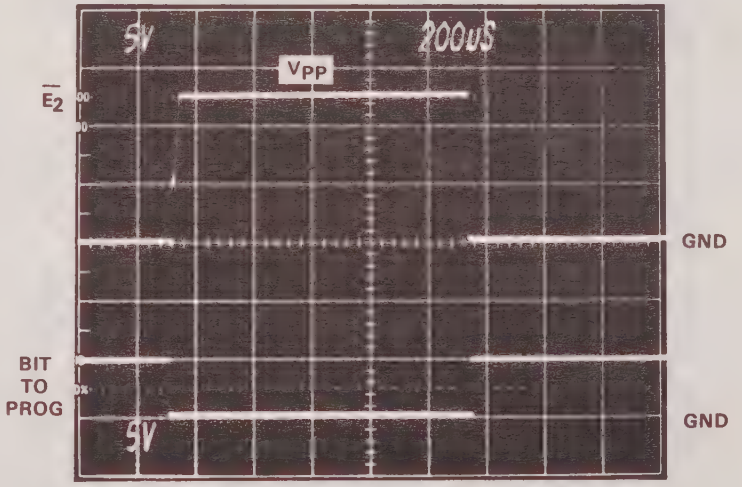
FAMILY CODES C9, CA

DATA I/O

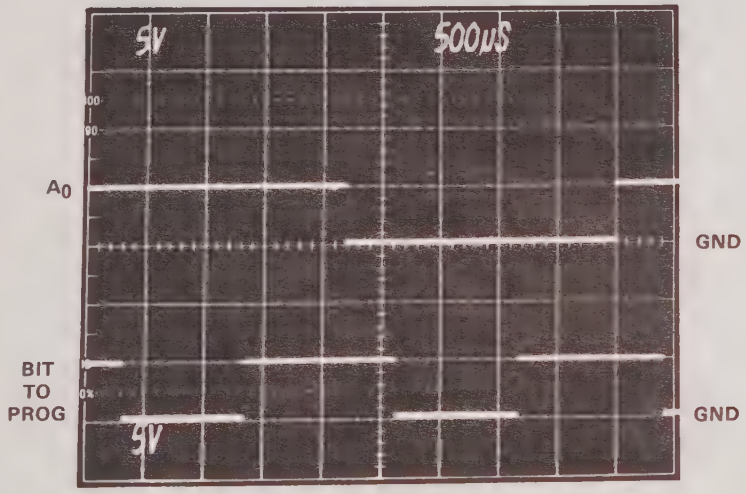
0526/1282


5V
200µS
t_{pw}
$\overline{E_2}$
GND
E_4
GND
5V

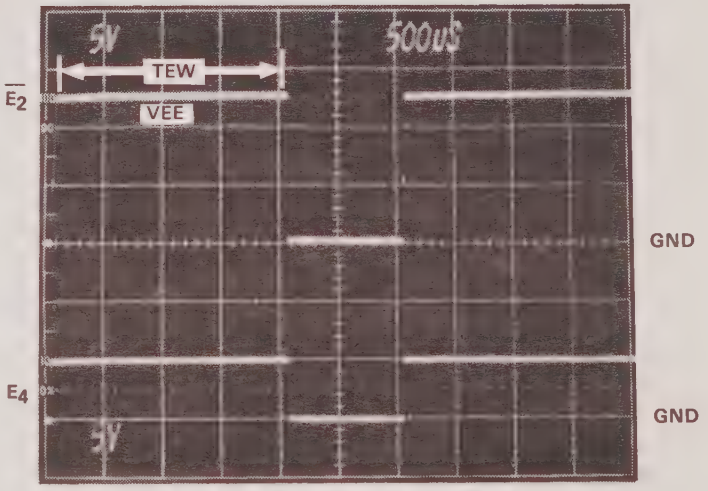
1


5V
200µS
V_{PP}
$\overline{E_2}$
GND
BIT
TO
PROG
GND
5V

2


5V
500µS
A_0
GND
BIT
TO
PROG
GND
5V

3


5V
500µS
TEW
$\overline{E_2}$
VEE
GND
E_4
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	11.5	12.0	12.5	V	
	V_{PPV}					N.A.
	V_{EE}	11.5	12.0	12.5	V	
	t_{pw}	1.0			ms	
	t_r					N.A.
	t_{ew}	2.0			ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.4	4.5	4.6	V	
	V_{REF}	0.7	0.8	0.9	V	701-1655/TP2
	HIGH LOAD	5.1	5.6	6.1	V	701-1655/TP4
	LOW LOAD	5.1	5.6	6.1	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.4	5.5	5.6	V	
	V_{REF}	1.9	2.0	2.1	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	6.1	6.6	7.1	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family CD.*
2. *Load RAM with hex 01 for Family CE.*
3. *Photo 4 shows erase pulse.*

REVISIONS

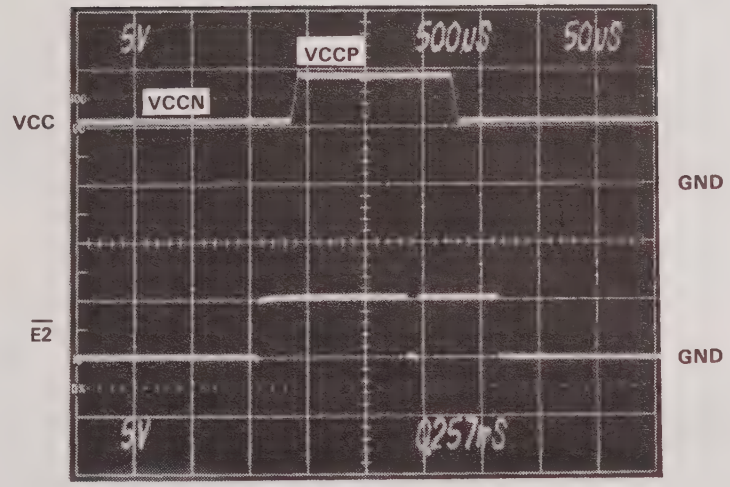
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

Sheet 1 of 1

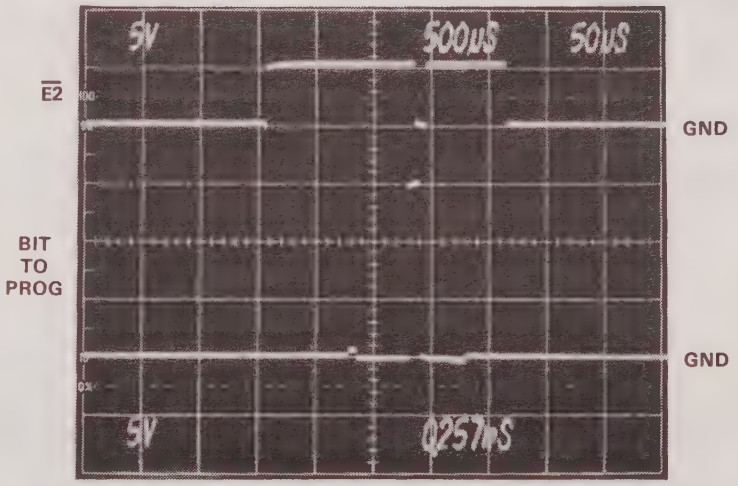
TIMING DIAGRAM

FAMILY CODES CD, CE

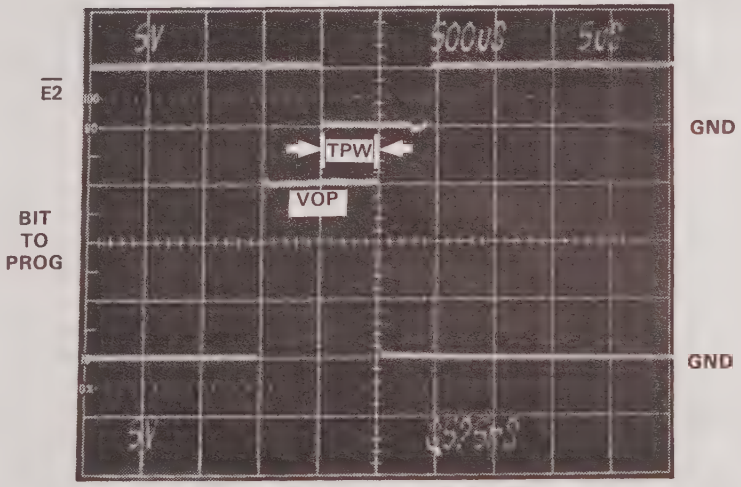
DATA I/O


5V
500uS
50uS
VCCP
VCCN
VCC
GND
E2
GND
5V
0257mS

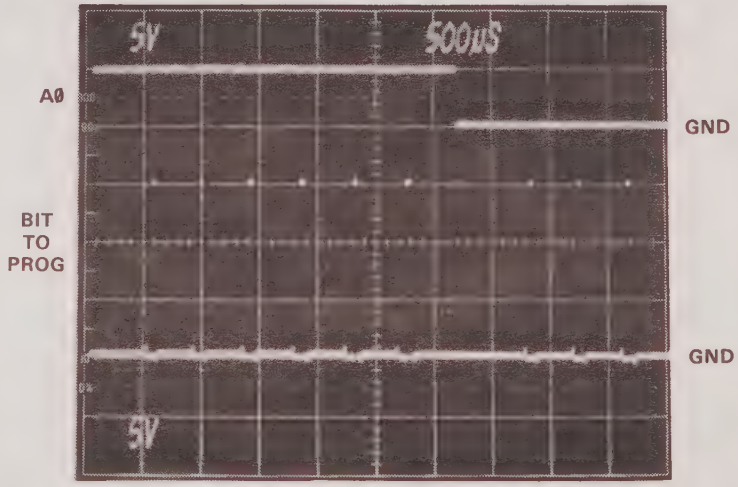
1


5V
500uS
50uS
E2
GND
BIT
TO
PROG
GND
5V
0257mS

2


5V
500uS
E2
GND
TPW
VOP
BIT
TO
PROG
GND
5V

3


5V
500uS
A0
GND
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	8.4	8.8	9.2	V	
	V_{CCN}	4.75	5.0	5.25	V	
	V_{OP}	17.0	17.5	18.0	V	
	T_{PWB}	4.7	5.0	5.3	µs	See Note 4
	T_{PWE}	29.5	30.0	30.5	µs	See Note 4
	Reject		6		Pulses	
	Overprogram		1		Pulse	
	TOP	19.5	20.0	20.5	µs	See Note 5
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.7	0.8	0.9	V	701-1655/TP2
	HIGH LOAD	24.5	25.5	26.5	V	701-1655/TP4
	LOW LOAD	24.5	25.5	26.5	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.3	2.4	2.5	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	6.6	7.1	7.6	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family CF.*
2. *Load RAM with hex 01 for Family D0*
3. *Load V_{CC} with a 100Ω, 2-watt resistor.*
4. *TPW increases from 5 µs to 30 µs in 5 µs incrments.*
5. *The overprogram TPW is 20 µs. This is not shown.*

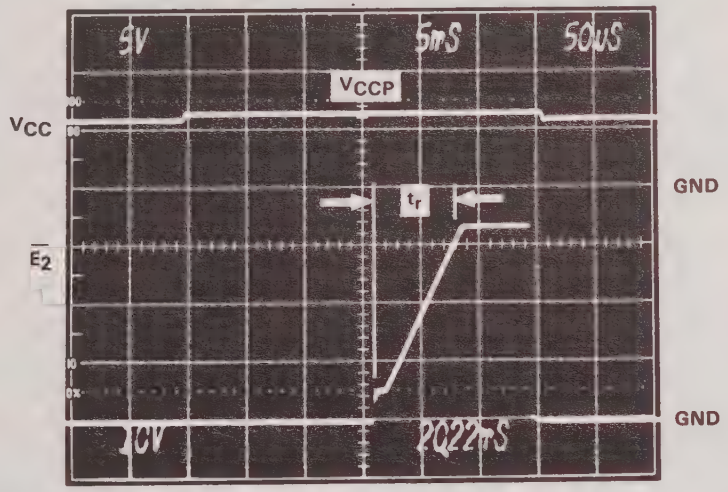
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

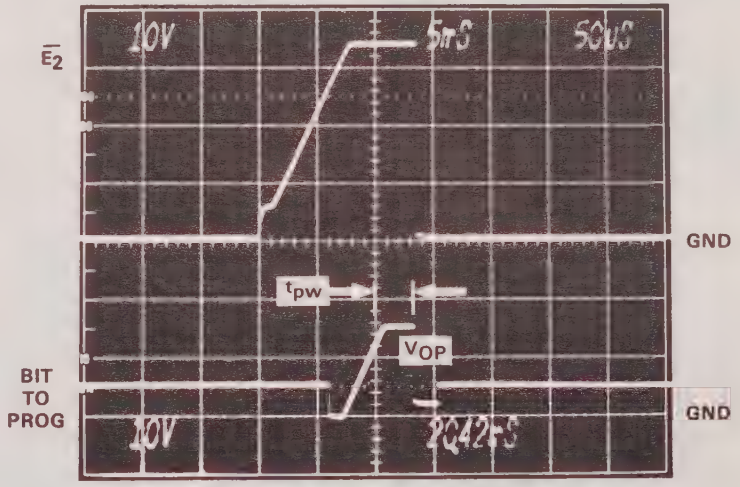
TIMING DIAGRAM

FAMILY CODES CF, D0

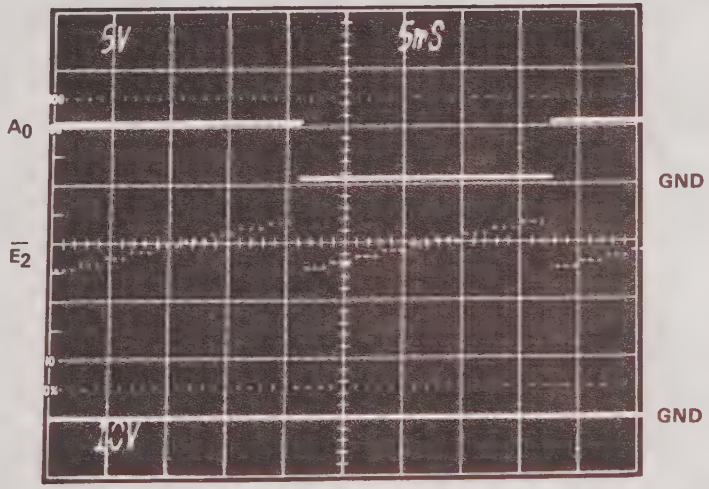
DATA I/O


5V
5mS
50uS
V_{CCP}
V_{CC}
GND
t_r
$\overline{E_2}$
GND
1CV
2Q22mS

1


10V
5mS
50uS
$\overline{E_2}$
GND
t_{pw}
V_{OP}
BIT
TO
PROG
GND
10V
2Q42mS

2


5V
5mS
A_0
GND
$\overline{E_2}$
GND
1CV

3

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.25	5.5	5.75	V	
	V_{OP}	14.5	15.0	15.5	V	
	V_{PPS}	24.0	25.0	26.0	V	See note 3
	V_{PPF}	32.0	33.0	34.0	V	See note 3
	t_{pw}	10		40	μs	
	t_r	53	66	88	μs	See note 4
	t_f					N.A.
	Reject		27		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.1	4.2	4.3	V	
	V_{REF}	0.8	0.9	1.0	V	701-1655/TP2
	HIGH LOAD	18.4	18.9	19.4	V	701-1655/TP4
	LOW LOAD	18.4	18.9	19.4	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.9	6.0	6.1	V	
	V_{REF}	2.9	3.0	3.1	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	5.1	5.6	6.1	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family D1.*
2. *Load RAM with hex 01 for Family D2.*
3. *Vpp starts at 25V and increments to 33V in 1-volt steps with 3 pulses per step.*
4. *TR is measured 10% to 90% of greatest amplitude $\overline{E_2}$ pulse.*

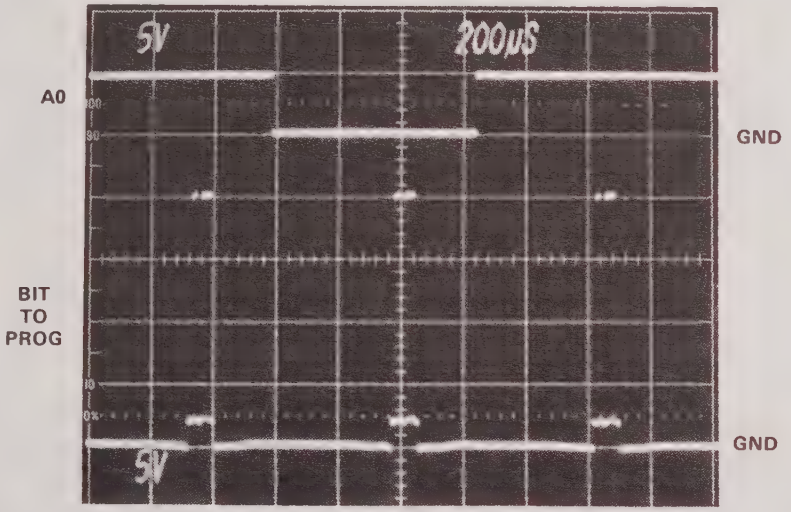
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

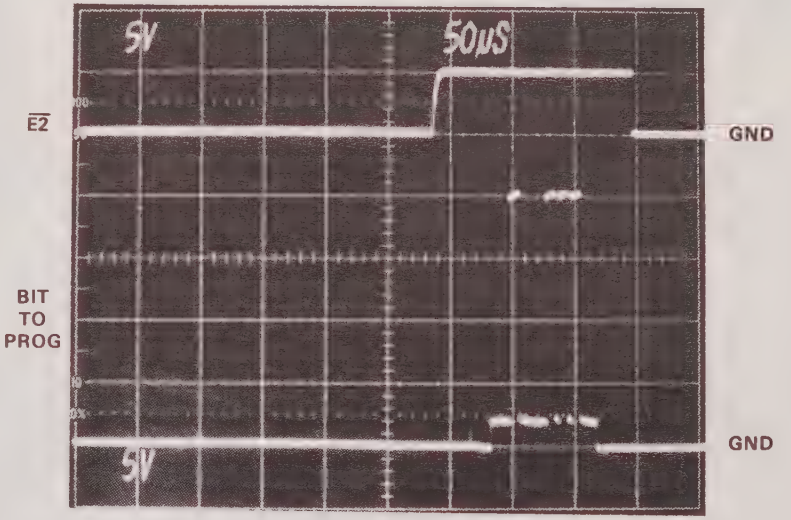
TIMING DIAGRAM

FAMILY CODES D1, D2

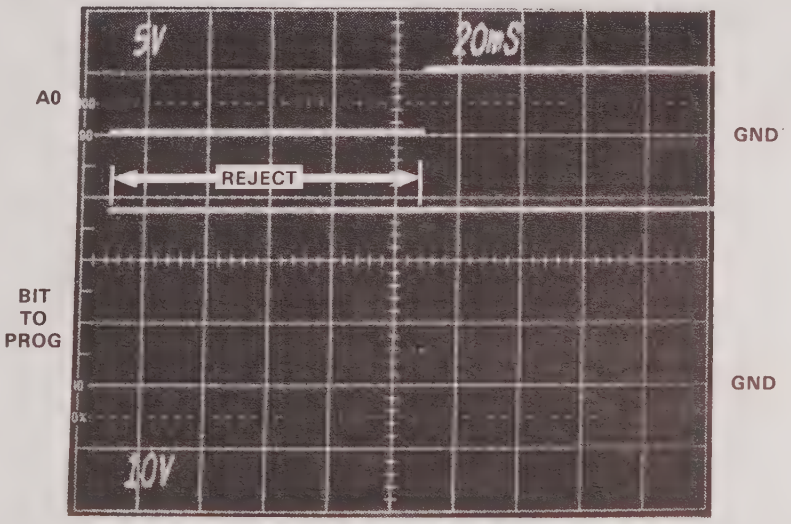
DATA I/O


5V
200µS
A0
GND
BIT
TO
PROG
GND
5V

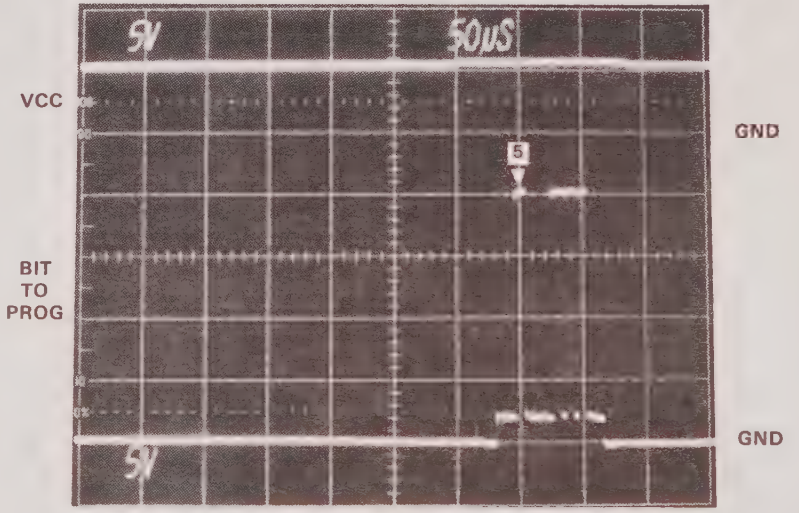
1


5V
50µS
$\overline{E2}$
GND
BIT
TO
PROG
GND
5V

2


5V
20mS
A0
GND
REJECT
BIT
TO
PROG
GND
10V

3


5V
50µS
VCC
GND
5
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.00	5.20	5.40	V	
	VPP					NA
	VOP	27.5	28.0	28.5	V	
	TPW	7.0	7.5	8.0	µs	See Note 3
	T_R	0.21		0.30	µs	
	T_F	0.21		0.30	µs	
	Overprogram		4		Pulses	
	Reject		10,000		Pulses	See Note 4
	Duty Cycle	70	75	80	%	
1ST PASS VERIFY	VCC	4.0	4.1	4.2	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	25.0	26.0	27.0	V	701-1655/TP4
	Low Load	25.0	26.0	27.0	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.4	6.5	6.6	V	
	VREF	6.9	7.0	7.1	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	8.6	9.6	10.6	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family D3.*
2. *Load RAM with hex 01 for Family D4.*
3. *Measurement taken at 10V point of 01 with a 100Ω load.*
4. *10,000 pulses equals 100 ms as shown in photo 3.*
5. *Do not use a wirewound load resistor.*
6. *01 loaded with a 100Ω, 5-watt resistor for photos 1, 2, 4-7.*

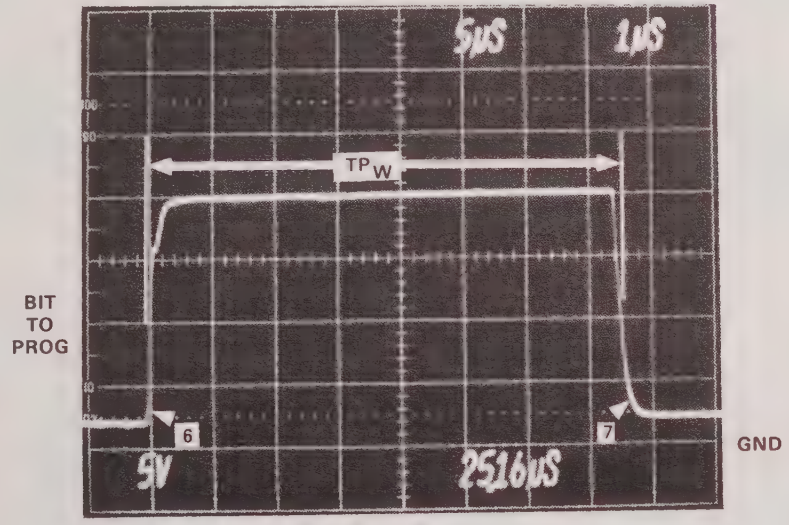
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

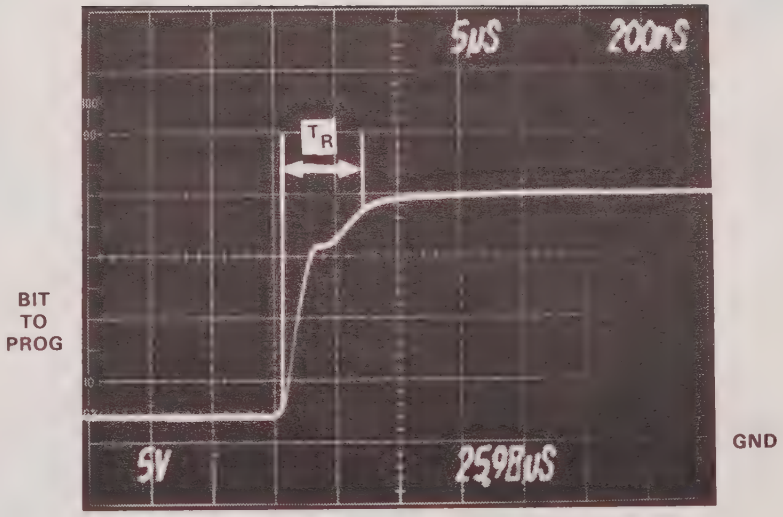
TIMING DIAGRAM

FAMILY CODES D3, D4

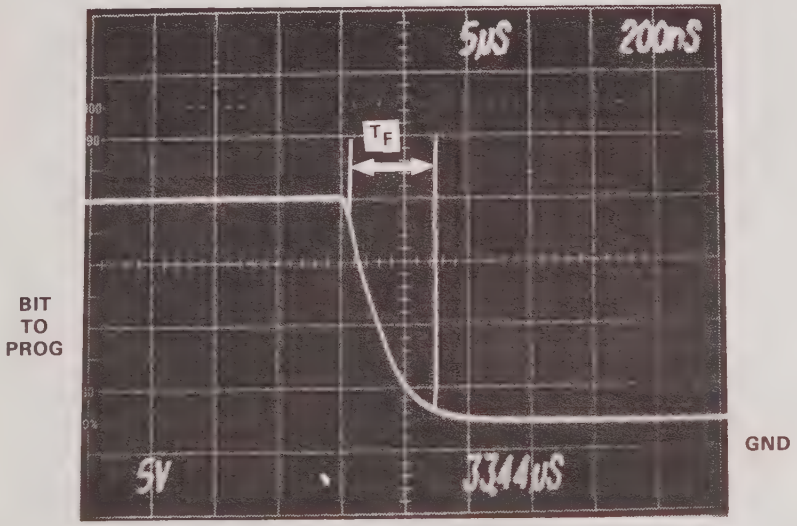
DATA I/O


5µS
1µS
TP W
BIT
TO
PROG
6
7
5V
2516µS
GND

5


5µS
200nS
T R
BIT
TO
PROG
5V
2598µS
GND

6


5µS
200nS
T F
BIT
TO
PROG
5V
3344µS
GND

7

REVISIONS

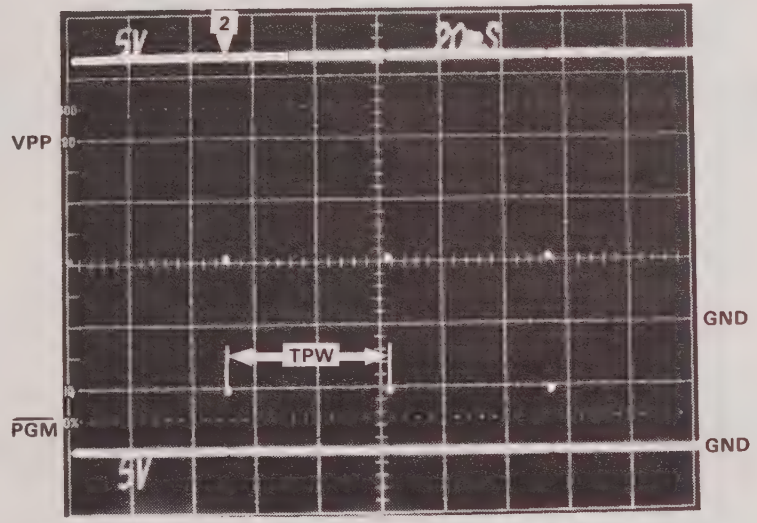
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CJJ	3/84

Sheet 2 of 2

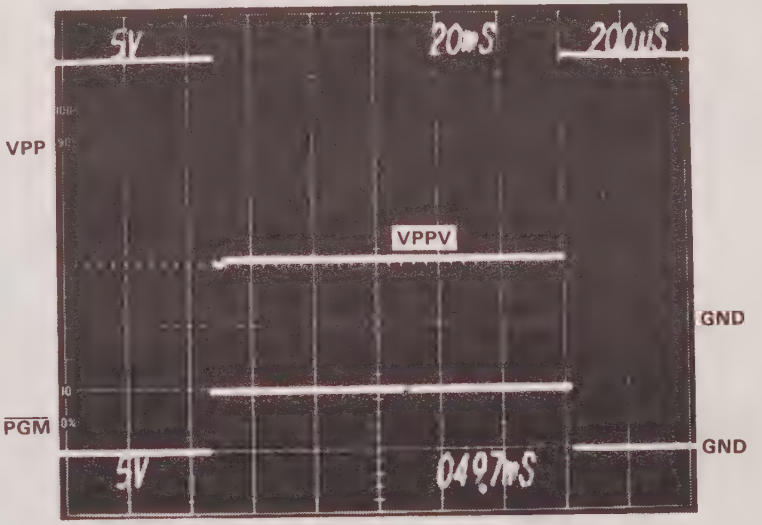
TIMING DIAGRAM

FAMILY CODES D3, D4

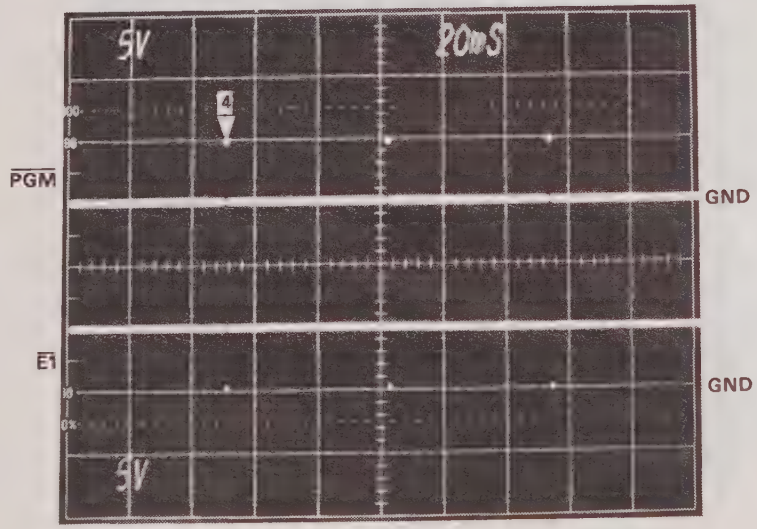
DATA I/O


5V
2
20mS
VPP
TPW
GND
PGM
GND
5V

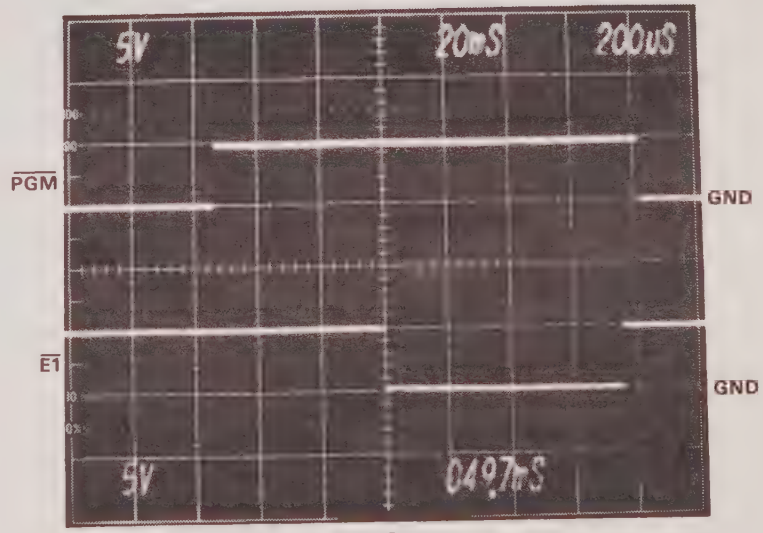
1


5V
20mS
200uS
VPP
VPPV
GND
PGM
GND
5V
049.7mS

2


5V
20mS
4
PGM
GND
E1
GND
5V

3


5V
20mS
200uS
PGM
GND
E1
GND
5V
049.7mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not shown
	VOP					NA
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	49.0	50.0	51.0	ms	
	TR					NA
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family D5.*
2. *Load RAM with hex 01 for Family D6 and bit-to-prog waveform becomes bit-no-prog waveform.*

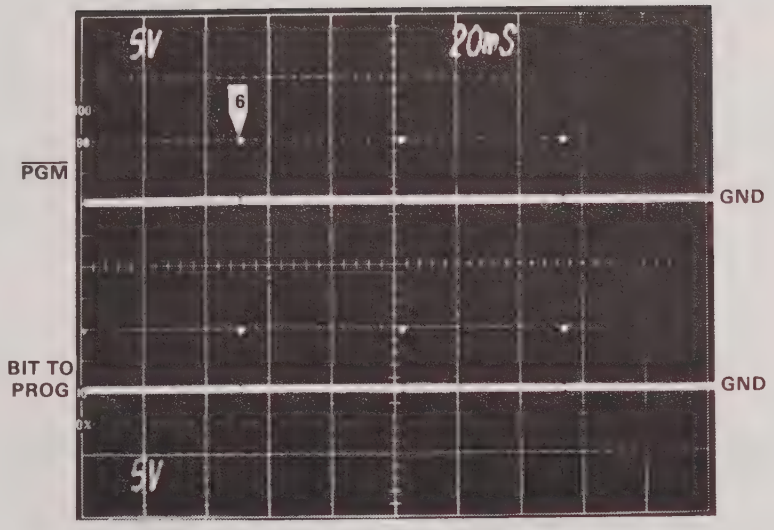
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

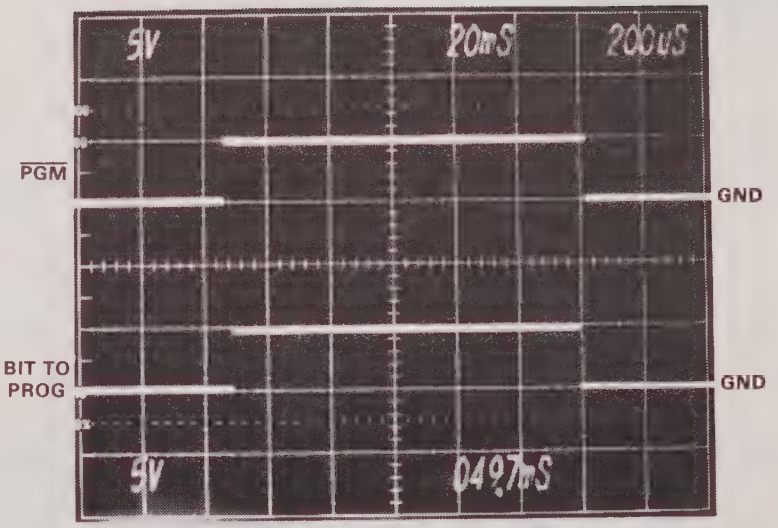
TIMING DIAGRAM

FAMILY CODES D5, D6

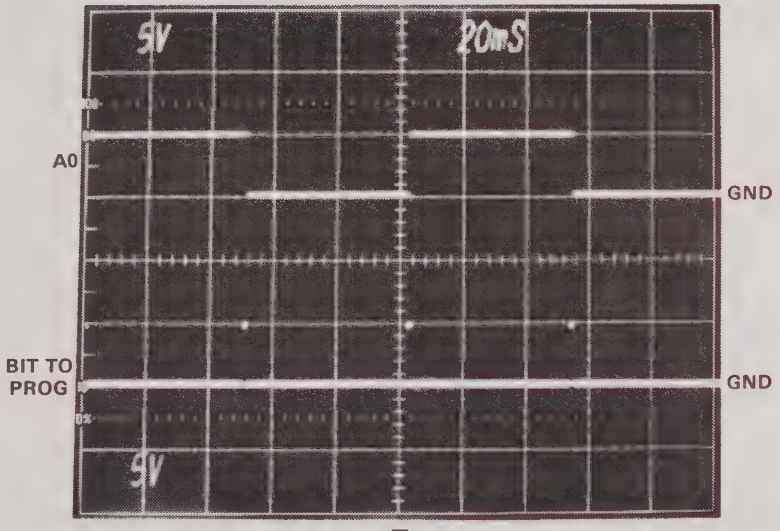
DATA I/O


5V
20mS
6
PGM
GND
BIT TO
PROG
GND
5V

5


5V
20mS
200uS
PGM
GND
BIT TO
PROG
GND
5V
049.7mS

6


5V
20mS
A0
GND
BIT TO
PROG
GND
5V

7

B-269
981-0001

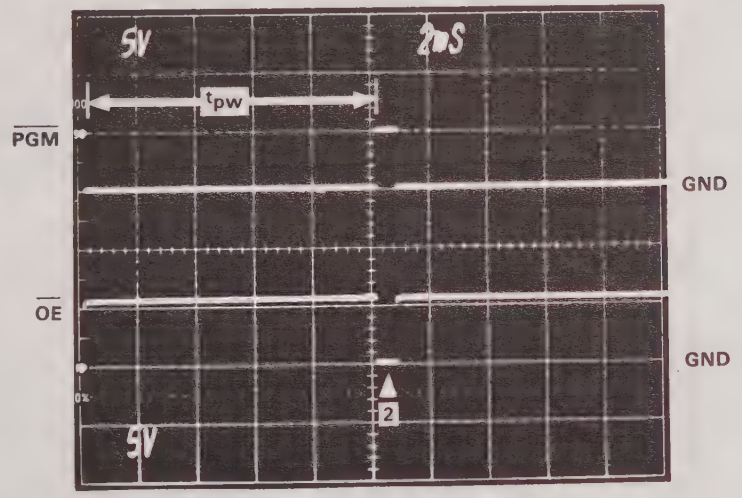
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTB	3/84

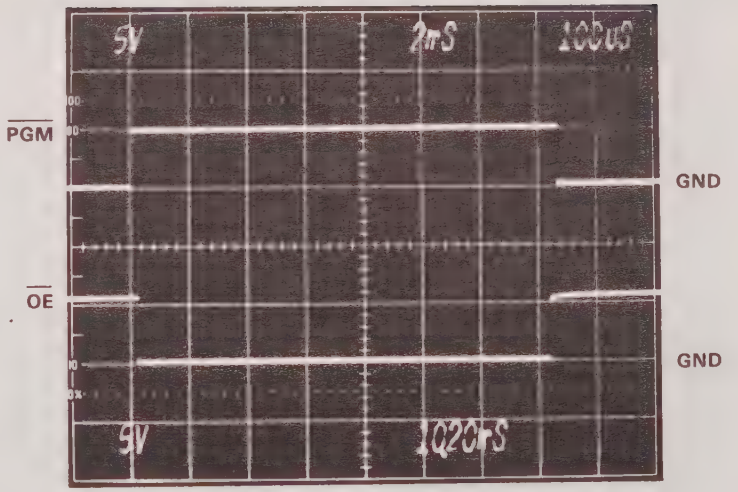
TIMING DIAGRAM

FAMILY CODES D5, D6

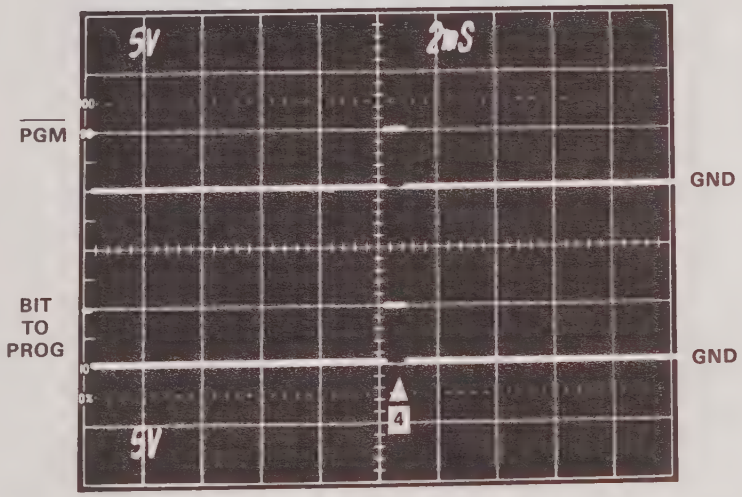
DATA I/O


5V
2mS
t_{pw}
PGM
GND
OE
GND
2
5V

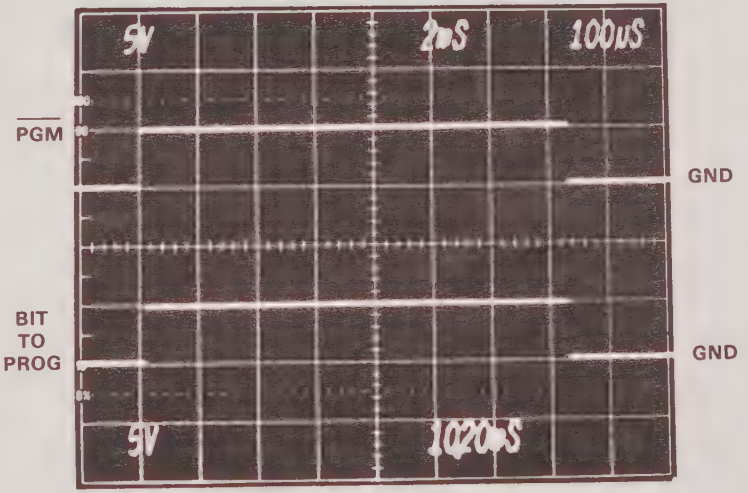
1


5V
2mS
100uS
PGM
GND
OE
GND
5V
1020FS

2


5V
2mS
PGM
GND
BIT
TO
PROG
GND
4
5V

3


5V
2mS
100uS
PGM
GND
BIT
TO
PROG
GND
5V
1020uS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	9.5	10.0	10.5	ms	
	t_r					N.A.
	t_{ew}	95	100	105	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.5	4.6	4.7	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	5.0	5.5	6.0	V	701-1655/TP4
	LOW LOAD	5.0	5.5	6.0	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.3	5.4	5.5	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	7.3	7.8	8.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family D7.*
2. *Load RAM with hex 01 for Family D8.*
3. *Photo 6 shows chip erase.*

REVISIONS

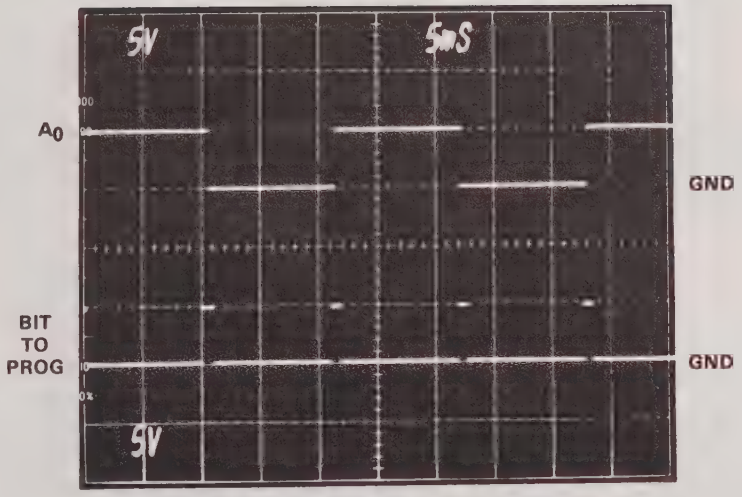
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	5/84

Sheet 1 of 2

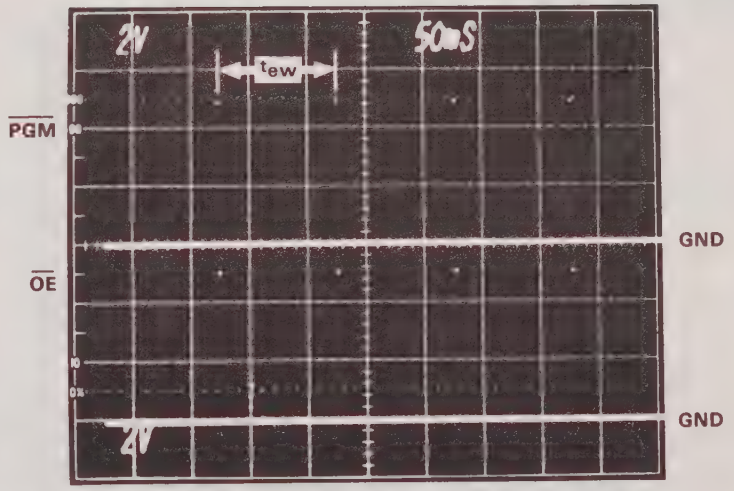
TIMING DIAGRAM

FAMILY CODES D7, D8

DATA I/O



5



6

B-273
981-0001

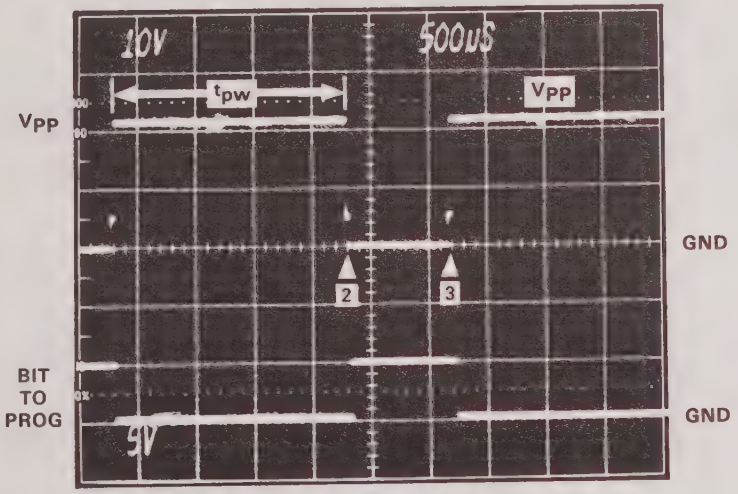
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

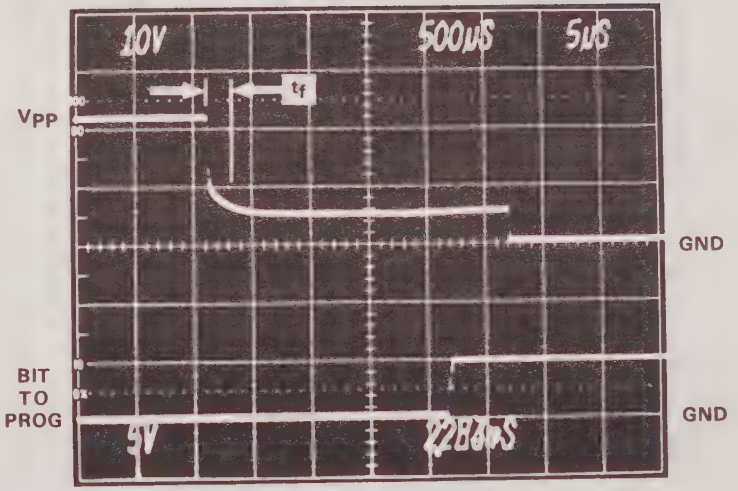
TIMING DIAGRAM

FAMILY CODES D7, D8

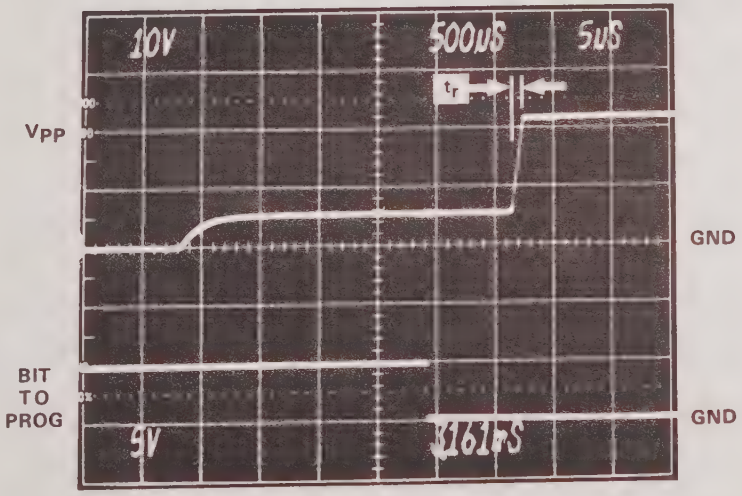
DATA I/O


10V
500uS
tpw
VPP
VPP
GND
2
3
BIT
TO
PROG
GND
5V

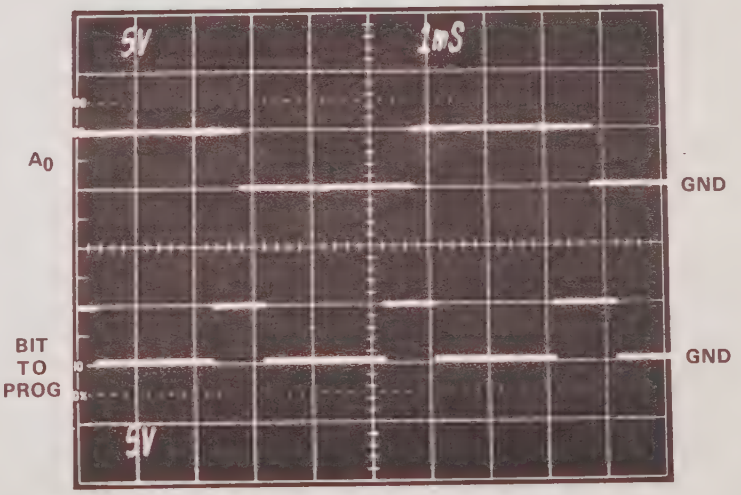
1


10V
500uS
5uS
tf
VPP
GND
BIT
TO
PROG
GND
5V

2


10V
500uS
5uS
tr
VPP
GND
BIT
TO
PROG
GND
5V

3


5V
1mS
A0
GND
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	20.5	21.0	21.5	V	
	V_{PPV}					N.A.
	t_{pw}	1.9	2.0	2.1	ms	
	t_r	0.5		2.0	μs	
	t_f	0.5		5.0	μs	
	Reject		20		PASSES	
	Overprogram		5		PASSES	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.4	0.5	0.6	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.3	2.4	2.5	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	6.5	7.0	7.5	V	701-1655/TP3

NOTES

1. Load RAM with hex FE for Family D9
2. Load RAM with hex 01 for Family DA.

REVISIONS

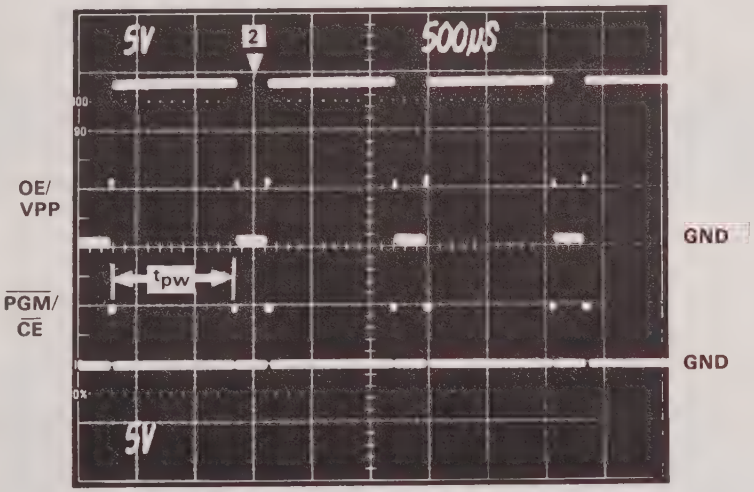
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

Sheet 1 of 1

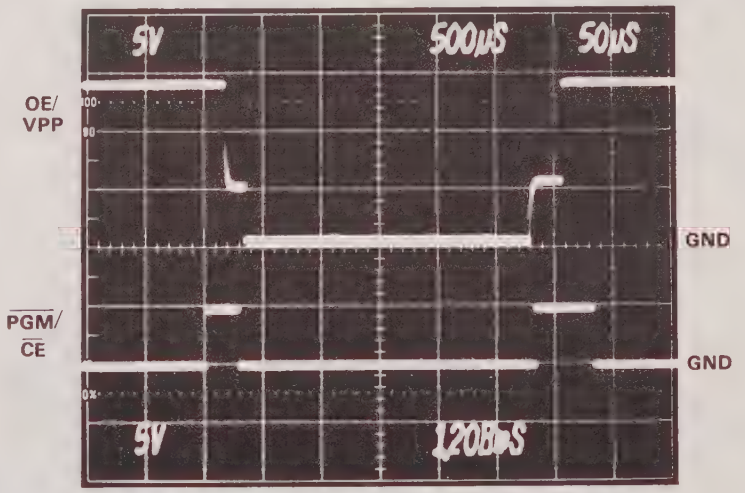
TIMING DIAGRAM

FAMILY CODES D9, DA

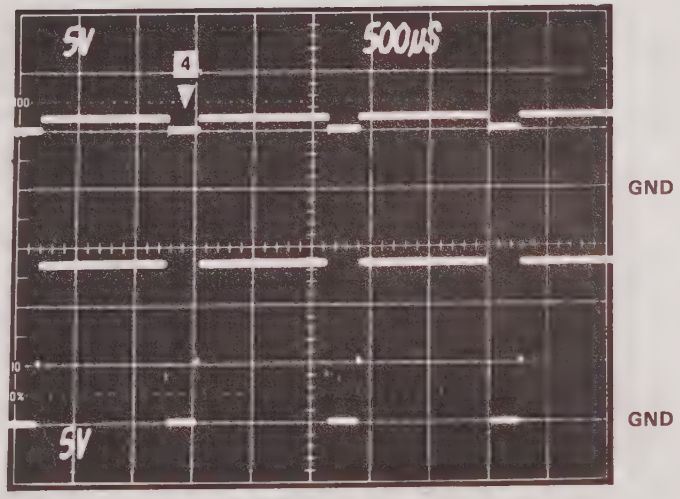
DATA I/O


5V
2
500µS
OE/
VPP
GND
tpw
PGM/
CE
GND
5V

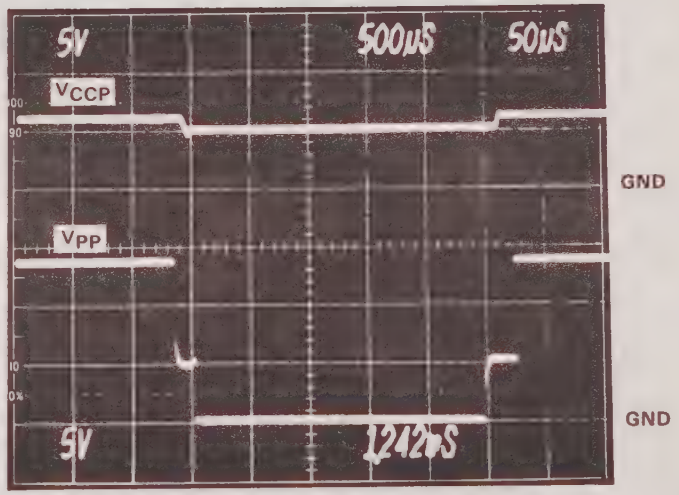
1


5V
500µS
50µS
OE/
VPP
GND
PGM/
CE
GND
5V

2


5V
4
500µS
VCC
GND
OE/
VPP
GND
5V

3


5V
500µS
50µS
VCCP
VCC
GND
VPP
OE/
VPP
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.75	6.0	6.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}	12.5	13.0	13.5	V	
	V_{PPV}					N.A.
	t_{pw}		1		ms	
	t_r					N.A.
	t_f					N.A.
	Reject		25		PULSES	
	Overprogram		1		PULSES	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family DD.*
2. *Load RAM with hex 01 for Family DE.*

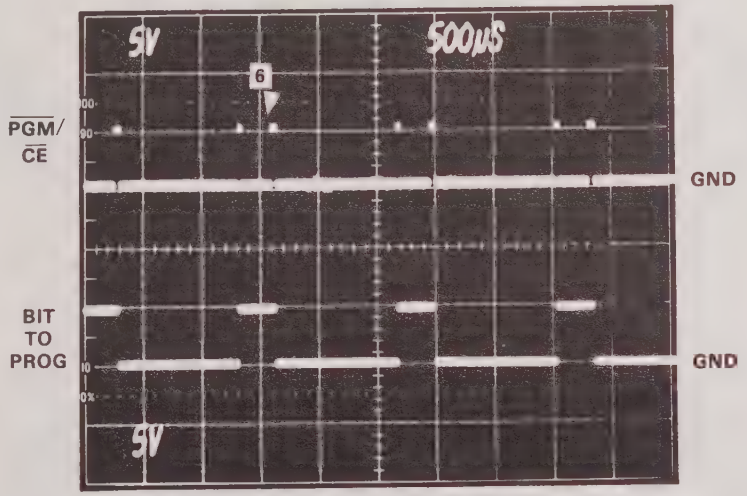
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

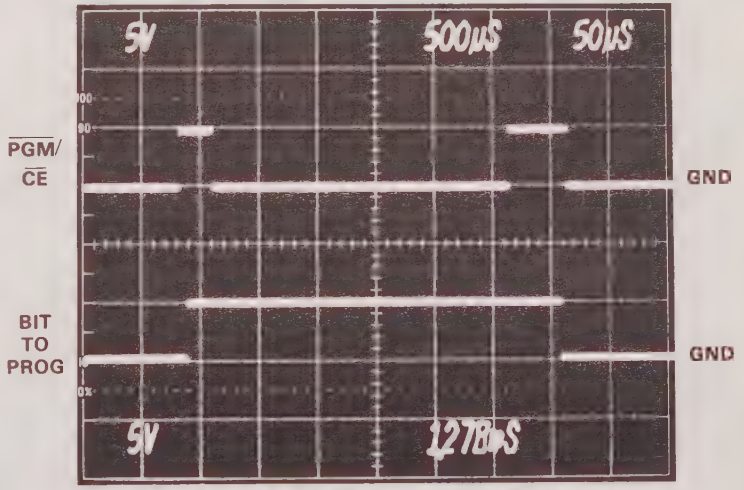
TIMING DIAGRAM

FAMILY CODES DD, DE

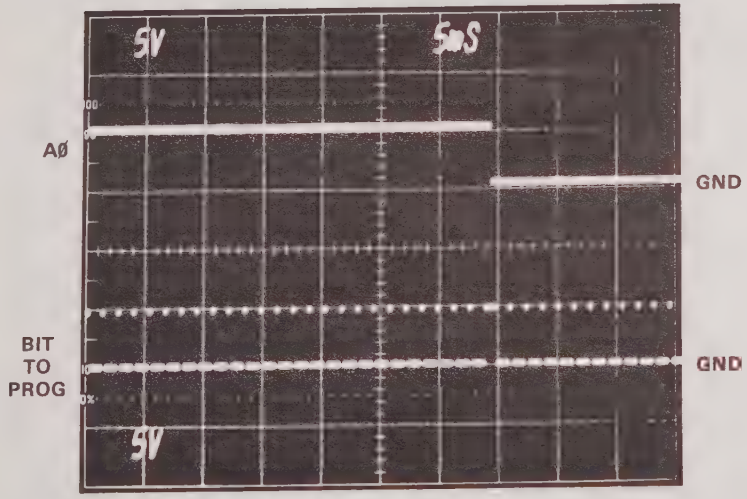
DATA I/O


5V
500µS
6
PGM/
CE
GND
BIT
TO
PROG
GND
5V

5


5V
500µS
50µS
PGM/
CE
GND
BIT
TO
PROG
GND
5V
127µS

6


5V
5µS
AØ
GND
BIT
TO
PROG
GND
5V

7

B-279
981-0001

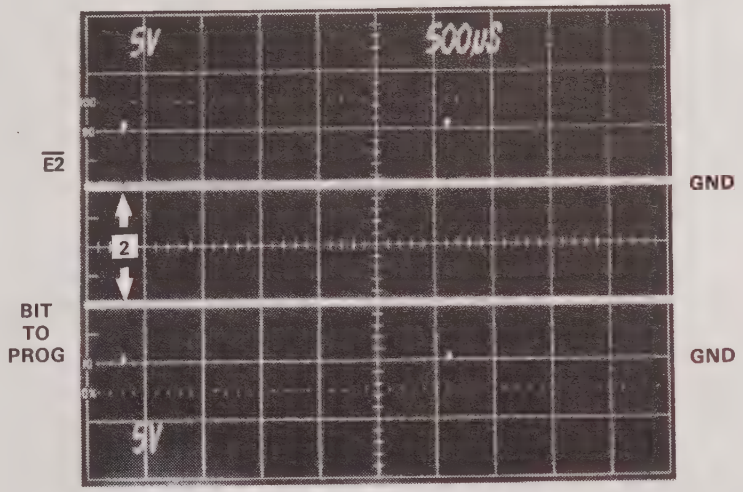
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

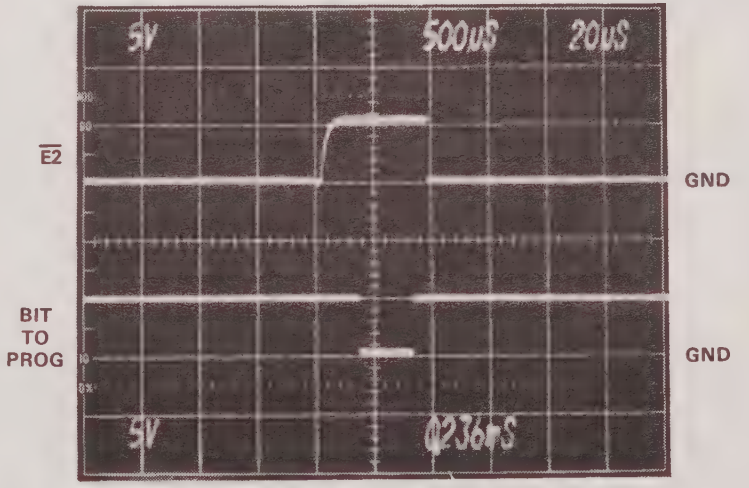
TIMING DIAGRAM

FAMILY CODES DD, DE

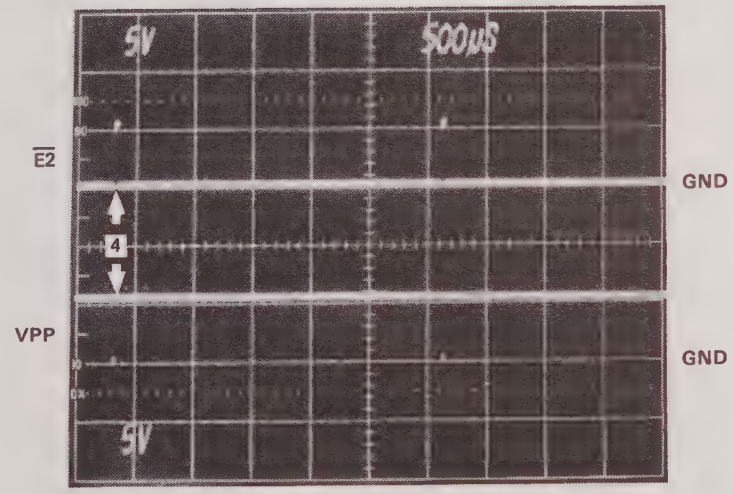
DATA I/O


5V
500uS
E2
GND
2
BIT
TO
PROG
GND
5V

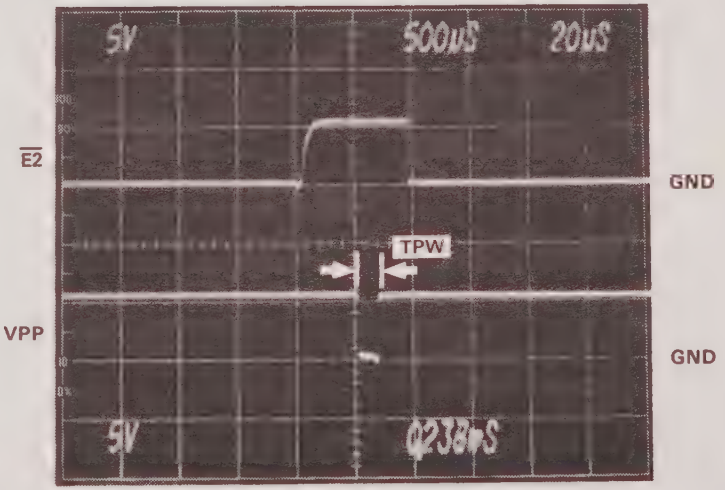
1


5V
500uS
20uS
E2
GND
BIT
TO
PROG
GND
5V
@236uS

2


5V
500uS
E2
GND
4
VPP
GND
5V

3


5V
500uS
20uS
E2
GND
TPW
VPP
GND
5V
@238uS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VEP	20.5	21.0	21.5	V	
	VEE	11.5	12.0	12.5	V	
	TPW	150			ns	
	TEW	9.0		15.0	ms	
	Reject		1		Pulse	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.3	0.4	0.5	V	701-1655/TP2
	HIGH LOAD	4.7	5.2	5.7	V	701-1655/TP4
	LOW LOAD	4.7	5.2	5.7	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.3	2.4	2.5	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	6.5	7.0	7.5	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family DF.*
2. *Load RAM with hex 01 for Family E0*
3. *Photo 6 shows erase pulse.*

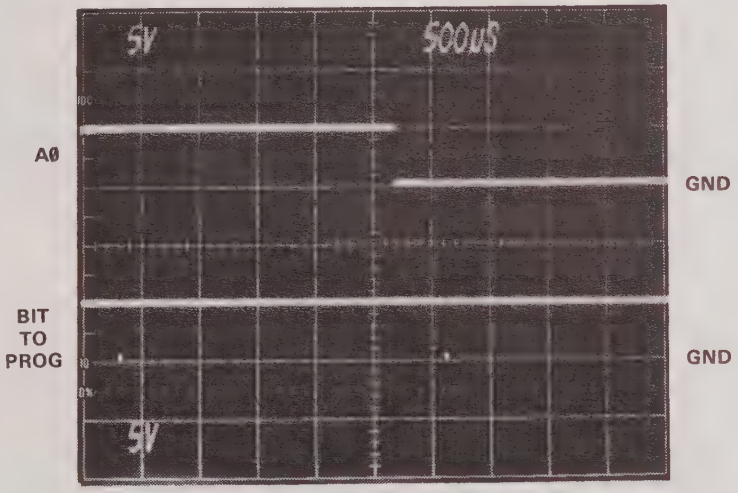
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

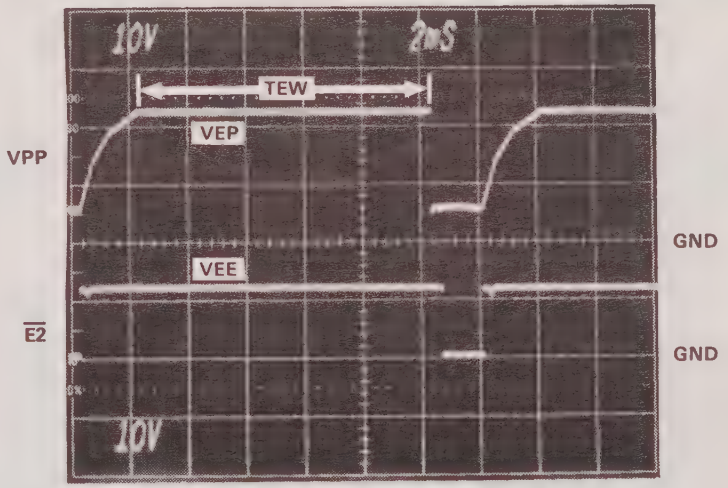
TIMING DIAGRAM

FAMILY CODES DF, E0

DATA I/O


5V
500uS
A0
GND
BIT
TO
PROG
GND
5V

5


10V
2mS
TEW
VEP
VPP
GND
VEE
E2
GND
10V

6

B-283
981-0001

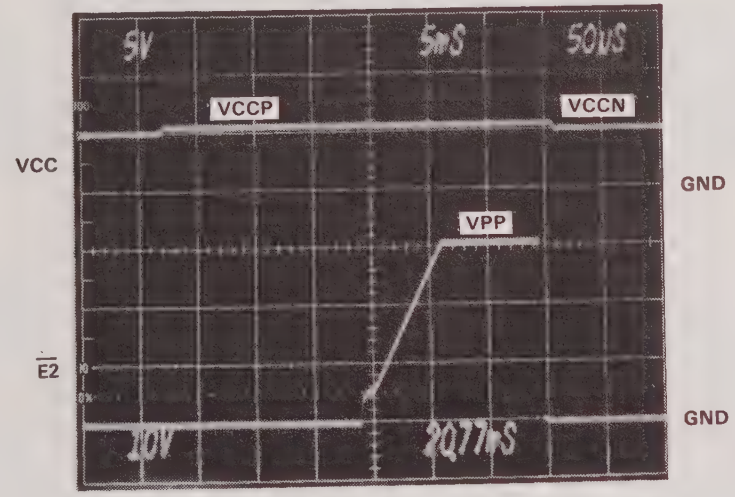
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

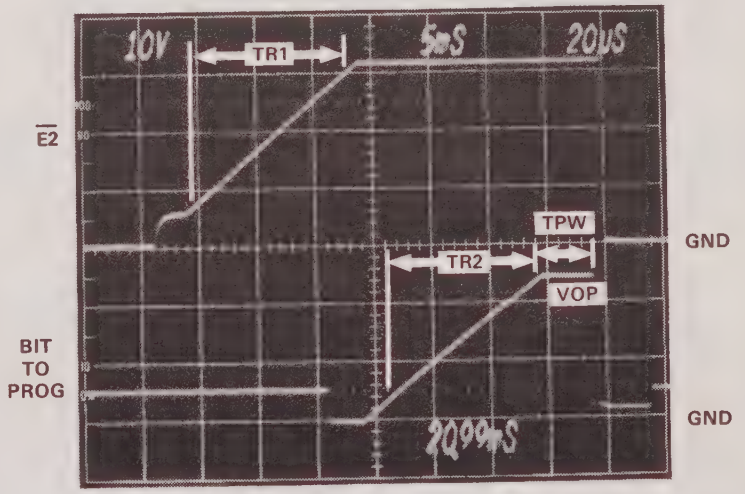
TIMING DIAGRAM

FAMILY CODES DF, E0

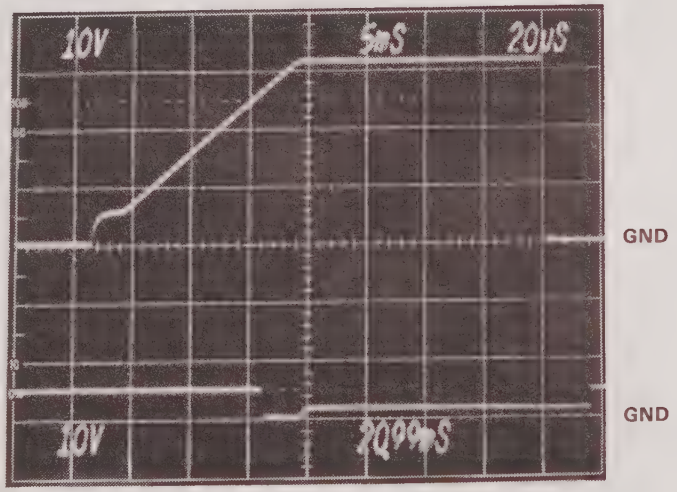
DATA I/O


5V
5mS
50uS
VCCP
VCCN
VCC
GND
VPP
E2
10V
GND

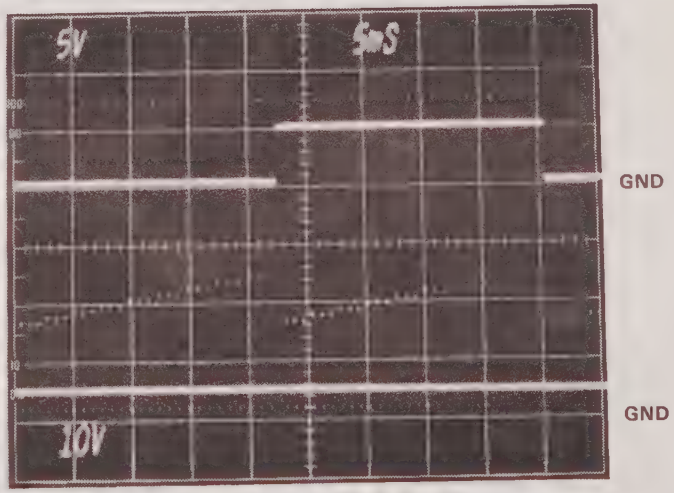
1


10V
TR1
5mS
20uS
E2
TPW
GND
TR2
VOP
BIT
TO
PROG
GND

2


10V
5mS
20uS
E2
GND
BIT
NO
PROG
10V
GND

3


5V
5mS
A0
GND
BIT
TO
PROG
10V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.3	5.5	5.7	V	
	V_{CCN}	4.75	5.0	5.25	V	
	V_{OPB}	16.5	17.0	17.5	V	See Note 3
	V_{OPE}	24.5	25.0	25.5	V	See Note 3
	V_{PPB}	22.5	23.0	23.5	V	See Note 3
	V_{PPE}	30.5	31.0	31.5	V	See Note 3
	T_{PW}	10.0		40.0	μs	See Note 4
	T_{R1}	50	63	82	μs	See Note 5
	T_{R2}	40	50	66	μs	See Note 5
	Reject		27		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	V_{CC}	4.1	4.2	4.3	V	
	V_{REF}	0.8	0.9	1.0	V	701-1655/TP2
	HIGH LOAD	17.9	18.9	19.9	V	701-1655/TP4
	LOW LOAD	17.9	18.9	19.9	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.9	6.0	6.1	V	
	V_{REF}	2.9	3.0	3.1	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.6	5.6	6.6	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family E5.*
2. *Load RAM with hex 01 for Family E6*
3. *These levels increment in 1-volt steps.*
4. *This is measured at the 90% level and all 9 pulse levels must meet this spec.*
5. *This is measured from 10% to 90% of the tallest pulse.*

REVISIONS

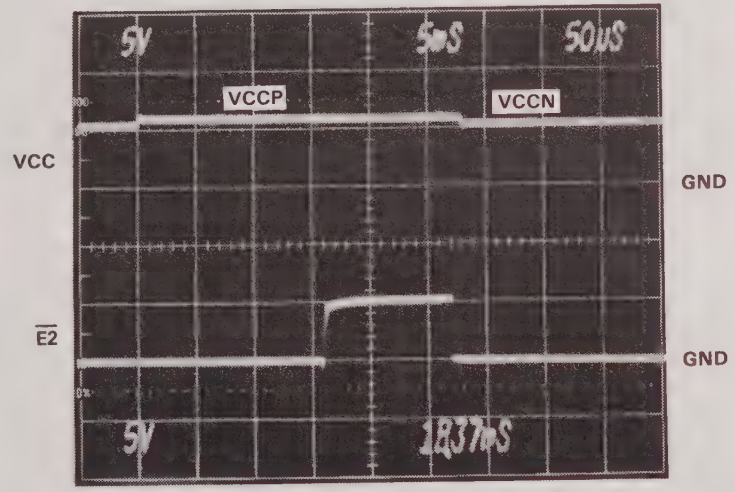
LTR	DESCRIPTION	P.E.	DATE

Sheet 1 of 1

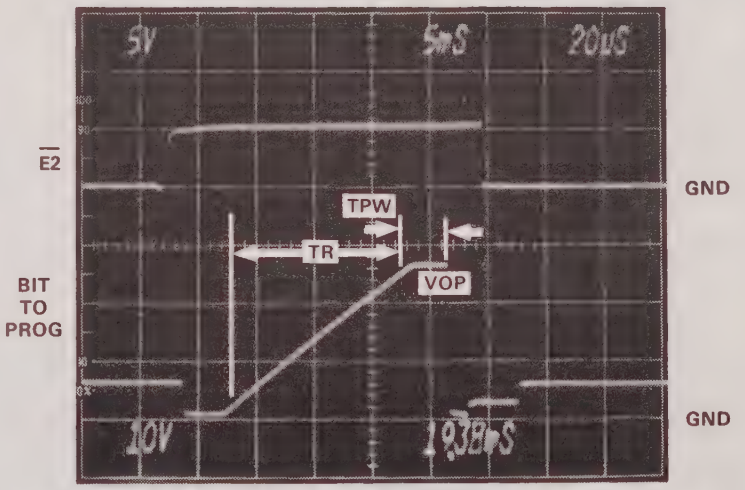
TIMING DIAGRAM

FAMILY CODES E5, E6

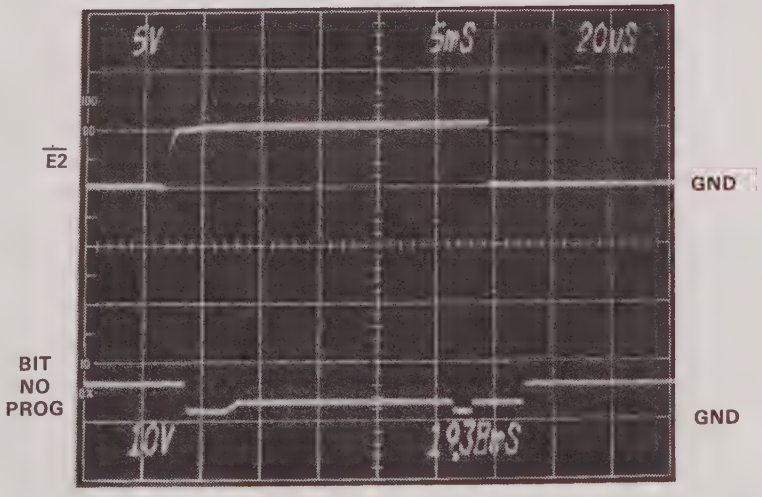
DATA I/O


5V
5mS
50uS
VCCP
VCCN
VCC
GND
E2
GND
5V
1837mS

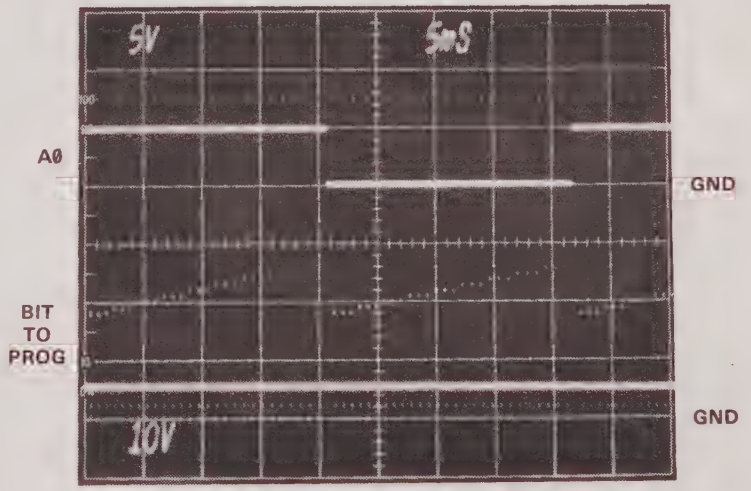
1


5V
5mS
20uS
E2
GND
TPW
TR
VOP
BIT
TO
PROG
GND
10V
1938mS

2


5V
5mS
20uS
E2
GND
BIT
NO
PROG
GND
10V
1938mS

3


5V
5mS
A0
GND
BIT
TO
PROG
GND
10V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.3	5.5	5.7	V	
	V_{CCN}	4.75	5.0	5.25	V	
	V_{OPB}	17.5	18.0	18.5	V	See Note 3
	V_{OPE}	25.5	26.0	26.5	V	See Note 3
	T_{PW}	10.0		40.0	μs	See Note 4
	T_R	42	52	70	μs	See Note 5
	Reject		27		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.1	4.2	4.3	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	HIGH LOAD	17.9	18.9	19.9	V	701-1655/TP4
	LOW LOAD	17.9	18.9	19.9	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	2.9	3.0	3.1	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.4	V	701-1655/TP4
	LOW LOAD	4.6	5.6	6.6	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family E7.*
2. *Load RAM with hex 01 for Family E8*
3. *These levels incrememt in 1-volt steps.*
4. *This is measured at the 90% level, and all 9 levels must meet this spec.*
5. *This is measured from 10% to 90% on the tallest pulse.*

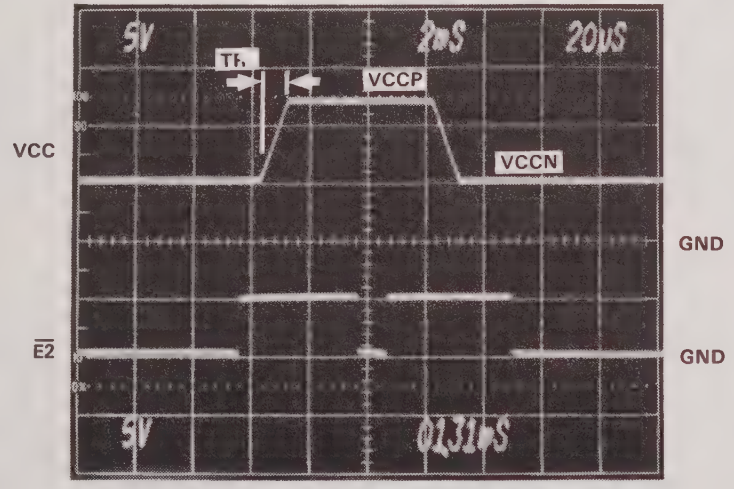
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

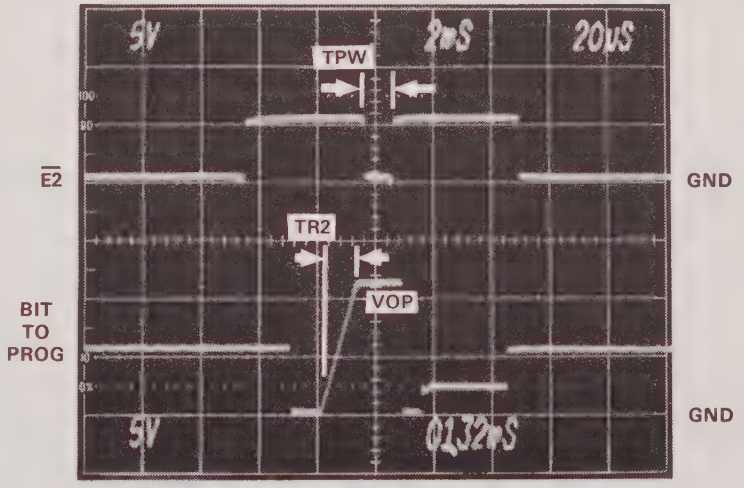
TIMING DIAGRAM

FAMILY CODES E7, E8

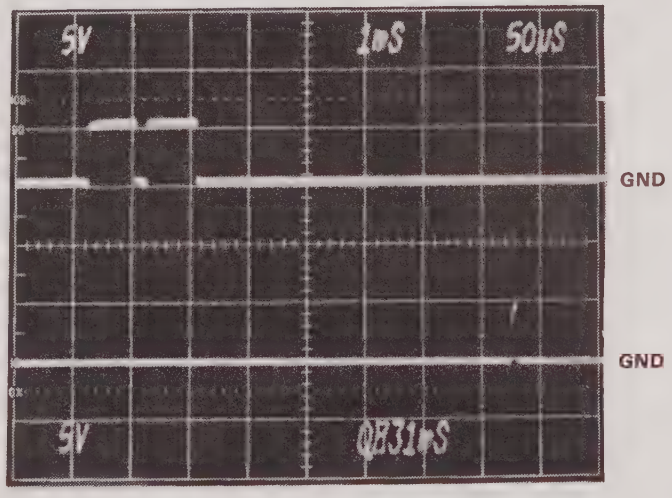
DATA I/O


5V
2mS
20uS
TF.
VCCP
VCCN
VCC
GND
E2
GND
5V
0131mS

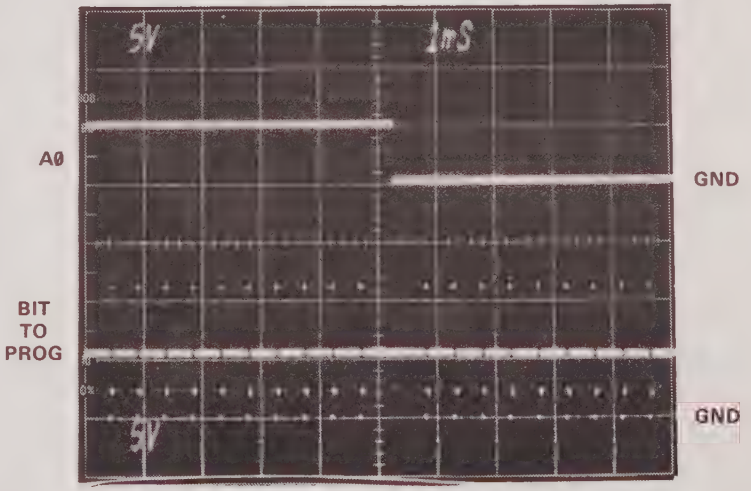
1


5V
2mS
20uS
TPW
E2
GND
TR2
VOP
BIT
TO
PROG
GND
5V
0132mS

2


5V
1mS
50uS
E2
GND
CLK
GND
5V
0831mS

3


5V
1mS
A0
GND
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	11.5	11.7	11.9	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	10.5	11.0	11.5	V	
	TPW	9.0	10.0	11.0	μs	
	TR1	10.0		20.0	μs	See Note 3
	TR2	5.0		18.0	μs	
	Reject		10		Pulses	
	Overprogram		5		Pulses	
1ST PASS VERIFY	VCC	4.2	4.3	4.4	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	HIGH LOAD	7.0	8.0	9.0	V	701-1655/TP4
	LOW LOAD	7.0	8.0	9.0	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	2.9	3.0	3.1	V	701-1655/TP2
	HIGH LOAD	7.8	8.8	9.8	V	701-1655/TP4
	LOW LOAD	7.8	8.8	9.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family EB.*
2. *Load RAM with hex 01 for Family EC*
3. *Load VCC with a 100Ω, 2-watt resistor.*

B-289
981-0001

REVISIONS

LTR	DESCRIPTION	P.E.	DATE

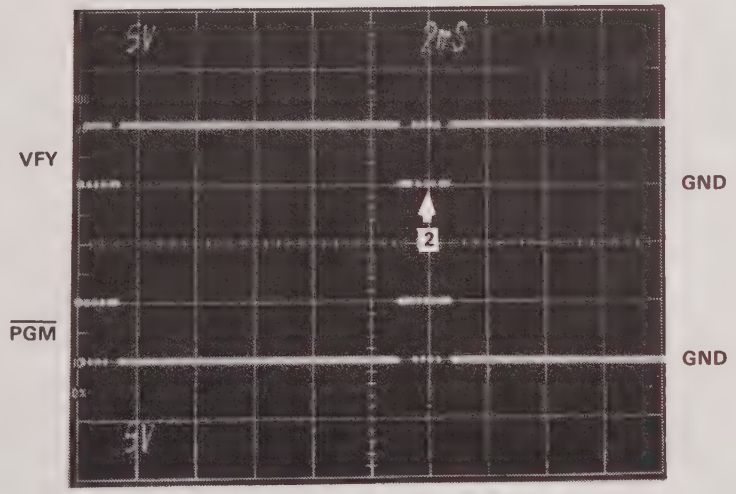
Sheet 1 of 1

TIMING DIAGRAM

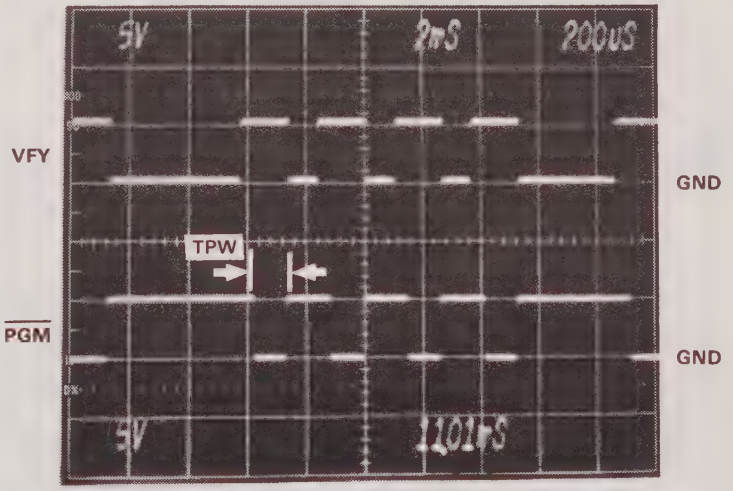
FAMILY CODES EB, EC

DATA I/O

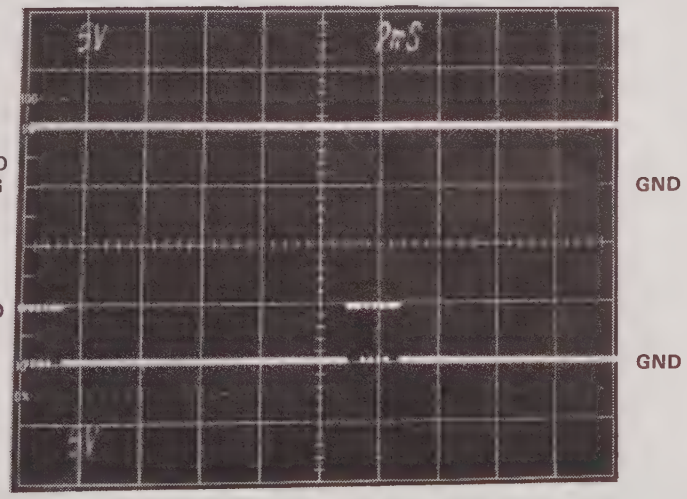
0526 1282


5V
2mS
VFY
GND
2
PGM
GND
5V

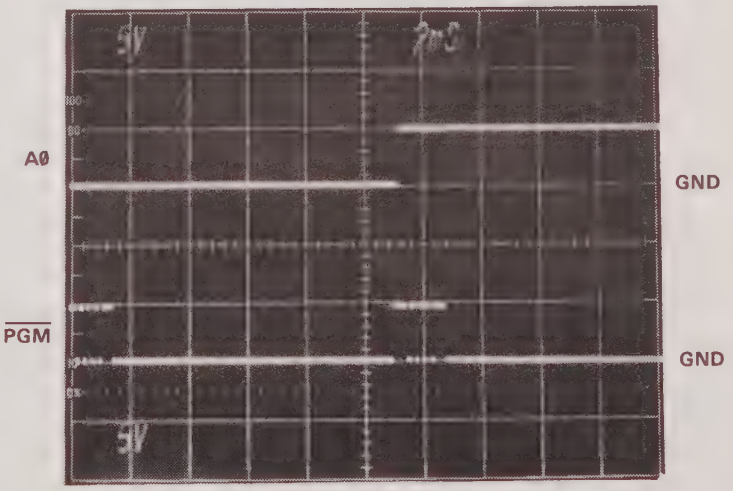
1


5V
2mS
200uS
VFY
GND
TPW
PGM
GND
5V
1101nS

2


5V
2mS
BIT TO PROG "1"
GND
BIT TO PROG "0"
GND
5V

3


5V
2mS
A0
GND
PGM
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VPP	13.0	13.5	14.0	V	Not Shown
	TPW	95	100	105	μs	
	Reject		4		Pulses	
	Overprogram		1		Pulse	See Note 3
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.3	5.3	6.3	V	701-1655/TP4
	LOW LOAD	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex 01 for both families.*
2. *Both zeros and ones have to be programmed.*
3. *The overprogram pulse is 2.4 ms times the number of programming pulses required to program the location.*

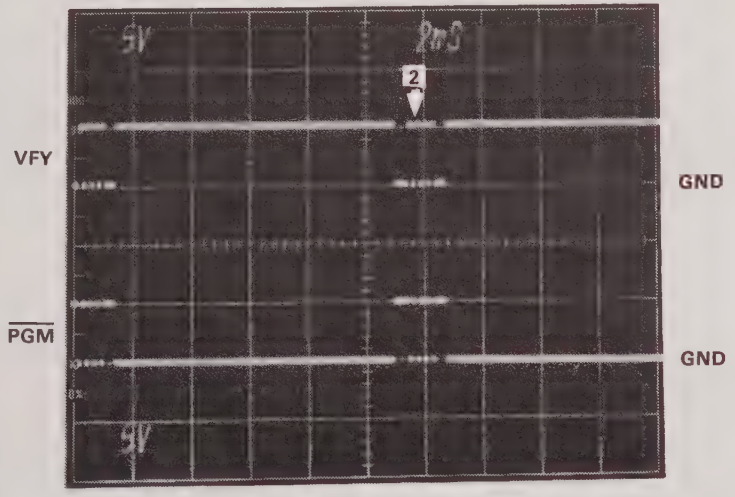
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

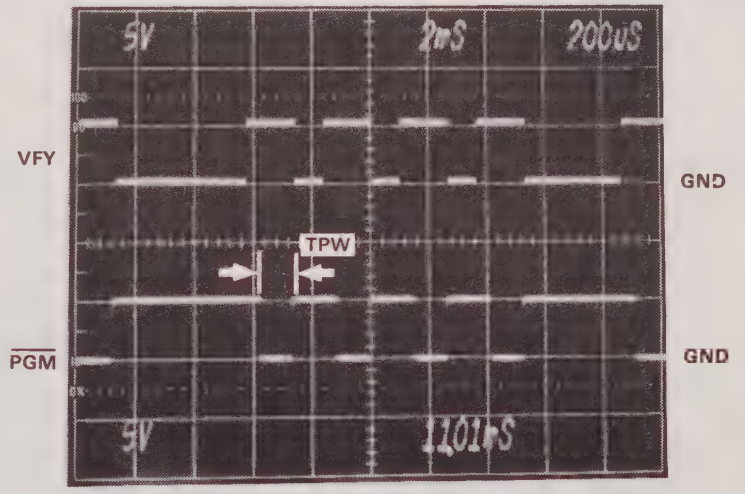
TIMING DIAGRAM

FAMILY CODES ED, EE

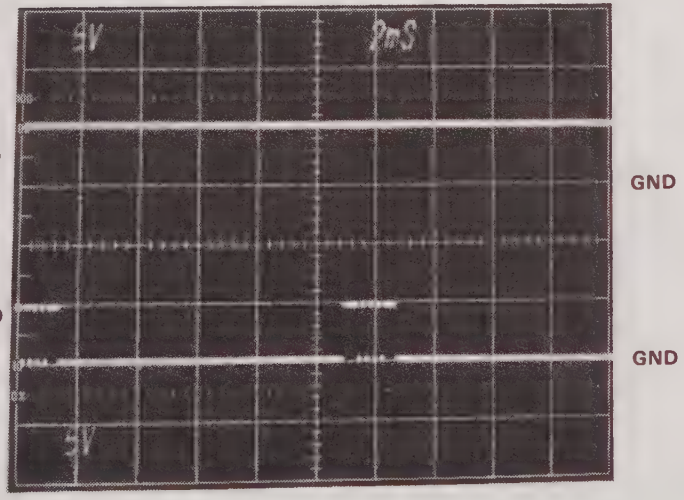
DATA I/O


5V
2mS
2
VFY
GND
PGM
GND
5V

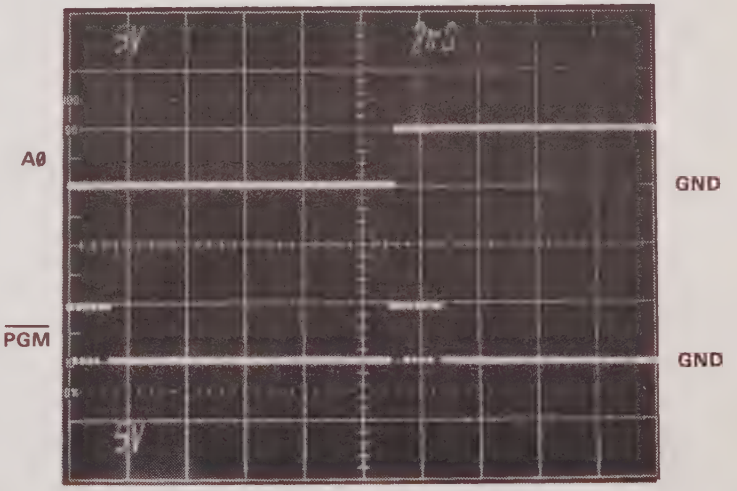
1


5V
2mS
200uS
VFY
GND
TPW
PGM
GND
5V
1101nS

2


5V
2mS
BIT TO PROG "1"
GND
BIT TO PROG "0"
GND
5V

3


5V
2mS
A0
GND
PGM
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VPP	13.0	13.5	14.0	V	Not Shown
	TPW	95	100	105	μs	
	Reject		4		Pulses	
	Overprogram		1		Pulse	See Note 3
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.3	5.3	6.3	V	701-1655/TP4
	LOW LOAD	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex 01 for both families.*
2. *Both zeros and ones have to be programmed.*
3. *The overprogram pulse is 2.4 ms times the number of programming pulses required to program the location.*

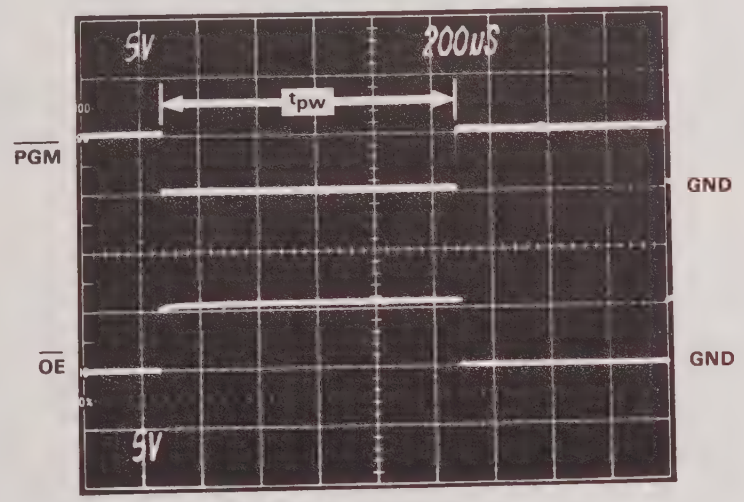
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

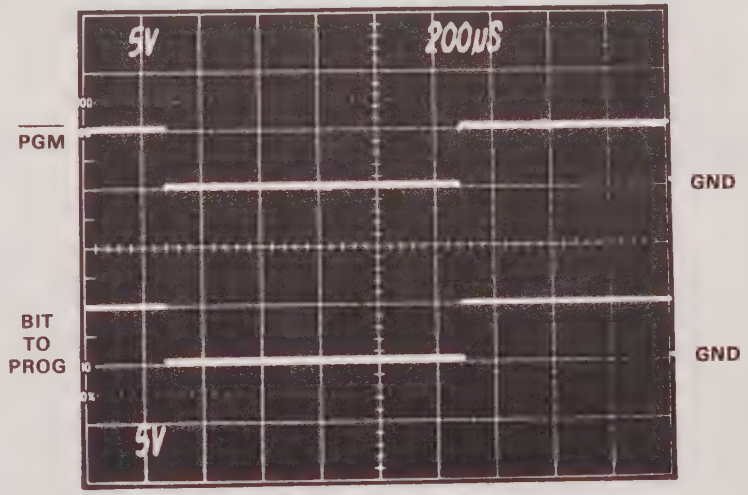
TIMING DIAGRAM

FAMILY CODES EF, F0

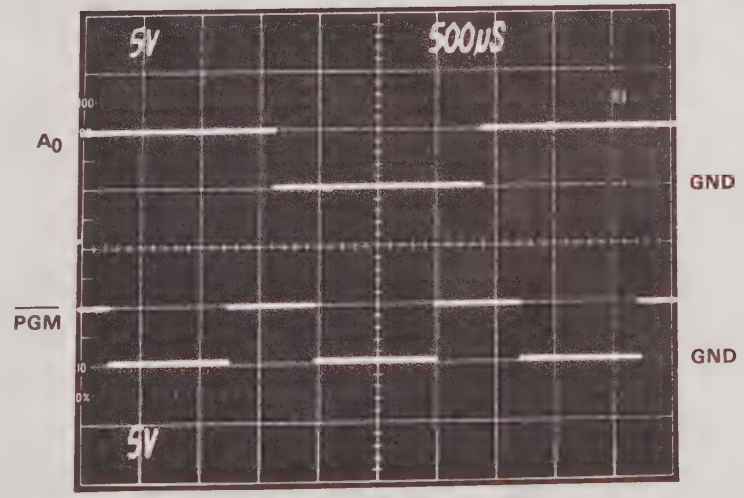
DATA I/O


5V
200uS
t_{pw}
PGM
GND
OE
GND
5V

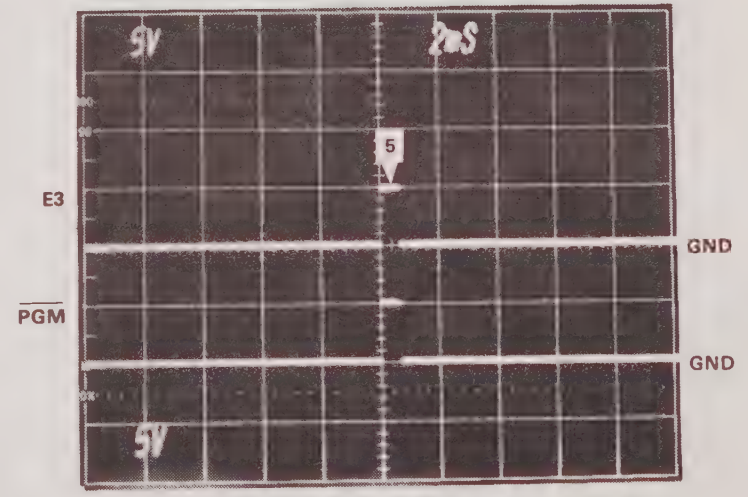
1


5V
200uS
PGM
GND
BIT
TO
PROG
GND
5V

2


5V
500uS
A_0
GND
PGM
GND
5V

3


5V
2mS
5
E3
GND
PGM
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	0.95	1.0	1.052		
				2	ms	
	t_r					N.A.
	t_{ew}	9.5	10.0	10.5	ms	
	t_f					N.A.
	Reject		1		Pulse	
	Overprogram		0		Pulses	
1ST PASS VERIFY	V_{CC}	4.5	4.6	4.7	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	5.0	5.5	6.0	V	701-1655/TP4
	LOW LOAD	5.0	5.5	6.0	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.3	5.4	5.5	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	7.3	7.8	8.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family F1.*
2. *Photos 4-7 are chip-erase photos.*

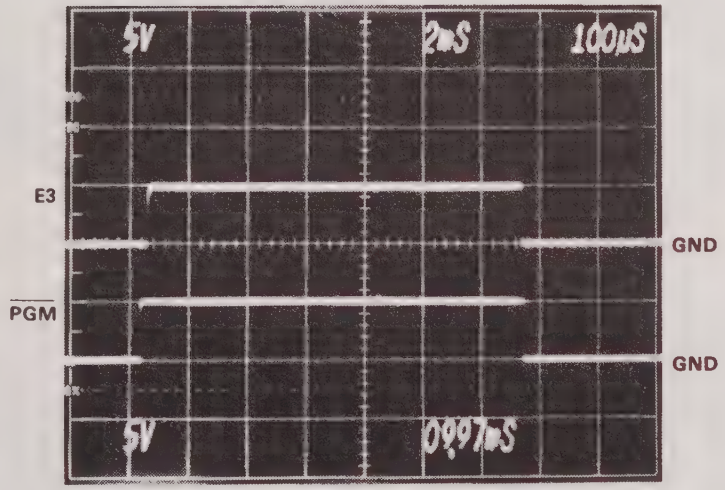
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

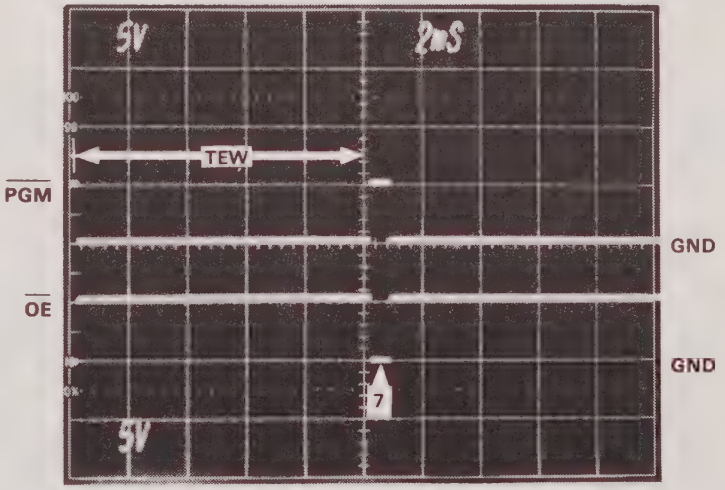
TIMING DIAGRAM

FAMILY CODES F1, F2

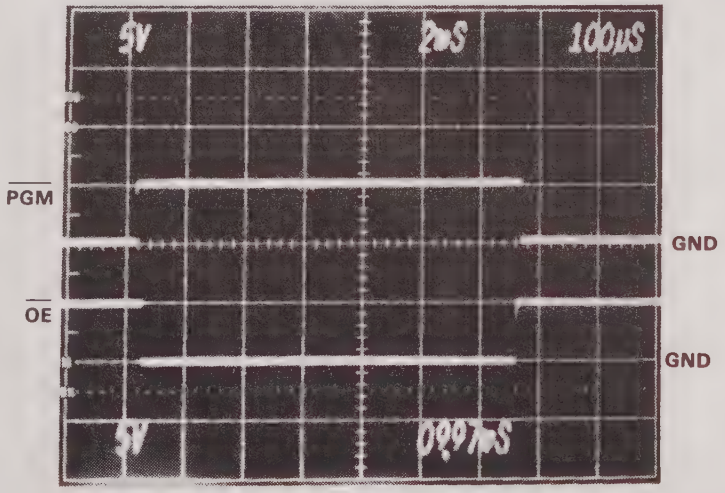
DATA I/O


5V
2mS
100µS
E3
GND
PGM
GND
5V
0.997mS

5


5V
2mS
TEW
PGM
GND
OE
GND
7
5V

6


5V
2mS
100µS
PGM
GND
OE
GND
5V
0.997mS

7

REVISIONS

LTR	DESCRIPTION	P.E.	DATE

Sheet 2 of 2

TIMING DIAGRAM

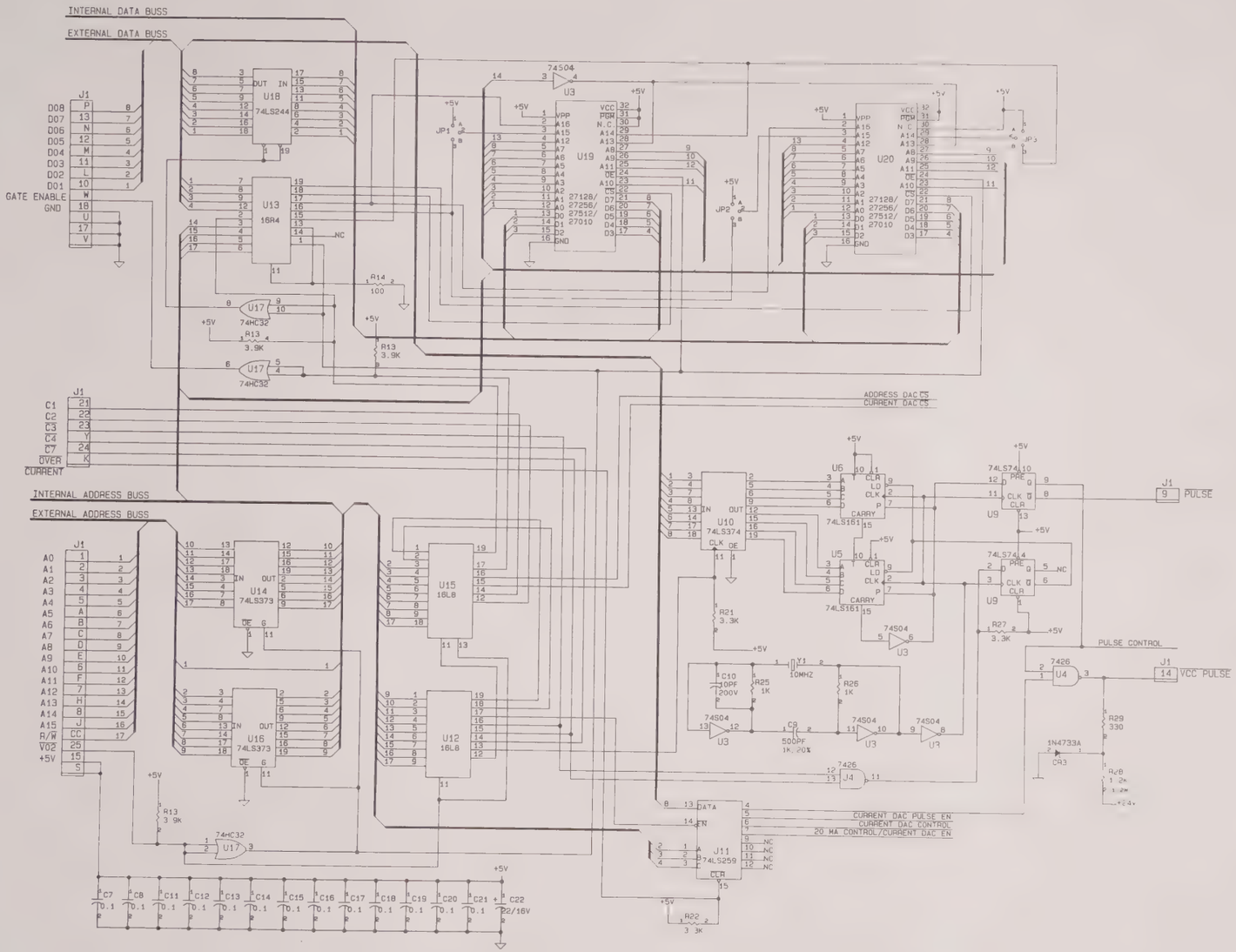
FAMILY CODES F1, F2

DATA I/O

APPENDIX C
SCHEMATICS

30-701-2126	Memory Card
30-701-1655	Address Card
30-702-1659	Socket Card
30-702-1661	Motherboard
30-701-1690	Waveform Generator

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	[illegible]	B.R.	C.T.Z.	9/1/87



P/N 701-2126-001

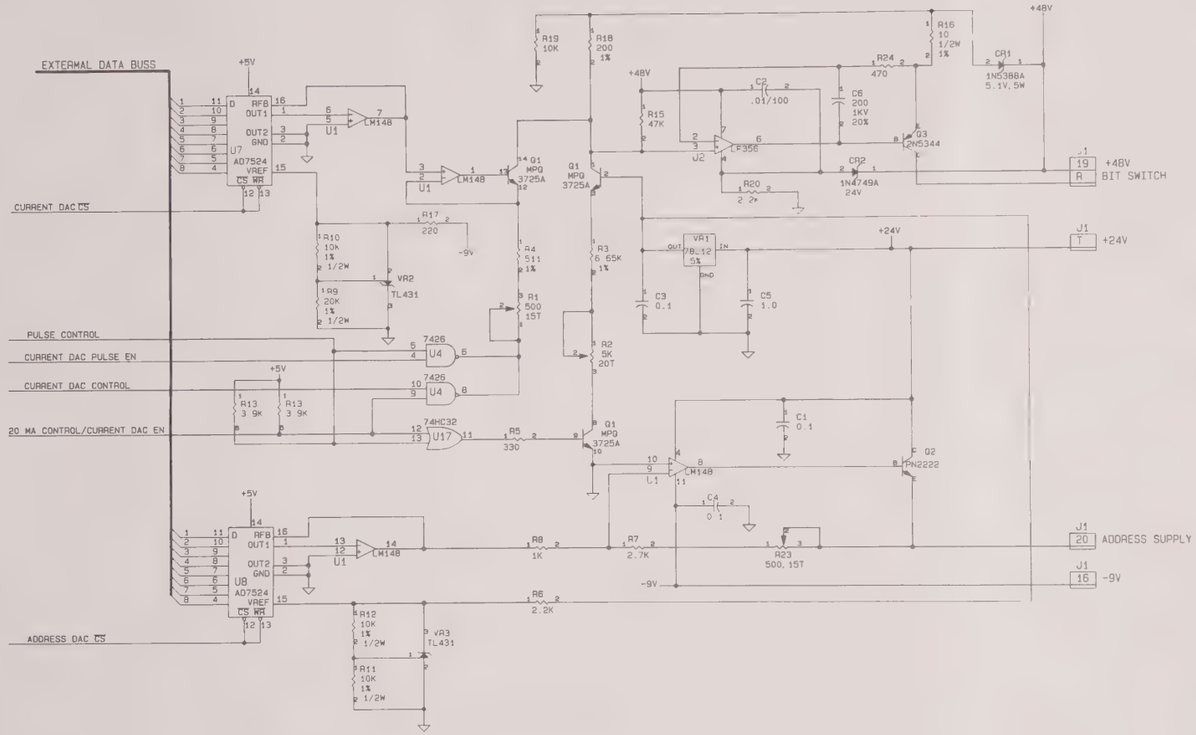
NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V.
3. LAST REFERENCE DESIGNATOR USED: J1, R29, Q3, VR3, CR3, C22, U20, JP3
4. POWER AND GROUND:

REF.DES.	GND	+5V
U3, U4, U9, U17	7	14
U5, U6, U11	8	16
U10, U12-U16, U18	10	20

5. UNUSED GATES:

DRAWN Jaehee Kim	DATE 4/6/87	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O REDMOND, WASH.
CHECKED [illegible]	4/13/87	TOLERANCES, UNLESS OTHERWISE SPECIFIED XX ± XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM, MEMORY BOARD
ELEC ENG [illegible]	4/1/87		
MECH ENG B Valdura	4/13/87		
MFG ENG [illegible]	4/13/87	DO NOT SCALE DRAWING	SIZE D · FSCM NO 54193 · DRAWING NO 30-701-2126
QUAL ASSUR [illegible]	4/13/87		
APPD [illegible]	4/13/87		SCALE — · D.A.D. · SHEET 1 OF 2

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	SEE SHEET ONE	JK	JR	CJ	4/13/87



DRAWN	JAEHEE KIM	DATE	1/13/87
CHECKED	Bill Rigsbee		4/13/87
ELEC ENG			
MECH ENG			
MFG ENG			
QUAL ASSUR			
APPD			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES UNLESS OTHERWISE SPECIFIED
XX ±
XXX ±
ANGULAR

DO NOT SCALE DRAWING

DATA I/O REDMOND, WASH.

TITLE
SCHEMATIC DIAGRAM,
MEMORY BOARD

SIZE	FSCM NO	DRAWING NO
D	54193	30-701-2126

SCALE —— D.A.D SHEET 2 OF 2

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	BV			
B	ECN 4782	CL			2/83
C	INC. ADCN B1 PER ECP 0120	KN			1/19/85
D	INC. ADCN PER ECP 0226 AND CMA 0103	BV	DMS	PS	11/8/86

ADDRESS LATCH

SECONDARY DECODE

DATA LATCH

L.O. ADDRESS LATCH

H.O. ADDRESS LATCH

SOCKET SELECT LATCH

CURRENT SOURCE LATCH

COMPARATOR GATE/MUX

SUPPLY COMPARATORS

DATA LATCH

NOT SHOWN

IC. NO.	+5	GND
U22	PIN14	PIN7
U14	PIN14	PIN7

UNUSED GATES:

NOTES: UNLESS OTHERWISE SPECIFIED

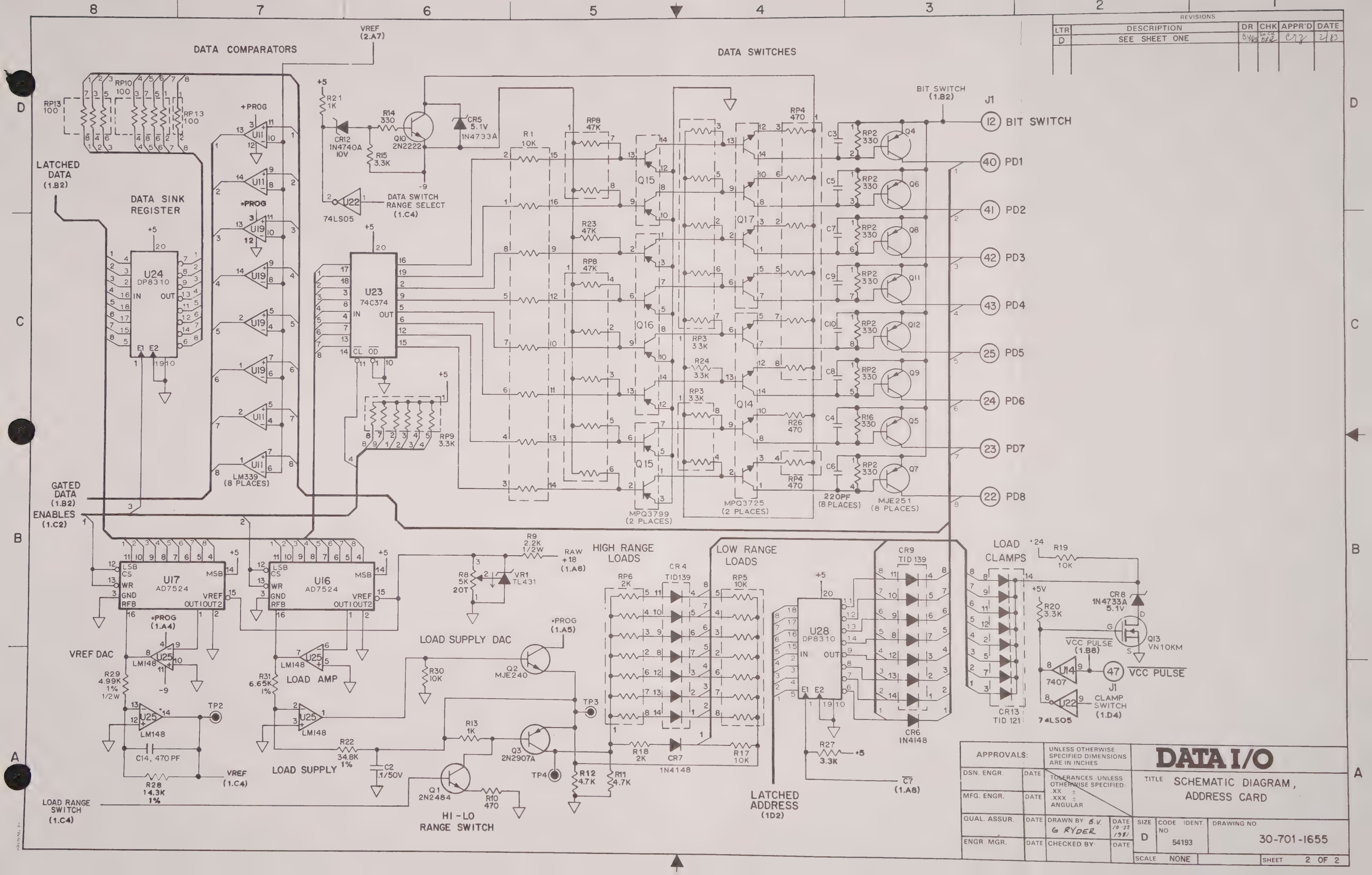
1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 10%.
3. LAST REFERENCE DESIGNATOR USED:
   TP4, CR13, JP1, J1, C18, U29, Q17, R38, RP13, P1
   NOT USED C1, CR11, U5, U7, U8, U9, U10, U12, U13, U15, R25, CR10
4. DELETED AT REV. B.

5 > JP1 INSTALLED IN -003

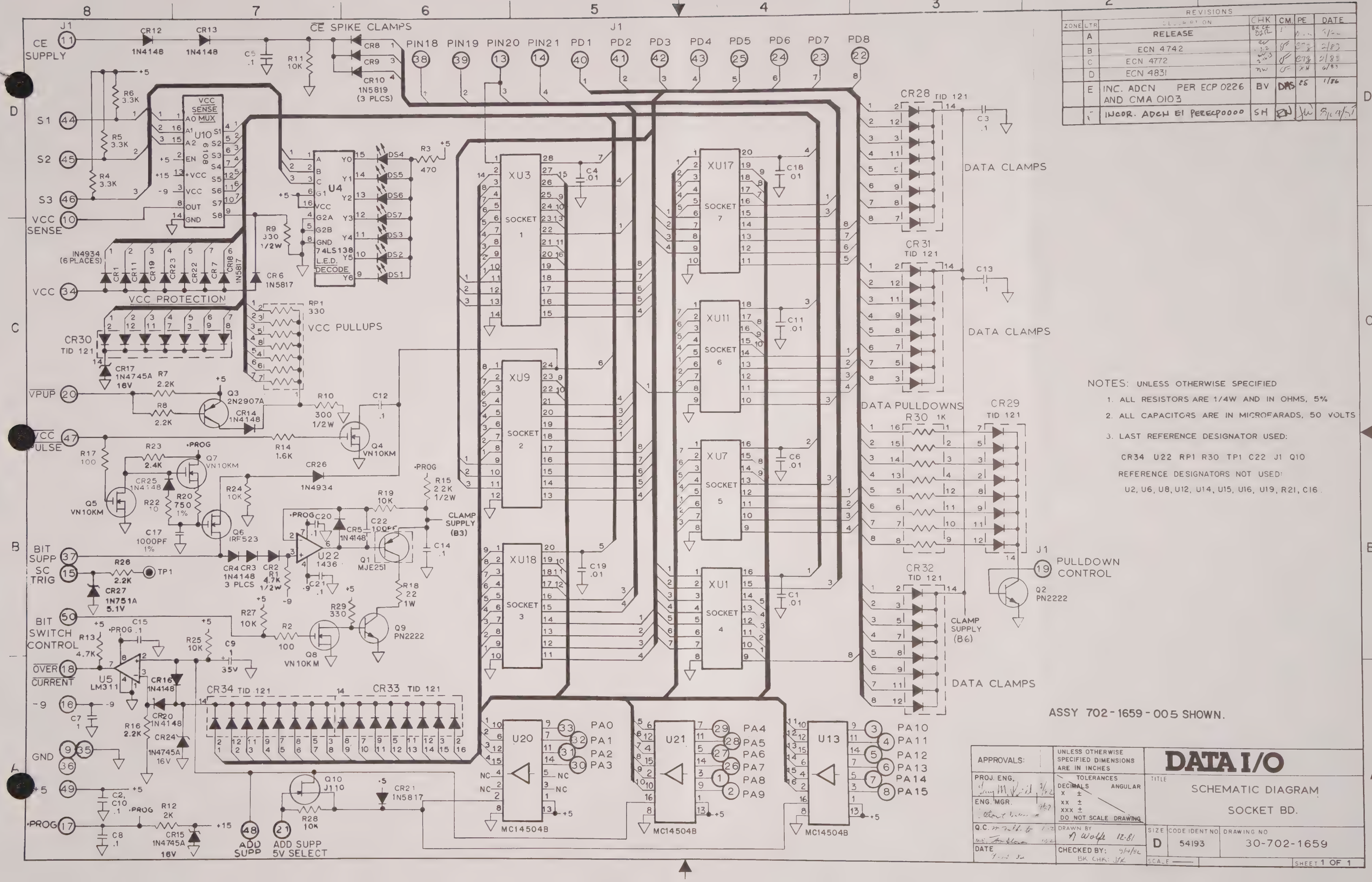
701-1655-002 SHOWN
-003 AS NOTED

APPROVALS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
DSN. ENGR. Gary M. Reilly	DATE 4/1/82	TOLERANCES, UNLESS OTHERWISE SPECIFIED XX ± XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM, ADDRESS CARD	
MFG ENGR	DATE			
QUAL ASSUR	DATE	DRAWN BY Barry V.	DATE Oct 22 81	SIZE D
ENGR MGR Victor E. Bell	DATE 4/1/82	CHECKED BY	DATE 4/1/82	CODE IDENT NO 54193
				DRAWING NO 30-701-1655
				SCALE NONE
				SHEET 1 OF 2

PAGE 1/PAGE 0



REVISIONS
LTR DESCRIPTION DR CHK APPR'D DATE
D SEE SHEET ONE
DATA COMPARATORS
DATA SWITCHES
VREF (2.A7)
LATCHED DATA (1.B2)
DATA SINK REGISTER
U24 DP8310
U23 74C374
U22 74LS05
DATA SWITCH RANGE SELECT (1.C4)
BIT SWITCH (1.B2)
J1
12 BIT SWITCH
40 PD1
41 PD2
42 PD3
43 PD4
25 PD5
24 PD6
23 PD7
22 PD8
GATED DATA (1.B2)
ENABLES (1.C2)
LM339 (8 PLACES)
MPQ3799 (2 PLACES)
MPQ3725 (2 PLACES)
220PF (8 PLACES)
MJE251 (8 PLACES)
U17 AD7524
U16 AD7524
VREF DAC
LOAD AMP
LOAD SUPPLY
LOAD SUPPLY DAC
HIGH RANGE LOADS
LOW RANGE LOADS
LOAD CLAMPS
U28 DP8310
LATCHED ADDRESS (1D2)
HI-LO RANGE SWITCH
LOAD RANGE SWITCH (1.C4)
VCC PULSE (1.B8)
VCC PULSE
CLAMP SWITCH (1.D4)
74LS05
7407
VR1 TL431
Q1 2N2484
Q2 MJE240
Q3 2N2907A
Q13 VN10KM
CR13 TID 121
CR6 1N4148
CR7 1N4148
CR8 1N4733A 5.1V
CR9 TID 139
CR4 TID139
CR5 5.1V 1N4733A
CR12 1N4740A 10V
Q10 2N2222
R29 4.99K 1% 1/2W
R28 14.3K 1%
R31 6.65K 1%
R22 34.8K 1%
R30 10K
R13 1K
R10 470
R12 4.7K
R11 4.7K
R18 2K
R17 10K
R27 3.3K
R20 3.3K
R19 10K
R9 2.2K 1/2W
R8 5K 20T
RAW +18 (1.A8)
C14, 470 PF
C2 .1/50V
TP2
TP3
TP4
APPROVALS:
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE SPECIFIED: .XX ± .XXX ± ANGULAR
DSN. ENGR. DATE
MFG. ENGR. DATE
QUAL. ASSUR. DATE
ENGR MGR. DATE
DRAWN BY B.V. G RYDER DATE 10-22 1981
CHECKED BY DATE
DATA I/O
TITLE SCHEMATIC DIAGRAM, ADDRESS CARD
SIZE D
CODE IDENT. NO 54193
DRAWING NO 30-701-1655
SCALE NONE
SHEET 2 OF 2



REVISIONS						
ZONE	LTR	DESCRIPTION	CHK	CM.	PE	DATE
	A	RELEASE				
	B	ECN 4742				2/83
	C	ECN 4772				2/83
	D	ECN 4831				6/83
	E	INC. ADCN PER ECP 0226 AND CMA 0103	BV	DAS		1/86
	F	INCOR. ADCN E1 PERECP0000	SH			

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%
2. ALL CAPACITORS ARE IN MICROFARADS, 50 VOLTS
3. LAST REFERENCE DESIGNATOR USED:

CR34 U22 RP1 R30 TP1 C22 J1 Q10

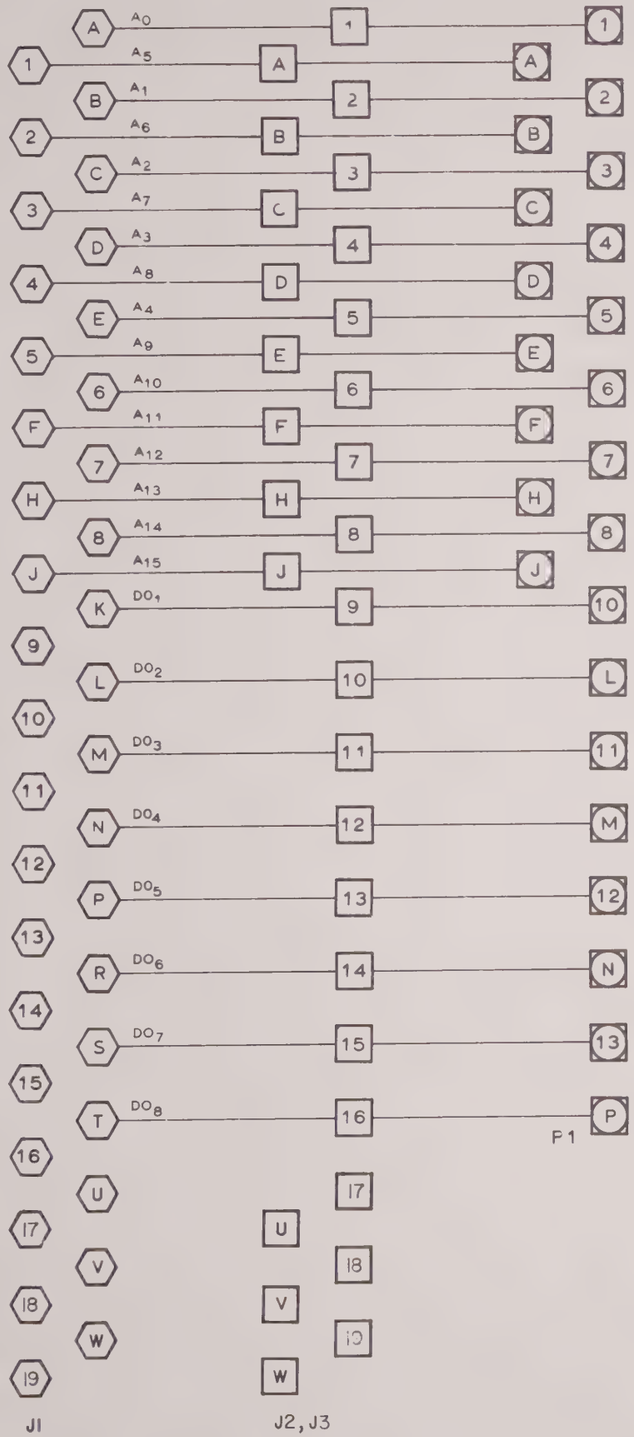
REFERENCE DESIGNATORS NOT USED:

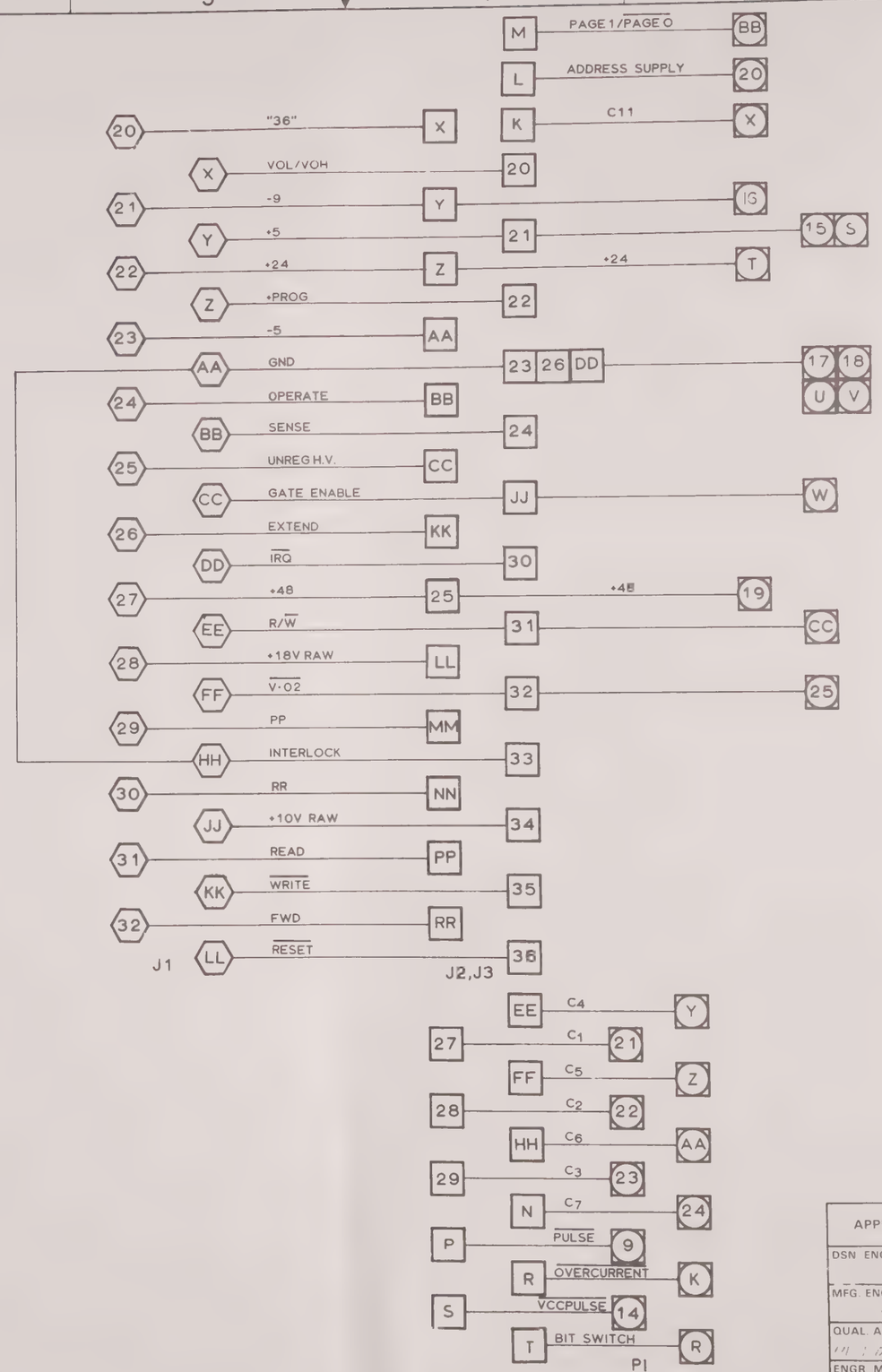
U2, U6, U8, U12, U14, U15, U16, U19, R21, C16.

ASSY 702-1659-005 SHOWN.

APPROVALS:	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O
PROJ. ENG.	TOLERANCES DECIMALS ANGULAR X ± XX ± XXX ± DO NOT SCALE DRAWING	TITLE SCHEMATIC DIAGRAM SOCKET BD.
ENG. MGR.		
Q.C.	DRAWN BY N. Wolfe 12-81	SIZE D · CODE IDENT NO 54193 · DRAWING NO 30-702-1659
DATE	CHECKED BY: BK CHK:	SCALE — · SHEET 1 OF 1

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	R.B.			





APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		DATA I/O	
DSN ENGR	DATE	TOLERANCES, UNLESS OTHERWISE SPECIFIED XX ± XXX ± ANGULAR		TITLE SCHEMATIC DIAGRAM, MOTHERBOARD	
MFG. ENGR	DATE				
QUAL. ASSUR.	DATE	DRAWN BY R. BENN	DATE 12-21-81	SIZE D	CODE INDENT NO 54193
ENGR. MGR.	DATE	CHECKED BY	DATE	DRAWING NO 30-702-1661	
				SCALE —	SHEET 1 OF 1

REVISIONS						
ZONE	LTR	DESCRIPTION	LR		CM.	PE	DATE
	A	RELEASE					
	B	ECN #5040	SH				
	C	INC. ADCN BI, PER ECP 0026	NL				
	D	INC. ADCN PER ECP 0226 AND CMA 0103, & ECP 0094	BV				1/86
	E	INC ADCN DI, PER ECP 0421					6/87

VCC SUPPLY

$\overline{CE}$ SUPPLY

BIT SUPPLY

CURRENT SENSE INTEGRATOR

BIT SUPPLY SWITCH

-5V SUPPLY OVERCURRENT (2,B8)

VCC (2,D8)

VCC SENSE (2,D8)

BIT SUPPLY (2,D8)

CE SUPPLY (2,D8)

BIT SWITCH (2.C8)

BIT SWITCH .6 (2.A8)

SWITCH CONTROL BUS

CURRENT SOURCE REFERENCE (2,C8)

CURRENT SOURCE KILL (2,C8)

ADDRESS SUPPLY (2,B3)

NOTES: UNLESS OTHERWISE SPECIFIED

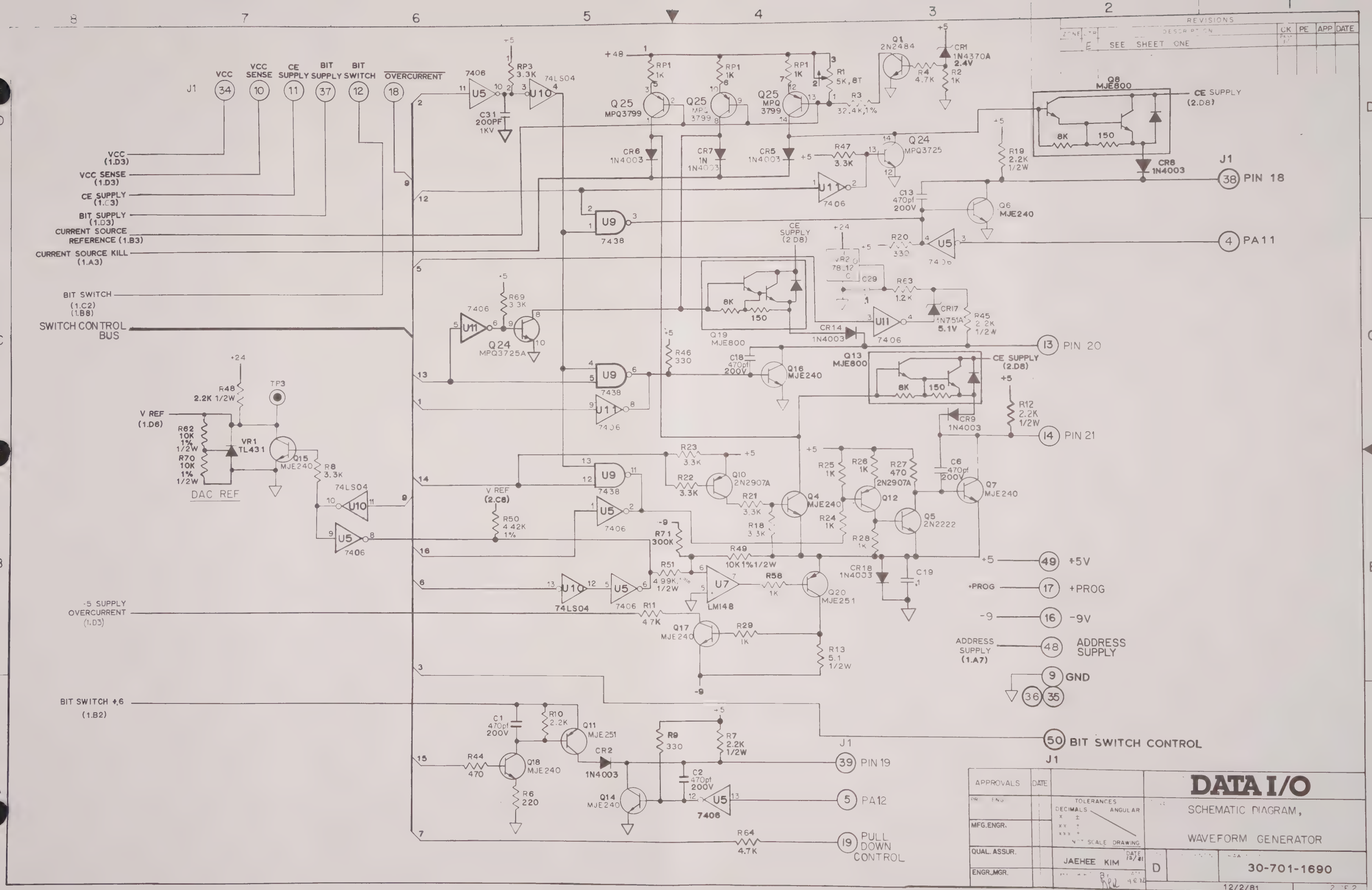
1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V, 10%.
3. LAST REFERENCE DESIGNATOR USED: R71, C40, RP3, Q25, U20, CR20, TP4, VR2
4.

IC. NO.	+5V	GND
U17-19	16	8
U16,20	20	10
U5,9-11	14	7

5. ALL DIODES ARE IN4148 UNLESS OTHERWISE SPECIFIED.

P/N 701-1690-0C5

APPROVALS:	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
PROJ ENG.	TOLERANCES DECIMALS X ± .XX ± .XXX ± ANGULAR ± DO NOT SCALE DRAWING	TITLE SCHEMATIC DIAGRAM, WAVEFORM GENERATOR	
ENG. MGR.	DRAWN BY 12-81 JAEHEE KIM	SIZE D	CODE IDENT NO 54193
Q.C.	CHECKED BY:	DRAWING NO 30-701-1690	
DATE		SCALE —	12/2/81 SHEET 1OF 2



REVISIONS
SEE SHEET ONE
J1
VCC
VCC SENSE
CE SUPPLY
BIT SUPPLY
BIT SWITCH
OVERCURRENT
VCC (1.D3)
VCC SENSE (1.D3)
CE SUPPLY (1.C3)
BIT SUPPLY (1.D3)
CURRENT SOURCE REFERENCE (1.B3)
CURRENT SOURCE KILL (1.A3)
BIT SWITCH (1.C2) (1.B8)
SWITCH CONTROL BUS
V REF (1.D6)
DAC REF
-5 SUPPLY OVERCURRENT (1.D3)
BIT SWITCH +.6 (1.B2)
CE SUPPLY (2.D8)
V REF (2.C8)
PIN 18
PA11
PIN 20
PIN 21
+5V
+PROG
-9V
ADDRESS SUPPLY (1.A7)
ADDRESS SUPPLY
GND
BIT SWITCH CONTROL
PIN 19
PA12
PULL DOWN CONTROL
Q25 MPQ3799
Q24 MPQ3725
Q24 MPQ3725A
Q19 MJE800
Q13 MJE800
Q8 MJE800
Q6 MJE240
Q16 MJE240
Q10 2N2907A
Q4 MJE240
Q12 2N2907A
Q5 2N2222
Q7 MJE240
Q20 MJE251
Q17 MJE240
Q11 MJE251
Q18 MJE240
Q14 MJE240
Q15 MJE240
Q1 2N2484
VR1 TL431
VR2 78L12
CR1 1N4370A 2.4V
CR17 1N751A 5.1V
CR8 1N4003
CR9 1N4003
CR18 1N4003
CR14 1N4003
CR2 1N4003
CR6 1N4003
CR7 1N 1N4003
CR5 1N4003
CR2 1N4003
TP3
DATA I/O
SCHEMATIC DIAGRAM,
WAVEFORM GENERATOR
APPROVALS
DATE
MFG.ENGR.
QUAL. ASSUR.
ENGR.MGR.
TOLERANCES
DECIMALS
ANGULAR
NOT SCALE DRAWING
JAEHEE KIM
D
30-701-1690
12/2/81

SOCKET ADAPTER

351A-067

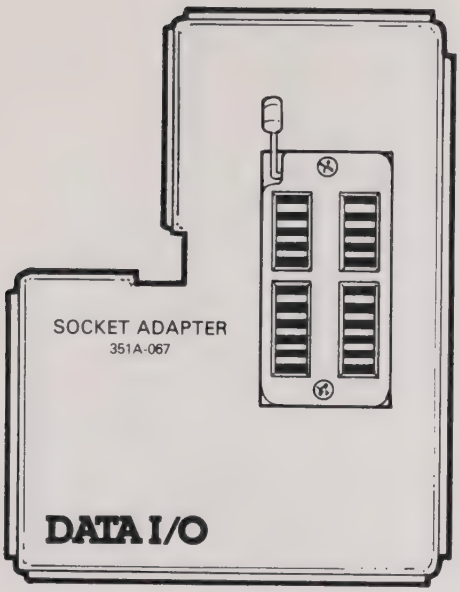


Figure 1. Socket Adapter 351A-067

The 351A-067 Socket Adapter enhances the UniPak™'s capabilities by enabling it to program the devices that could not otherwise be programmed on the UniPak™. When you choose the appropriate family and pinout, the Socket Adapter reroutes signals coming from the 24-pin socket on the UniPak™ to the 22-pin socket on the adapter. Refer to the UniPak™ manual or the Data I/O *Comparison Chart of Programmable Devices* to match devices to Socket Adapter part numbers and UniPak™ revision levels.

CAUTION

Do not turn the programmer on or off while a device is installed in the socket adapter — voltage transients may cause spurious programming. Do not change devices when a programming operation is occurring.

This socket adapter is used in the 24-pin socket of the UniPak™ and Unipak 2™. When the socket adapter is inserted, the 24-pin socket must be closed to hold it in place and to make good electrical contact.

STORAGE AND MAINTENANCE

Store the Socket Adapter in a location free of dust, excessive moisture, and extremes of temperature and humidity. Be careful to protect the top and bottom connectors from physical damage. Periodically inspect each socket contact for accumulated dirt and debris. Also inspect each contact for smooth opening and closing. Dirt and debris can usually be removed with compressed air.

The socket itself is constructed of polysulfone material and should be cleaned only with methyl alcohol, Freon TE™, or detergent and water. Do not lubricate.

Socket failure may be caused by mechanical damage to the socket. If the damage restricts positive opening and closing, replace the unit.

CIRCUIT DESCRIPTION

Figure 2 is a schematic representation of the socket adapter electronics. Device pinout is shown at the right (XU1). Socket pins, which mate with the programming receptacle, are on the left. Looking at the top of the socket adapter, shown at left, device pin 1 is on the upper left. Looking at the bottom of the socket adapter, connector pin one is in the upper right.

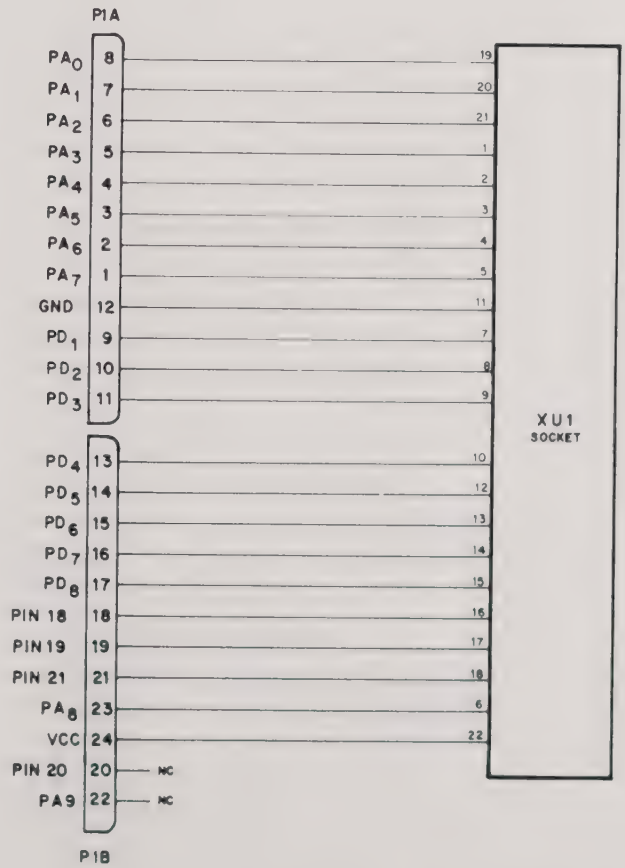


Figure 2. Schematic Diagram, Socket Adapter 351A-067

UniPak™ is a trademark of Data I/O Corporation.

10-715-1631
REV B MAR 84

SOCKET ADAPTER

351A-068

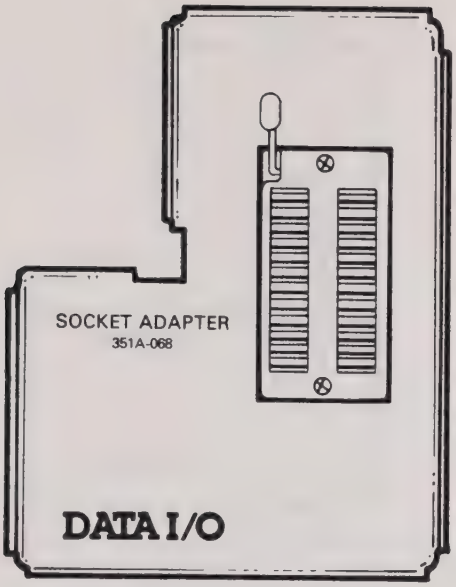


Figure 1. Socket Adapter 351A-068

The 351A-068 Socket Adapter enhances the UniPak™'s capabilities by enabling it to program the devices that could not otherwise be programmed on the UniPak™. When you choose the appropriate family and pinout, the Socket Adapter reroutes signals coming from the 24-pin socket on the UniPak™ to the 24-pin socket on the adapter. Refer to the UniPak™ manual or the Data I/O *Comparison Chart of Programmable Devices* to match devices to Socket Adapter part numbers and UniPak™ revision levels.

CAUTION

Do not turn the programmer on or off while a device is installed in the socket adapter — voltage transients may cause spurious programming. Do not change devices when a programming operation is occurring.

This socket adapter is used in the 24-pin socket of the UniPak™ and Unipak 2™. When the socket adapter is inserted, the 24-pin socket must be closed to hold it in place and to make good electrical contact.

STORAGE AND MAINTENANCE

Store the Socket Adapter in a location free of dust, excessive moisture, and extremes of temperature and humidity. Be careful to protect the top and bottom connectors from physical damage. Periodically inspect each socket contact for accumulated dirt and debris. Also inspect each contact for smooth opening and closing. Dirt and debris can usually be removed with compressed air.

The socket itself is constructed of polysulfone material and should be cleaned only with methyl alcohol, Freon TE™, or detergent and water. Do not lubricate.

Socket failure may be caused by mechanical damage to the socket. If the damage restricts positive opening and closing, replace the unit.

CIRCUIT DESCRIPTION

Figure 2 is a schematic representation of the socket adapter electronics. Device pinout is shown at the right (XU1). Socket pins, which mate with the programming receptacle, are shown on the left. Looking at the top of the socket adapter, shown at left, device pin 1 is on the upper left. Looking at the bottom of the socket adapter, connector pin one is in the upper right.

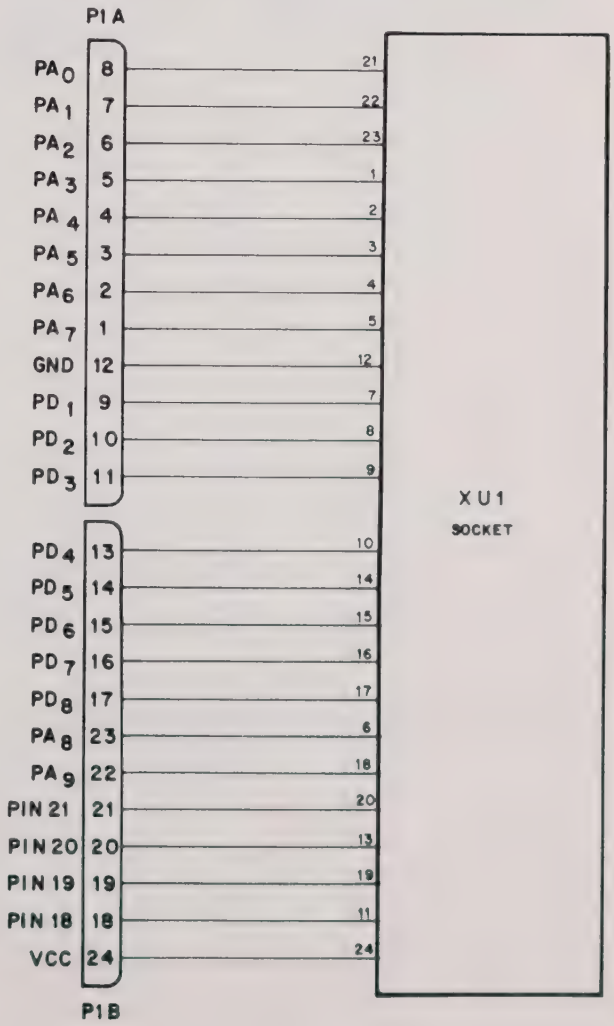


Figure 2. Schematic Diagram, Socket Adapter 351A-068

UniPak™ is a trademark of Data I/O Corporation.

10-715-1632
REV B MAR 84

SOCKET ADAPTER

351A-066

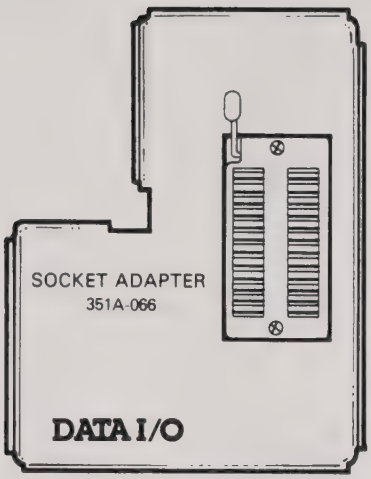


Figure 1. Socket Adapter 351A-066

The 351A-066 Socket Adapter enhances the UniPak™'s capabilities by enabling it to program the devices that could not otherwise be programmed on the UniPak™. When you choose the appropriate family and pinout, the Socket Adapter reroutes signals coming from the 24-pin socket on the UniPak™ to the 24-pin socket on the adapter. Refer to the UniPak™ manual or the Data I/O *Comparison Chart of Programmable Devices* to match devices to Socket Adapter part numbers and UniPak™ revision levels.

CAUTION

Do not turn the programmer on or off while a device is installed in the socket adapter—voltage transients may cause spurious programming. Do not change devices when a programming operation is occurring.

This socket adapter is used in the 24-pin socket of the UniPak™ and Unipak 2™. When the socket adapter is inserted, the 24-pin socket must be closed to hold it in place and to make good electrical contact.

STORAGE AND MAINTENANCE

Store the Socket Adapter in a location free of dust, excessive moisture, and extremes of temperature and humidity. Be careful to protect the top and bottom connectors from physical damage. Periodically inspect each socket contact for accumulated dirt and debris. Also inspect each contact for smooth opening and closing. Dirt and debris can usually be removed with compressed air.

The socket itself is constructed of polysulfone material and should be cleaned only with methyl alcohol, Freon TE™, or detergent and water. Do not lubricate.

Socket failure may be caused by mechanical damage to the socket. If the damage restricts positive opening and closing action, replace the unit.

CIRCUIT DESCRIPTION

Figure 2 is a schematic representation of the socket adapter electronics. Device pinout is shown at the right. Socket pins, which mate with the UniPak™ 24-pin socket, are shown to the left. Looking at the top of the socket adapter, device pin 1 is on the upper left. Looking at the bottom of the socket adapter, connector pin one is in the upper right.

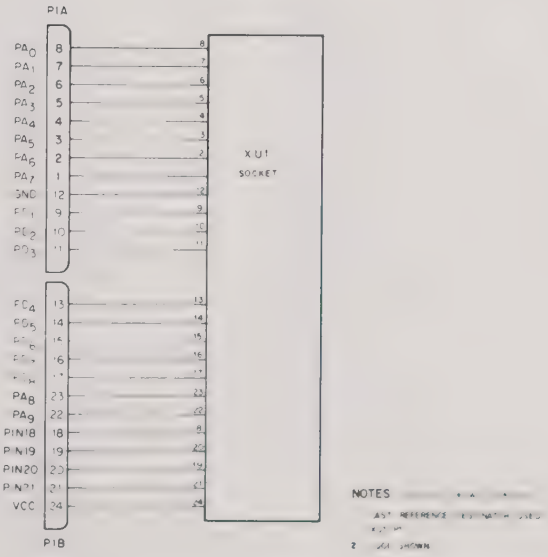


Figure 2. Schematic Diagram, Socket Adapter 351A-066

UniPak™ is a trademark of Data I/O Corporation.
10-715-1773
REV B MAR 84

U.S. Sales Offices and Representatives
Direct Sales and Service Offices

Data I/O Corporation
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
Telex Dom. 15-2167,
Int'l. 4740166 DIO UI

NORTHWEST REGION

Data I/O Corporation
1700 Wyatt Drive
Suite 1
Santa Clara, CA 95054
(408) 727-0641

SOUTHWEST REGION

Data I/O Corporation
2770 South Harbor Blvd.
Suite K
Santa Ana, CA 92704
(714) 662-1182 *(Sales)*
(714) 662-2498 *(Service)*
Telex 755870

EASTERN REGION

Data I/O Corporation
Nashua Road
Route 101A
Amherst, NH 03031
(603) 889-8511 *(Sales)*
(603) 889-8513 *(Service)*
Telex 943431

CENTRAL REGION

Data I/O Corporation
1810 N. Glenville Drive
Suite 108
Richardson, TX 75081
(214) 235-0044
Telex 792474

Representatives

ALASKA, WASHINGTON (TRI-CITIES, VANCOUVER), OREGON

Northwest Test and Measurement
8196 Southwest Hall
Suite 217
Beaverton, OR 97005
(503) 646-9966
1-800-247-5700
Telex 910-467-8775

WESTERN WASHINGTON, SPOKANE

Northwest Test and Measurement
4020 148th Ave. N.E.
Suite F
Redmond, WA 98052
(206) 881-8857

ARKANSAS, LOUISIANA, OKLAHOMA, TEXAS

TESTECH, Inc.
1000 E. Campbell Road
Suite 108
Richardson, TX 75081
(214) 644-5010

4800 West 34th St.
Suite D-6
Houston, TX 77092
(713) 956-0837

1715 Capital of Texas Hwy S.
Suite 107
Austin, TX 78746
(512) 327-7033

OHIO

Electro Sales Associates
1635 Mardon Drive
Dayton, OH 45432
(513) 426-5551

26250 Euclid Avenue
Suite 331
Cleveland, OH 44132
(216) 261-5440

MICHIGAN

Electro Sales Associates
29200 Vassar Road
Suite 505
Livonia, MI 48152
(313) 474-7320

9816 Portage Road
Portage, MI 49002
(616) 323-2416

PENNSYLVANIA, WEST VIRGINIA, EASTERN KENTUCKY

Electro Sales Associates
3740 Mount Royal Blvd.
Allison Park, PA 15101
(412) 487-3801

UPSTATE NEW YORK

DB Associates, Inc.
7000 E. Genesee Street
Building D
Fayetteville, NY 13066
(315) 446-0220

KANSAS, NEBRASKA

Midtec Associates, Inc.
7702 Mize Road
DeSoto, KS 66018
(913) 441-6565
Telex 910-743-4129

MISSOURI

Midtec Associates, Inc.
8460 Lindbergh North
Suite 11
Florissant, MO 63031
(314) 837-5200

FLORIDA

Pen Tech Associates
201 S.E. 15th Terrace
Suite K
Deerfield Beach, FL 33441
(305) 421-4989

1398 Semoran Blvd.
Suite 106
Casselberry, FL 32707
(305) 645-3444

GEORGIA, TENNESSEE

Pen Tech Associates
627 Cherokee Street
Suite 21
Marietta, GA 30060
(404) 424-1931

NORTHERN FLORIDA, ALABAMA, TENNESSEE, MISSISSIPPI

Pen Tech Associates
3322 Memorial Pkwy. S.W.
Suite 36
Huntsville, AL 35801
(205) 881-9298

NORTH CAROLINA, SOUTH CAROLINA

Pen Tech Associates
3709 Alliance Drive
Suite C
Greensboro, NC 27407
(919) 852-6000

MINNESOTA, NORTH DAKOTA, SOUTH DAKOTA

Torkelson Associates
4940 Viking Drive
Minneapolis, MN 55435
(612) 835-2414
Telex 910-576-2740

NORTHERN ILLINOIS, IOWA, INDIANA

Torkelson Associates
108 Wilmot Road, Suite 110
Deerfield, IL 60015
(312) 945-8700
Telex 910-992-1438

INDIANA, WESTERN KENTUCKY

Torkelson Associates
2346 S. Lynhurst
Room B101
Indianapolis, IN 46241
(317) 244-7867
Telex 810-341-3141

WISCONSIN

Torkelson Associates
2840 N. Brookfield Road
Brookfield, WI 53005
(414) 784-7736

ARIZONA, NEVADA

Zeus Electronics, Inc.
1428 E. Pierson Street
Phoenix, AZ 85014
(602) 263-6022
1-800-528-4512
Telex 910-951-1362

NEW MEXICO, EL PASO CO., TEXAS

Zeus Electronics, Inc.
8100 Mountain Road N.E.
Suite 111
Albuquerque, NM 87110
(505) 842-6633
1-800-528-4512

COLORADO, WYOMING

Zeus Electronics, Inc.
3333 Quebec Street
Suite 2950
Denver, CO 80207
(303) 321-4246
1-800-528-4512

UTAH, IDAHO, MONTANA

Zeus Electronics, Inc.
1849 W. North Temple
Suite B105
Salt Lake City, UT 84116
(801) 534-0500
(801) 534-0503

VIRGINIA, WASHINGTON D.C.

SCI-REP, Inc.
9512A Lee Highway
Fairfax, VA 22031
(703) 385-0600
Telex 710-833-0361

NEW JERSEY, EASTERN PENNSYLVANIA

SCI-REP, Inc.
304 Cooper Center
Pennsauken, NJ 08109
(609) 662-5222
Telex 710-892-1297 SCI-REP PESN

Addresses on this list subject to change without notice.

0321 784

International Sales Offices and Representatives

Europe

Data I/O Europe
Vondelstraat 50-52
NL-1054 GE Amsterdam
The Netherlands
(20)186855
Telex 16616 DATIO NL

Data I/O Germany GmbH
Bahnhofstrasse 3
D-6453 Seligenstadt
West Germany
(6182)3088 89
Telex 4184962 DATA D

AUSTRIA

Ing. Ernst Steiner
Hummelgasse 14
A-1130 Wien
Austria
(222)827474
Telex 135026 ES A

BELGIUM

Simac Electronics
Rue du Progres 52
BOITE 3
B-1000 Brussels
Belgium
(2)2192451-3
Telex 23662 SIMEIP B

DENMARK

ITT Multikomponent A/S
Naverland 29
DK-2600 Glostrup
Denmark
(2)451822 or (2)456645
Telex 33355 ITT DK

FINLAND

Instrumentarium Elektroniikka
PL 64 (Vitikka 1)
SF-02630 ESPOO 63
Finland
(358)0905281
Telex 124426 HAVUL SF

FRANCE

M.B. Electronique
606, rue Fourny
Zac de Buc
P.O. Box 31
F-78530, Buc, France
(3)9568131
Telex MB 695414 F

GERMANY

Instrumatic Electronics GmbH
Am Kirchenholzel 14
D-8032 Grafelfing (near Munich)
West Germany
(89)852063
Telex 524298 INSTR D

GREECE

Eltronics Ltd.
2, Alopekis Str. 52
GR-106 75 Athens 139
(1) 7249511, -15
Telex 216589 DARX GR

ISRAEL

TELSYS, Ltd.
12, Kehilat Venetsia Street
Tel-Aviv 69010
Israel
(3)494891-5/(3)494881-2
Telex 32392 TSEE IL

ITALY

Sistrel SPA
Via Giuseppe Armellini 39
I-00143 Roma
Italy
(6)5915551
Telex 680356 SISTREL I

Sistrel SPA
Via P. da Volpedo 59
I-20092 Cinisello Balsamo (Mi)
Italy
(2)6120129 or 6181893
Telex 334643 SISTREL I

NETHERLANDS

Simac Electronics
Veenstraat 20
NL-5503HR Veldhoven
The Netherlands
(40)533725
Telex 51037 SIMAC NL

NORWAY

Teleinstrument A/S
P.O. Box 134
N-1371 Asker
Norway
(2)789460
Telex 72919 TELIN N

PORTUGAL

Decada
Equipamentos de Electronica
e Cientificos, Sarl
Av. Bombeiros Voluntarios, Lote 102b
Miraflores/Alges
1495 Lisboa
Portugal
2103420
Telex 15515 ESPC P

SPAIN

Instrumatic Espanola
Alameda Principal 26
Apartado 151
Malaga 5
Spain
(52)213199/213898
Telex 77131 HAFN E

Instrumatic
Juan Hurtado de Mendoza 9
Madrid-16
Spain
(1)2502577 2507278
Telex 46277 ITIC E

SWEDEN

Macrotek AB
Vallingbyvagen 212, Box 43
S-162 11 Vallingby, Sweden
(8)870190
Telex 12543 MATEK S

SWITZERLAND

Instrumatic SA
5-7, rue du Clos
CH-1207 Geneve
Switzerland
(22)360830
Telex 28667 INSR CH

Instrumatic AG
Weingartenstrasse 9
CH-8803 Ruschlikon
Switzerland
(1)7241410
Telex 56605 INST CH

TURKEY

Data I/O Europe
Vondelstraat 50-52
NL-1054 GE Amsterdam
The Netherlands
(20)186855
Telex 16616 DATIO NL

UNITED KINGDOM

Microsystem Services
P.O. Box 37
Lincoln Road
Cressex Industrial Estate
High Wycombe
Bucks, HP12 3XJ, England
(494)41661
Telex 837187 MICSYS G

International

Data I/O International
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9746
U.S.A.
(206) 881-6444
Telex Dom. 15-2167, Int'l. 4740166 DIO UI

AUSTRALIA

ADELAIDE, AUSTRALIA

Warburton Franki (Adelaide) Pty. Ltd.
322 Grange Road
Kidman Park
South Australia 5025 Australia
3567333
Telex Warfran AA82579

BRISBANE, QUEENSLAND

Warburton Franki (Brisbane) Pty. Ltd.
13 Chester Street
Fortitude Valley
Queensland 4006 Australia
527255
Telex Warfran AA41052

MELBOURNE, VICTORIA

Warburton Franki (Melbourne) Pty. Ltd.
220 Park Street
South Melbourne
Victoria 3205 Australia
699 4999
Telex Warfran AA31370

PERTH, WESTERN AUSTRALIA

Warburton Franki (Perth)
98-102 Belgravia Street
Belmont, 6104
Western Australia
65 7000
Telex Warfran AA92908

SYDNEY, NEW SOUTH WALES

Warburton Franki (Sydney)
1-5 Carter St.
Lidcombe N.S.W.
P.O. Box 394
Australia 2141
648 1711
Telex AA22265

CORPORATE OFFICE

Warburton Franki (Corporate Office)
9 Birnie Ave., P.O. Box 117
Lidcombe, N.S.W. Australia 2141
647-2266
Telex Warfran AA21299

BRAZIL

Cosele
Instrumentos Electronicos Ltda.
Rue da Consolacao, 867
3.° And. - Conj. 32
01301 - Sao Paulo - SP
Brazil
255-1733 or 256-7421 or 231-5548
Telex (011) 30869 CSEL-BR
(011) 38044 CSEL-BR

Cosele
Instrumentos Electronicos Ltda
Rua Sacadura Cabral, 120
Sala 205 - Saude - 20081
Rio De Janeiro - RJ
(021) 283-2036
Telex (021) 33019

CANADA

Allan Crawford Associates, Ltd.
6503 Northam Drive
Mississauga, Ontario L4V 1J2
(416) 678-1500
Telex 06 968769

881 Lady Ellen Place
Ottawa, Ontario K1Z 5L3
(613) 722-7682
Telex 053 3600

7018 Cote De Liesse
St. Laurent, P.Q. H4T 1E7
(514) 731-8564
Telex 05-824944

1935-30th Avenue N.E.
Calgary, Alberta T2E 6Z5
(403) 230-1341
Telex 03 821186

3795 William Street
Burnaby, B.C. V5C 3H3
(604) 294-1326
Telex 04 54247

192 Joseph Zatzman Drive
Dartmouth, Nova Scotia B3B 1N4
(902) 463-9360
Telex 019 31604

15043A 118th Avenue
Edmonton, Alberta T5V 1H9
(403) 451-4893

CHINA

Dorado Co.
P.O. Box 4155
Seattle, WA 98104
583-0000

International P.O. Box 9051
Beijing, China
Telex: 329473 (Burgess Sea)

HONG KONG

Eurotherm (Far East) Ltd.
49-51 Wong Chuk Hang Rd.
Flat A & B, 19/F
Derrick Industrial Bldg.
Aberdeen, Hong Kong
5-546391
Telex 72449 EFELD HX

INDIA

Transmarketing Private, Ltd.
Sterling Center
16/2 Dr. Annie Besant Rd.
Bombay 400-18
India
022 4921874/022, 4920320
Telex 011-5424 TMTIN

59, Millers Road
Benson Town
Bangalore
India 560-046

JAPAN

Data I/O Japan Company, Ltd.
Ginza Orient Building, 6F.
8-9-13, Ginza, Chuo-ku
Tokyo 104 Japan
(03) 574-0211
Telex 2522685 DATAIO J

S. KOREA

Elcom System, Inc.
Jinduk Bld. Room 302
55-15 Nonhyun-Dong
Kangnam Ku
Seoul, Korea
555 5222 or 557-3836
Telex ADUCEL K25227

MALAYSIA

GEA Technology PTE., Ltd.
Units 1003 to 1008, Block 3, 10th Floor
PSA Multi-Storey Complex
Pasir Panjang Road
Singapore 0511
2729412
Telex RS 37162 Answerback Geasin

MEXICO

Christensen, S.A.
Guillermo Prieto 76-304
Col. San Rafael
Delegacion Cuahutemoc
06470-Mexico, D.F.
546-25-95 546-29-55
Telex 017-75612 Mycome

NEW ZEALAND

Wellington-New Zealand:
Warburton Franki, Ltd.
42-43 Oxford Terrace
Lower Hutt, New Zealand
693-016
Telex Warfran NZ 3824

Warburton Franki, Ltd.
P.O. Box 9301; Newmarket
142 Broadway
Auckland, New Zealand
504-458
Telex Warfran NZ 3824

PHILIPPINES

Data I/O International
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
Telex Dom. 15-2167/Int'l. 4740166 DIO UI

SINGAPORE

GEA Technology PTE., Ltd.
Units 1003 to 1008, Block 3, 10th Floor
PSA Multi-Storey Complex
Pasir Panjang Road
Singapore 0511
2729412
Telex RS 37162 Answerback Geasin

SOUTH AFRICA

Electronic Building Elements (PTY) Ltd.
P.O. Box 4609
Pine Square, 18th Street
Hazelwood
Pretoria, South Africa
46-9221/7
Telex 3 0181 SA
Telegrams Elbilem

SOUTH & CENTRAL AMERICA

Data I/O International
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9746
U.S.A.
(206) 881-6444
Telex Dom. 15-2167, Int'l. 4740166 DIO UI

TAIWAN

Surtek International, Inc.
315 Fu Hsing N. Road
104, Taiwan R.O.C.
(2) 713-4022
Telex 23756 MULTIIC

THAILAND

Dynamic Supply Engineering R.O.P.
12 Soi Pasara 1, Sukhumvit 63
Bangkok-11, Thailand
Tel. - 3914434, 39228532
Telex 82455 DYNASUP TH

Addresses on this list subject to change without notice.

0321/784

SOCKET ADAPTER

351A-073

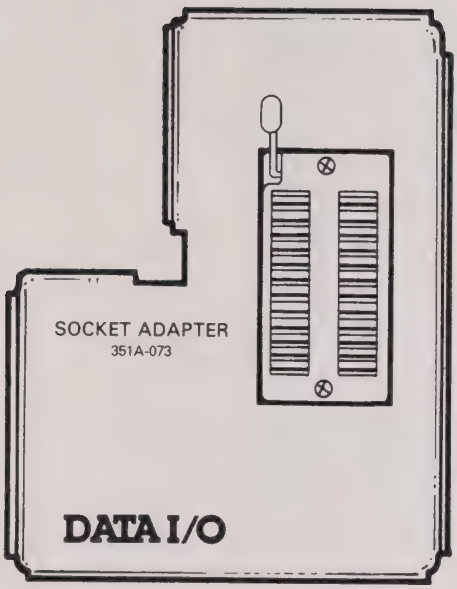


Figure 1. Socket Adapter 351A-073

The 351A-073 Socket Adapter enhances the UniPak™'s capabilities by enabling it to program the devices that could not otherwise be programmed on the UniPak™. When you choose the appropriate family and pinout, the Socket Adapter reroutes signals coming from the 28-pin socket on the UniPak™ to the 24-pin socket on the adapter. Refer to the UniPak™ manual or the Data I/O *Comparison Chart of Programmable Devices* to match devices to Socket Adapter part numbers and UniPak™ revision levels.

CAUTION

Do not turn the programmer on or off while a device is installed in the socket adapter — voltage transients may cause spurious programming. Do not change devices when a programming operation is occurring.

This socket adapter is used in the 28-pin socket of the UniPak™ and Unipak 2™. When the socket adapter is inserted, the 28-pin socket must be closed to hold it in place and to make good electrical contact.

STORAGE AND MAINTENANCE

Store the Socket Adapter in a location free of dust, excessive moisture, and extremes of temperature and humidity. Be careful to protect the top and bottom connectors from physical damage. Periodically inspect each socket contact for accumulated dirt and debris. Also inspect each contact for smooth opening and closing. Dirt and debris can usually be removed with compressed air.

The socket itself is constructed of polysulfone material and should be cleaned only with methyl alcohol, Freon TE™, or detergent and water. Do not lubricate.

Socket failure may be caused by mechanical damage to the socket. If the damage restricts positive opening and closing, replace the unit.

CIRCUIT DESCRIPTION

Figure 2 is a schematic representation of the socket adapter electronics. Device pinout is shown at the right (XU1). Socket pins, which mate with the programming receptacle, are on the left. Looking at the top of the socket adapter, shown at left, device pin 1 is on the upper left. Looking at the bottom of the socket adapter, connector pin one is in the upper right.

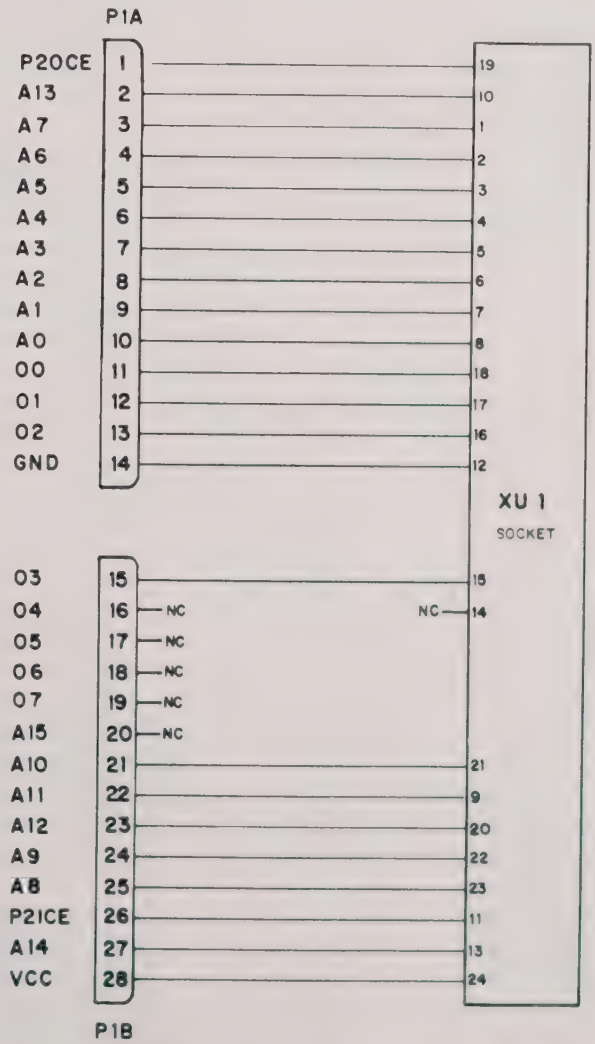


Figure 2. Schematic Diagram, Socket Adapter 351A-073

UniPak™ is a trademark of Data I/O Corporation.
10-715-1938
REV B MAR 84

Product Warranty

Data I/O warrants that product(s) sold pursuant to any resultant agreement shall be free from defects in material or workmanship at the time of delivery. Such warranty shall extend for one (1) year for hardware and ninety (90) days for software, unless specified otherwise, beginning from the date of shipment. Buyer must provide notice to Data I/O within this prescribed warranty period of any defect; if the defect is not the result of improper usage, service, maintenance or installation and equipment has not been otherwise damaged or modified after delivery, Data I/O shall either replace or repair the defective part or parts of equipment or replace the equipment or refund the purchase price at Data I/O's option after return of such equipment by buyer to Data I/O. Shipment to Data I/O's facility shall be borne on account of buyer, including all duties, fees, brokerage and special handling charges. Shipment from Data I/O's facility shall be borne by Data I/O.

(a) Consequential Damages — Data I/O shall not be liable for any incidental or consequential damages incurred as a result of any defect in any equipment sold hereunder and Data I/O's liability is specifically limited to its obligation described herein to repair or replace a defective part or parts covered by this warranty.

(b) Exclusive Warranty — The warranty set forth herein is the only warranty, oral or written made by Data I/O and is in lieu of and replaces all other warranties, expressed or implied, including the WARRANTY OF MERCHANTABILITY AND THE WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE.

090-0003-001

NO POSTAGE NECESSARY IF MAILED IN THE UNITED STATES

BUSINESS REPLY CARD

FIRST CLASS PERMIT NO. 41 REDMOND, WA 98052

POSTAGE WILL BE PAID BY ADDRESSEE

DATA I/O

Reader Comments
Technical Publications Supervisor
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9987

NO POSTAGE NECESSARY IF MAILED IN THE UNITED STATES

BUSINESS REPLY CARD

FIRST CLASS PERMIT NO. 41 REDMOND, WA 98052

POSTAGE WILL BE PAID BY ADDRESSEE

DATA I/O

Warranty/Registration
Technical Support Manager
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9987

Reader Comments

The manual's completeness, accuracy, organization, usability, and reliability: _____

_____

Did you find errors in this manual? _____

How can this manual be improved? _____

_____

_____

Additional comments: _____

_____

Name _____ Title _____

Department _____ M/S _____

Company _____

Address _____

City _____ State _____ Zip _____

Phone ( ) _____ Manual or Part No. _____

Warranty Registration / License Acknowledgment

Please sign and return this card to Data I/O within five days

Did the packaging of this equipment exhibit any outward signs of physical damage? . . . . . ☐ YES ☐ NO

Did this equipment arrive intact, without loose parts or cable damage? . . . . . ☐ YES ☐ NO

Did the equipment operate on power-up? . . . . . ☐ YES ☐ NO

Did you attain adequate system performance? . . . . . ☐ YES ☐ NO

Were any electrical adjustments required? . . . . . ☐ YES ☐ NO

If you required assistance, was a local Data I/O representative contacted? . . . . . ☐ YES ☐ NO

Comments: _____

Name _____ Title _____

Department _____ M/S _____

Company _____ Phone ( ) _____

Address _____

City _____ State _____ Zip _____

The undersigned hereby agrees to the terms and conditions of the software license agreement for the product listed below:

Model or Description _____ Serial or Part No. _____

Date Received _____ Signature _____

UNIPAK 2/2B™

Software Update Kit

985-0002-019 *November 1990*

Data I/O has made every attempt to ensure that the information in this document is accurate and complete. However, Data I/O assumes no liability for errors, or for any damages that result from use of this document or the equipment that it accompanies.

Data I/O reserves the right to make changes to this document without notice at any time.

ORDERING INFORMATION

When ordering this manual, use Part Number 985-0002-019.
Applies to: Engineering part numbers 953-0002-023 and up
and 953-0017-017 and up.

UniPak 2™ and UniPak 2B™ are trademarks of Data I/O Corporation.

Copyright Data I/O Corporation, 1989, 1990. All rights reserved.

INTRODUCTION

WARNING

The procedures described in this document are intended for use only by personnel qualified to service electronic equipment. Do not attempt to perform these procedures unless you are qualified to do so.

This manual provides the software update instructions necessary for updating either the UniPak 2 or the UniPak 2B. The parts included in each of the update kits are listed in Table 1 below:

Table 1. Software Update Kit Parts

Type of Kit	Description	Quantity	Data I/O Part No.	Installation Location
UniPak 2	EPROM	1	324-0059-053	U19
	EPROM	1	324-0059-054	U20
	Decode PAL	1	324-1760-013	U13
	Label	1	–	
	Documentation Notice	1	090-0332	
	UniPak 2 User Notes	1	984-0001	
UniPak 2B	EPROM	1	324-0059-053	U19
	EPROM	1	324-0059-054	U20
	Decode PAL	1	324-1760-013	U13
	Label	1	–	
	UniPak 2B Device List	1	984-0179	
	UniPak 2B Acceptance Test	1	984-0179	
	UniPak 2B User Notes	1	984-0179	

Firmware Version Number: VER 23.0

CAUTION

The software update kit EPROMs are static-sensitive. Observe standard handling precautions, such as performing the update kit procedures at an anti-static workstation or wearing a grounded wrist-strap, otherwise, damage to the EPROMs may result.

UNIPAK 2/2B SOFTWARE UPDATE KIT INSTALLATION

The following paragraphs describe how to install the software update kit. You will need the following tools for installation of the kit:

- One Phillips-head screwdriver (medium size, #1 or #2)
- One slot-head screwdriver (medium size)
- One pair of needle-nose pliers
- IC extractor tool, or small slot-head screwdriver
- Soldering Iron

For the Software Update Kit to work, your UniPak 2/2B must have a 701-2126 Memory Board. To determine if your pak has the correct memory board, perform the following steps:

1. Install the UniPak 2/2B in the programmer and turn the programmer on.
2. Press **SELECT**. Type **E F** on the programmer keyboard and then press **START**.

If the display does not show version 13.0 or greater, the new Memory Board must be installed. A hardware update kit (951-0045) is required.

NOTE

If you are installing only the Software Update Kit, go directly to the UniPak 2/2B Disassembly section on the following page.

If you are installing the Hardware Update Kit, go to UniPak 2/2B Disassembly section of the Hardware Update Kit manual. Complete the instructions and when instructed to do so, go to the Firmware Installation section in this manual.

If you are installing a UniPak 2 to 2B Conversion Kit and/or the Hardware Update Kit, begin installing the conversion kit first. When the conversion kit instructions direct you to install the software and/or hardware update kit:

1. a. *If you are installing a new memory board, go to step 6 of the Hardware Update Kit manual, complete the instructions and then go directly to the Firmware Installation section in this manual.*

   b. *If you are not installing a new memory board, go directly to the Firmware Installation section in this manual.*

2. *Complete the software update kit installation as directed in the Firmware Installation section of this manual.*
3. *Proceed to the Testing the UniPak 2B section of the conversion kit manual and*

   a. *If the conversion kit was installed, complete the conversion kit installation.*

   b. *If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete the installation there.*

UniPak 2/2B Disassembly

To disassemble the UniPak 2/2B for installation of the updated firmware, follow the procedures listed below.

1. Remove the UniPak 2/2B from the programmer, if it is installed.
2. Set the UniPak 2/2B face down on the flat surface of a static-free workstation.
3. Using the medium size slot-head screwdriver, unscrew the captive fasteners (Figure 1, Step 1) until they hang loosely; the fasteners will not separate from their standoffs.
4. Lift the card cage up slightly, then pull out (as shown in Figure 1, Step 2) to unlock the flanges.

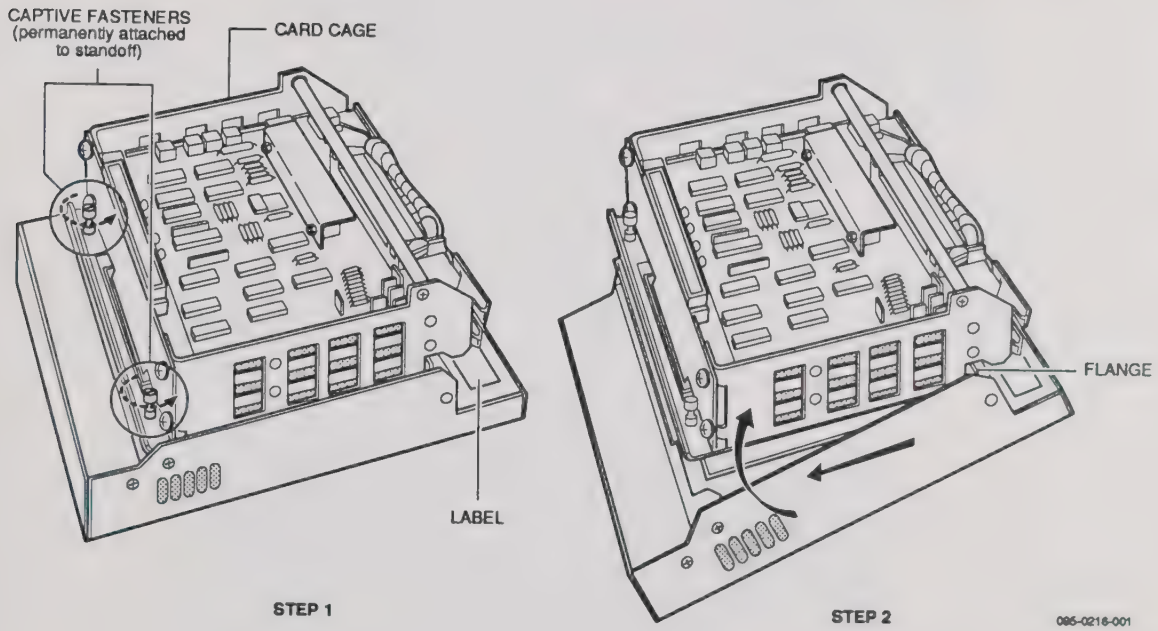


Figure 1. UniPak 2/2B Disassembly
(UniPak 2 shown)

5. Lift the card cage up and out of its top cover until you can see the socketboard interconnect cable (see Figure 2). Do not detach the socketboard interconnect cable.
6. Turn the card cage over and set it on the flat surface next to the top cover. This step exposes the armite or mylar shield which covers the memory board.

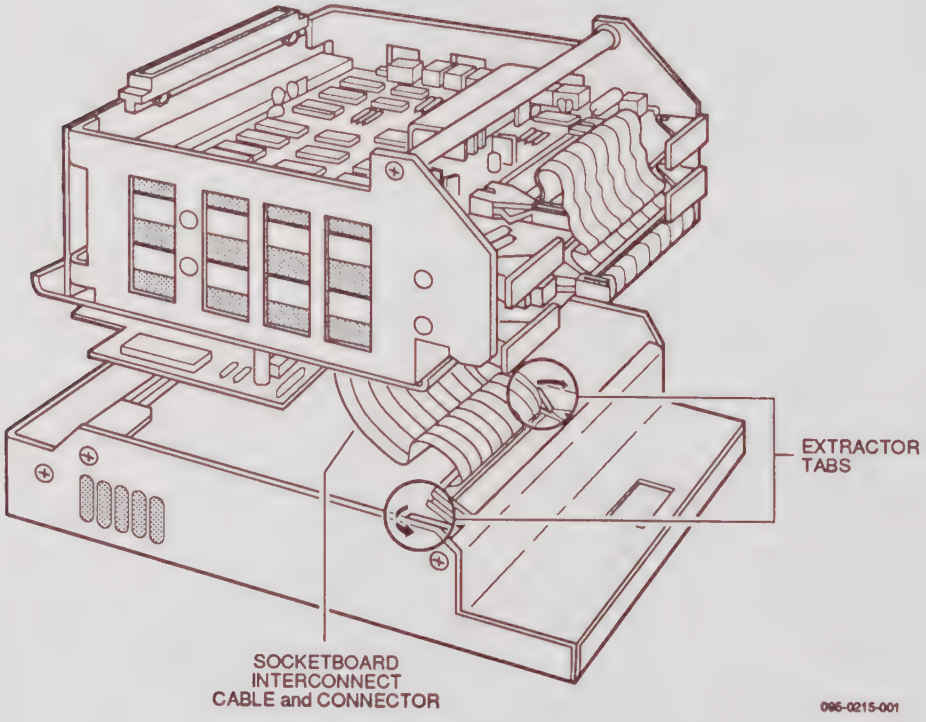


Figure 2. Socketboard Interconnect Cable

7. Remove the two Phillips-head screws and armite or mylar shield from the memory board (see Figure 3). Retain the washers and screws for reassembly. (If you are updating a UniPak 2B that was factory built, rather than a field conversion, it will not contain any washers.)
8. Pull the memory board straight up to unplug it from the card edge connector (as shown in Figure 3).

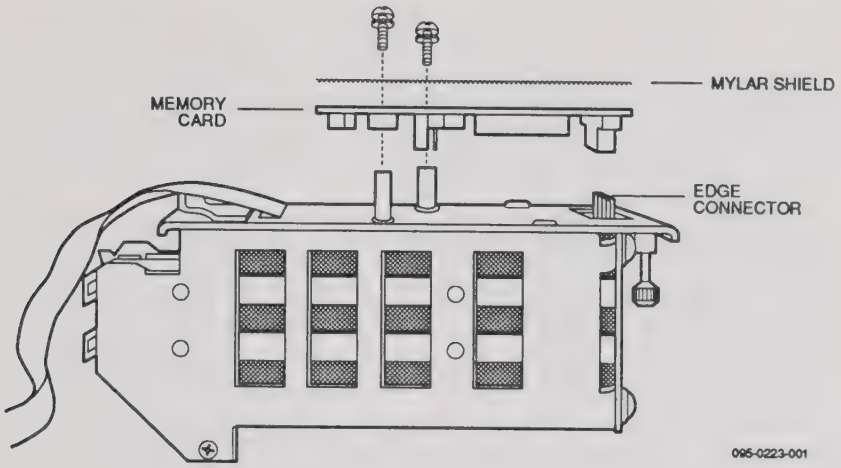


Figure 3. Memory Board Removal

9. Turn the 701-2126 memory board over so the component side faces up (Figure 4) in preparation for firmware installation.

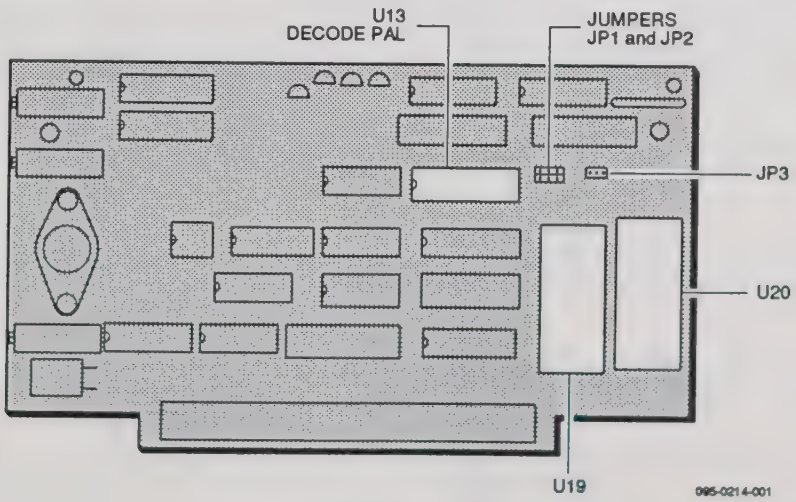


Figure 4. Update Component Location

Table 2. Jumper Configuration

Jumper	Position
JP1	Position B
JP2	Position B
JP3	Position B

Firmware Installation

The following steps describe how to install the firmware components of the update kit into your disassembled UniPak 2/2B. Follow the procedures in the order that they are presented here.

CAUTION

The software update kit EPROMs are static-sensitive. Perform the following procedures at a static-free work station to prevent static-related damage to the EPROMs.

1. Remove EPROMs U19, U20 and decode PAL U13 (see figure 4) from the memory board using an IC extractor tool or small slot-head screwdriver.
2. Refer to Table 2 for jumper configurations. If any jumpers are not in the correct locations, use the needle-nose pliers and soldering iron to change them to the correct location.

NOTE

Prior to installing the firmware, check the socket contacts to ensure that they are not damaged. If any socket contact is damaged, repair or replace that part before proceeding with the firmware installation.

3. Install the software update kit Decode PAL U13 in memory board socket U13. Refer to Table 1 for software update kit firmware part numbers and their corresponding installation locations.

WARNING

When installing EPROMs be sure to bottom justify them in the socket (Figure 5).

4. Install the software update kit EPROMs U19 and U20 in sockets U19 and U20, respectively. Refer to table 1 for software update kit component part numbers and their corresponding installation locations.

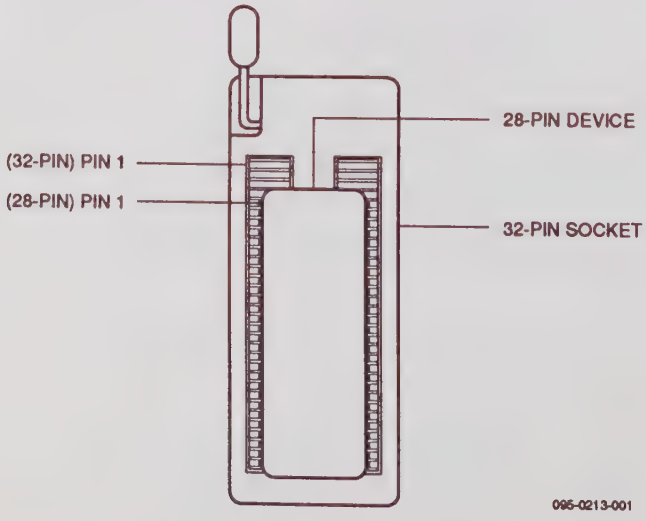


Figure 5. EPROM Installation Alignment

UniPak 2/2B Reassembly and Testing

Reassembly of the UniPak 2/2B is performed by reversing the disassembly procedures. Follow the steps listed below and refer to Figures 1 through 3 on the previous pages.

1. Plug the memory board into its card cage edge connector (figure 3) until it is firmly seated.
2. Replace the armite or mylar shield, washers (if included) and two Phillips-head screws.
3. Reinsert the card cage into the top cover with the memory board facing into the top cover (Figure 2). Tilt the card cage up and push gently forward to lock the top cover's flange between the card cage's top and bottom flanges (Figure 1, Step 2). Then gently set the card cage back into the top cover.
4. Using the medium size slot-head screwdriver, tighten the captive fastener slot screws finger tight.
5. Perform a self-test on the UniPak 2/2B by installing it in a programmer and applying power.

   If the programmer fails to power up correctly, or the self-test message is not displayed, check to make sure that all of the software update kit installation procedures (and conversion kit installation procedures, if you are installing the conversion kit) were performed correctly. If the self-test fails again, contact your local Data I/O Service Center for assistance.
6. Verify the correct firmware configuration/version number by pressing **SELECT E F START** on the programmer's keyboard. Check the programmer display for the four-character configuration number and the version number. See the bottom of Table 1 on the first page of this document for the correct configuration and version numbers.

   If the correct configuration and version numbers are not displayed, the firmware has not been installed correctly. Check to make sure that all installation procedures were performed correctly. Make sure that all PROMs are fully inserted into their sockets and are making proper contact at their connections. Install the UniPak 2/2B in a programmer and again press **SELECT E F START**. If the configuration/version number displayed still does not match that listed in Table 1, contact your local Data I/O Service Center for assistance.

   If the configuration/version number listed in Table 1 is displayed, then the update kit firmware installation is complete.
7. Using an indelible ink pen, write the serial number of your unit on the serial number label provided. Affix the enclosed label over the existing label on the back side of the front panel. The UniPak 2 label location is shown in Figure 1, Step 1. The UniPak 2B label is located on the vertical surface facing the indicated UniPak 2 label location.

   If you are installing a UniPak 2 to 2B conversion kit, complete the conversion kit installation at this time, starting with the subsection Testing the UniPak 2B.

   If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete that section before doing the acceptance test.

   If you are updating a UniPak 2B, an acceptance test was included in the user note. If you want to re-accept the UniPak 2B after updating it, perform the acceptance test procedures as directed in the enclosed acceptance test manual.

Installed 8-14-90
a Fanzoi

UNIPAK 2/2B™

Software Update Kit

985-0002-018 July 1990

Data I/O has made every attempt to ensure that the information in this document is accurate and complete. However, Data I/O assumes no liability for errors, or for any damages that result from use of this document or the equipment that it accompanies.

Data I/O reserves the right to make changes to this document without notice at any time.

ORDERING INFORMATION

When ordering this manual, use Part Number 985-0002-018.
Applies to: Engineering part numbers 953-0002-022 and up
and 953-0017-016 and up.

UniPak 2™ and UniPak 2B™ are trademarks of Data I/O Corporation.

Copyright Data I/O Corporation, 1989, 1990. All rights reserved.

INTRODUCTION

WARNING

The procedures described in this document are intended for use only by personnel qualified to service electronic equipment. Do not attempt to perform these procedures unless you are qualified to do so.

This manual provides the software update instructions necessary for updating either the UniPak 2 or the UniPak 2B. The parts included in each of the update kits are listed in Table 1 below:

Table 1. Software Update Kit Parts

Type of Kit	Description	Quantity	Data I/O Part No.	Installation Location
UniPak 2	EPROM	1	324-0059-051	U19
	EPROM	1	324-0059-052	U20
	Decode PAL	1	324-1760-012	U13
	Label	1	–	
	Documentation Notice	1	090-0332	
	UniPak 2 User Notes	1	984-0001	
UniPak 2B	EPROM	1	324-0059-051	U19
	EPROM	1	324-0059-052	U20
	Decode PAL	1	324-1760-011	U13
	Label	1	–	
	UniPak 2B Device List	1	984-0179	
	UniPak 2B Acceptance Test	1	984-0179	
	UniPak 2B User Notes	1	984-0179	

Firmware Configuration/Version Number: D2AC VER 22.0

CAUTION

The software update kit EPROMs are static-sensitive. Observe standard handling precautions, such as performing the update kit procedures at an anti-static workstation or wearing a grounded wrist-strap, otherwise, damage to the EPROMs may result.

UNIPAK 2/2B SOFTWARE UPDATE KIT INSTALLATION

The following paragraphs describe how to install the software update kit. You will need the following tools for installation of the kit:

- One Phillips-head screwdriver (medium size, #1 or #2)
- One slot-head screwdriver (medium size)
- One pair of needle-nose pliers
- IC extractor tool, or small slot-head screwdriver
- Soldering Iron

For the Software Update Kit to work, your UniPak 2/2B must have a 701-2126 Memory Board. To determine if your pak has the correct memory board, perform the following steps:

1. Install the UniPak 2/2B in the programmer and turn the programmer on.
2. Press **SELECT**. Type **E F** on the programmer keyboard and then press **START**.

If the display does not show version 13.0 or greater, the new Memory Board must be installed. A hardware update kit (951-0045) is required.

NOTE

If you are installing only the Software Update Kit, go directly to the UniPak 2/2B Disassembly section on the following page.

If you are installing the Hardware Update Kit, go to UniPak 2/2B Disassembly section of the Hardware Update Kit manual. Complete the instructions and when instructed to do so, go to the Firmware Installation section in this manual.

If you are installing a UniPak 2 to 2B Conversion Kit and/or the Hardware Update Kit, begin installing the conversion kit first. When the conversion kit instructions direct you to install the software and/or hardware update kit:

1. a. *If you are installing a new memory board, go to step 6 of the Hardware Update Kit manual, complete the instructions and then go directly to the Firmware Installation section in this manual.*
   b. *If you are not installing a new memory board, go directly to the Firmware Installation section in this manual.*
2. *Complete the software update kit installation as directed in the Firmware Installation section of this manual.*
3. *Proceed to the Testing the UniPak 2B section of the conversion kit manual and*
   a. *If the conversion kit was installed, complete the conversion kit installation.*
   b. *If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete the installation there.*

UniPak 2/2B Disassembly

To disassemble the UniPak 2/2B for installation of the updated firmware, follow the procedures listed below.

1. Remove the UniPak 2/2B from the programmer, if it is installed.
2. Set the UniPak 2/2B face down on the flat surface of a static-free workstation.
3. Using the medium size slot-head screwdriver, unscrew the captive fasteners (Figure 1, Step 1) until they hang loosely; the fasteners will not separate from their standoffs.
4. Lift the card cage up slightly, then pull out (as shown in Figure 1, Step 2) to unlock the flanges.

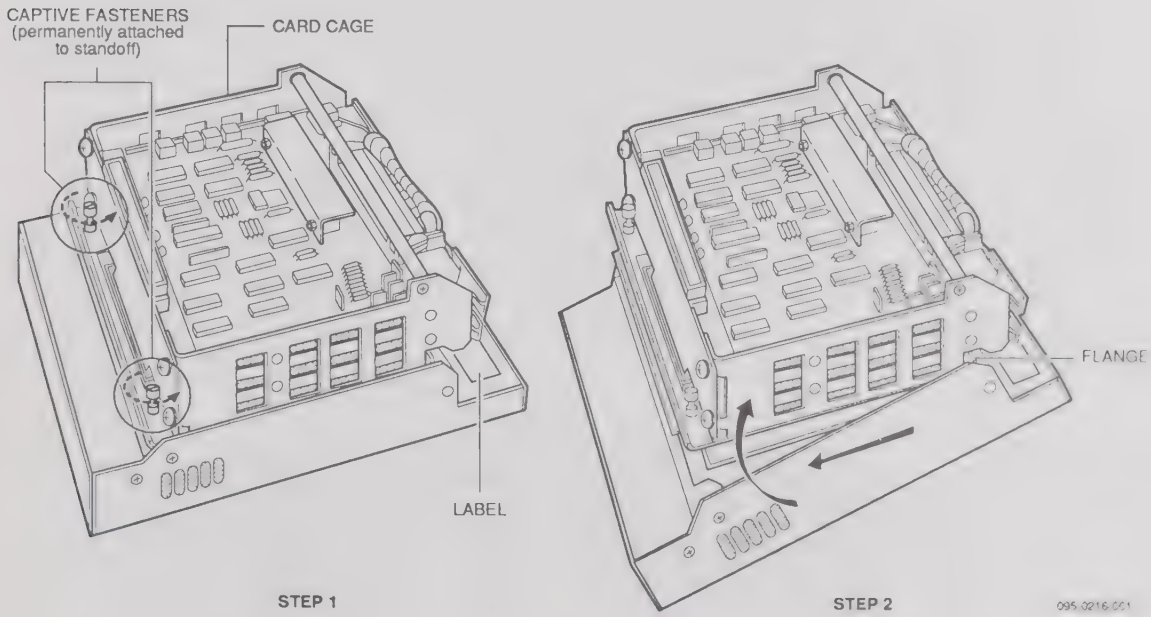


Figure 1. UniPak 2/2B Disassembly
(UniPak 2 shown)

5. Lift the card cage up and out of its top cover until you can see the socketboard interconnect cable (see Figure 2). Do not detach the socketboard interconnect cable.
6. Turn the card cage over and set it on the flat surface next to the top cover. This step exposes the armite or mylar shield which covers the memory board.

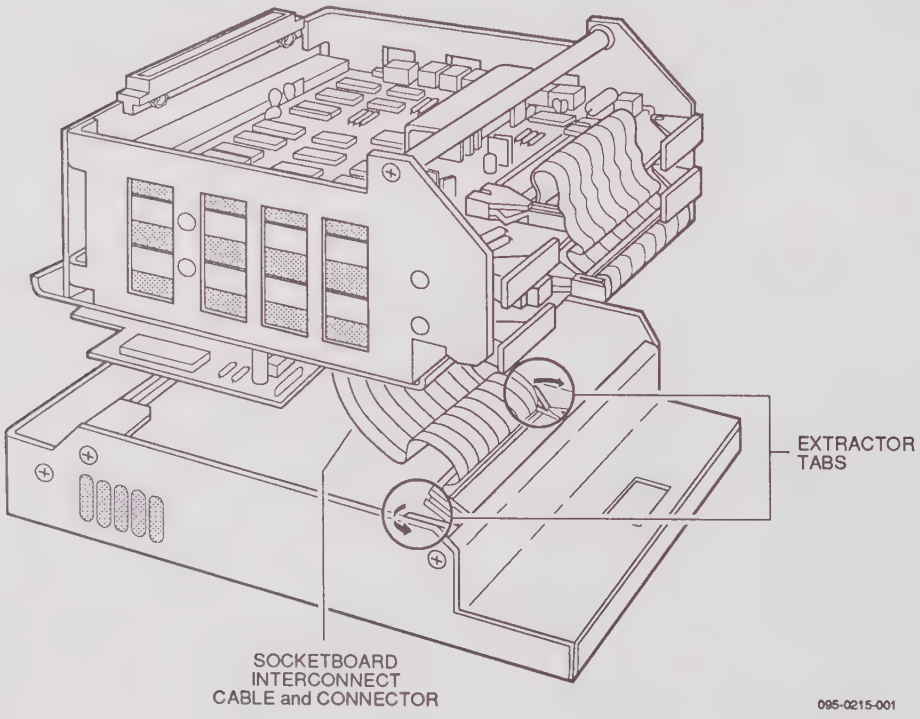


Figure 2. Socketboard Interconnect Cable

7. Remove the two Phillips-head screws and armite or mylar shield from the memory board (see Figure 3). Retain the washers and screws for reassembly. (If you are updating a UniPak 2B that was factory built, rather than a field conversion, it will not contain any washers.)
8. Pull the memory board straight up to unplug it from the card edge connector (as shown in Figure 3).

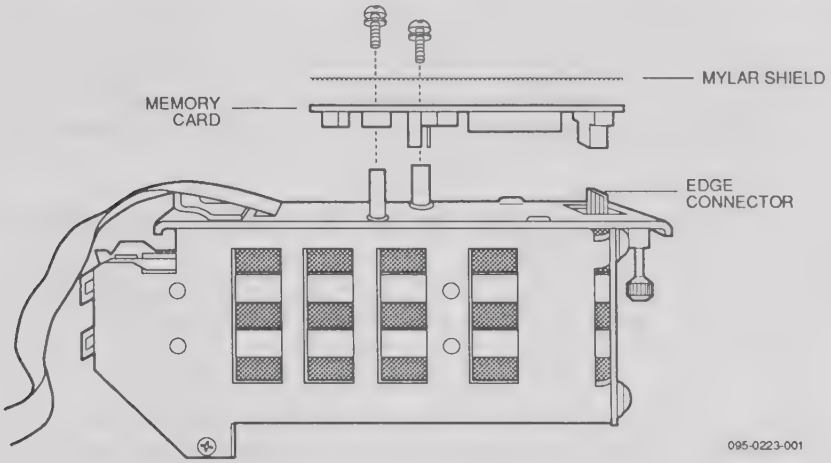


Figure 3. Memory Board Removal

9. Turn the 701-2126 memory board over so the component side faces up (Figure 4) in preparation for firmware installation.

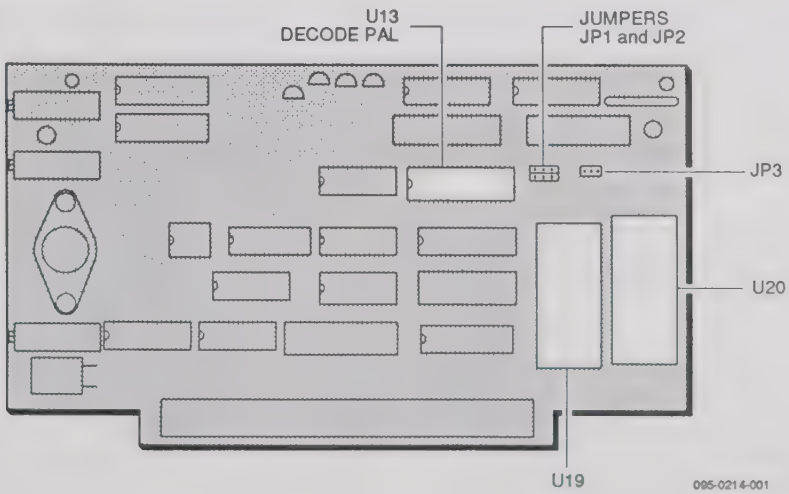


Figure 4. Update Component Location

Table 2. Jumper Configuration

Jumper	Position
JP1	Position B
JP2	Position B
JP3	Position B

Firmware Installation

The following steps describe how to install the firmware components of the update kit into your disassembled UniPak 2/2B. Follow the procedures in the order that they are presented here.

CAUTION

The software update kit EPROMs are static-sensitive. Perform the following procedures at a static-free work station to prevent static-related damage to the EPROMs.

1. Remove EPROMs U19, U20 and decode PAL U13 (see figure 4) from the memory board using an IC extractor tool or small slot-head screwdriver.
2. Refer to Table 2 for jumper configurations. If any jumpers are not in the correct locations, use the needle-nose pliers and soldering iron to change them to the correct location.

NOTE

Prior to installing the firmware, check the socket contacts to ensure that they are not damaged. If any socket contact is damaged, repair or replace that part before proceeding with the firmware installation.

3. Install the software update kit Decode PAL U13 in memory board socket U13. Refer to Table 1 for software update kit firmware part numbers and their corresponding installation locations.

WARNING

When installing EPROMs be sure to bottom justify them in the socket (Figure 5).

4. Install the software update kit EPROMs U19 and U20 in sockets U19 and U20, respectively. Refer to table 1 for software update kit component part numbers and their corresponding installation locations.

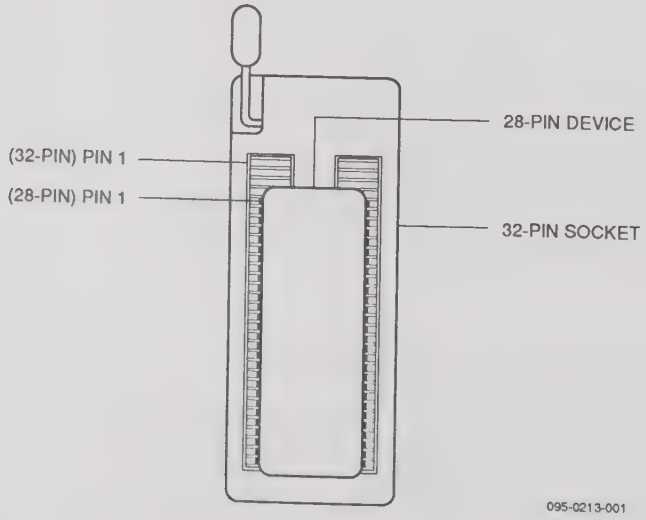


Figure 5. EPROM Installation Alignment

UniPak 2/2B Reassembly and Testing

Reassembly of the UniPak 2/2B is performed by reversing the disassembly procedures. Follow the steps listed below and refer to Figures 1 through 3 on the previous pages.

1. Plug the memory board into its card cage edge connector (figure 3) until it is firmly seated.
2. Replace the armite or mylar shield, washers (if included) and two Phillips-head screws.
3. Reinsert the card cage into the top cover with the memory board facing into the top cover (Figure 2). Tilt the card cage up and push gently forward to lock the top cover's flange between the card cage's top and bottom flanges (Figure 1, Step 2). Then gently set the card cage back into the top cover.
4. Using the medium size slot-head screwdriver, tighten the captive fastener slot screws finger tight.
5. Perform a self-test on the UniPak 2/2B by installing it in a programmer and applying power.

   If the programmer fails to power up correctly, or the self-test message is not displayed, check to make sure that all of the software update kit installation procedures (and conversion kit installation procedures, if you are installing the conversion kit) were performed correctly. If the self-test fails again, contact your local Data I/O Service Center for assistance.
6. Verify the correct firmware configuration/version number by pressing **SELECT E F START** on the programmer's keyboard. Check the programmer display for the four-character configuration number and the version number. See the bottom of Table 1 on the first page of this document for the correct configuration and version numbers.

   If the correct configuration and version numbers are not displayed, the firmware has not been installed correctly. Check to make sure that all installation procedures were performed correctly. Make sure that all PROMs are fully inserted into their sockets and are making proper contact at their connections. Install the UniPak 2/2B in a programmer and again press **SELECT E F START**. If the configuration/version number displayed still does not match that listed in Table 1, contact your local Data I/O Service Center for assistance.

   If the configuration/version number listed in Table 1 is displayed, then the update kit firmware installation is complete.
7. Using an indelible ink pen, write the serial number of your unit on the serial number label provided. Affix the enclosed label over the existing label on the back side of the front panel. The UniPak 2 label location is shown in Figure 1, Step 1. The UniPak 2B label is located on the vertical surface facing the indicated UniPak 2 label location.

   If you are installing a UniPak 2 to 2B conversion kit, complete the conversion kit installation at this time, starting with the subsection Testing the UniPak 2B.

   If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete that section before doing the acceptance test.

   If you are updating a UniPak 2B, an acceptance test was included in the user note. If you want to re-accept the UniPak 2B after updating it, perform the acceptance test procedures as directed in the enclosed acceptance test manual.

Installed
5-3-90

UNIPAK 2/2B™

Software Update Kit

985-0002-017 *March 1990*

Data I/O has made every attempt to ensure that the information in this document is accurate and complete. However, Data I/O assumes no liability for errors, or for any damages that result from use of this document or the equipment that it accompanies.

Data I/O reserves the right to make changes to this document without notice at any time.

ORDERING INFORMATION

When ordering this manual, use Part Number 985-0002-017.
Applies to: Engineering part numbers 953-0002-021 and up
and 953-0017-015 and up.

UniPak 2™ and UniPak 2B™ are trademarks of Data I/O Corporation.

Copyright Data I/O Corporation, 1989, 1990. All rights reserved.

INTRODUCTION

WARNING

The procedures described in this document are intended for use only by personnel qualified to service electronic equipment. Do not attempt to perform these procedures unless you are qualified to do so.

This manual provides the software update instructions necessary for updating either the UniPak 2 or the UniPak 2B. The parts included in each of the update kits are listed in Table 1 below:

Table 1. Software Update Kit Parts

Type of Kit	Description	Quantity	Data I/O Part No.	Installation Location
UniPak 2	EPROM	1	324-0059-049	U19
	EPROM	1	324-0059-050	U20
	Decode PAL	1	324-1760-011	U13
	Label	1	–	
	Documentation Notice	1	090-0332	
	UniPak 2 User Notes	1	984-0001	
UniPak 2B	EPROM	1	324-0059-049	U19
	EPROM	1	324-0059-050	U20
	Decode PAL	1	324-1760-010	U13
	Label	1	–	
	UniPak 2B Device List	1	984-0179	
	UniPak 2B Acceptance Test	1	984-0179	
	UniPak 2B User Notes	1	984-0179	

Firmware Configuration/Version Number: E110 VER 21.0

CAUTION

The software update kit EPROMs are static-sensitive. Observe standard handling precautions, such as performing the update kit procedures at an anti-static workstation or wearing a grounded wrist-strap, otherwise, damage to the EPROMs may result.

UNIPAK 2/2B SOFTWARE UPDATE KIT INSTALLATION

The following paragraphs describe how to install the software update kit. You will need the following tools for installation of the kit:

- One Phillips-head screwdriver (medium size, #1 or #2)
- One slot-head screwdriver (medium size)
- One pair of needle-nose pliers
- IC extractor tool, or small slot-head screwdriver
- Soldering Iron

For the Software Update Kit to work, your UniPak 2/2B must have a 701-2126 Memory Board. To determine if your pak has the correct memory board, perform the following steps:

1. Install the UniPak 2/2B in the programmer and turn the programmer on.

2. Press **SELECT**. Type **E F** on the programmer keyboard and then press **START**.

If the display does not show version 13.0 or greater, the new Memory Board must be installed. A hardware update kit (951-0045) is required.

NOTE

If you are installing only the Software Update Kit, go directly to the UniPak 2/2B Disassembly section on the following page.

If you are installing the Hardware Update Kit, go to UniPak 2/2B Disassembly section of the Hardware Update Kit manual. Complete the instructions and when instructed to do so, go to the Firmware Installation section in this manual.

If you are installing a UniPak 2 to 2B Conversion Kit and/or the Hardware Update Kit, begin installing the conversion kit first. When the conversion kit instructions direct you to install the software and/or hardware update kit:

1. a. *If you are installing a new memory board, go to step 6 of the Hardware Update Kit manual, complete the instructions and then go directly to the Firmware Installation section in this manual.*

   b. *If you are not installing a new memory board, go directly to the Firmware Installation section in this manual.*

2. *Complete the software update kit installation as directed in the Firmware Installation section of this manual.*

3. *Proceed to the Testing the UniPak 2B section of the conversion kit manual and*

   a. *If the conversion kit was installed, complete the conversion kit installation.*

   b. *If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete the installation there.*

UniPak 2/2B Disassembly

To disassemble the UniPak 2/2B for installation of the updated firmware, follow the procedures listed below.

1. Remove the UniPak 2/2B from the programmer, if it is installed.
2. Set the UniPak 2/2B face down on the flat surface of a static-free workstation.
3. Using the medium size slot-head screwdriver, unscrew the captive fasteners (Figure 1, Step 1) until they hang loosely; the fasteners will not separate from their standoffs.
4. Lift the card cage up slightly, then pull out (as shown in Figure 1, Step 2) to unlock the flanges.

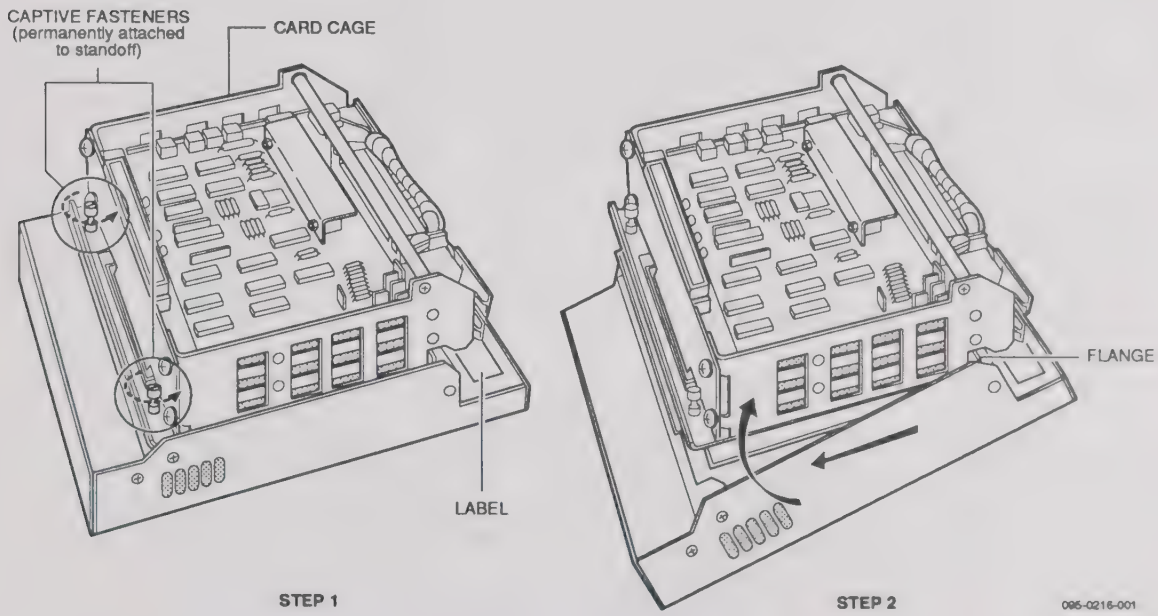


Figure 1. UniPak 2/2B Disassembly
(UniPak 2 shown)

5. Lift the card cage up and out of its top cover until you can see the socketboard interconnect cable (see Figure 2). Do not detach the socketboard interconnect cable.
6. Turn the card cage over and set it on the flat surface next to the top cover. This step exposes the armite or mylar shield which covers the memory board.

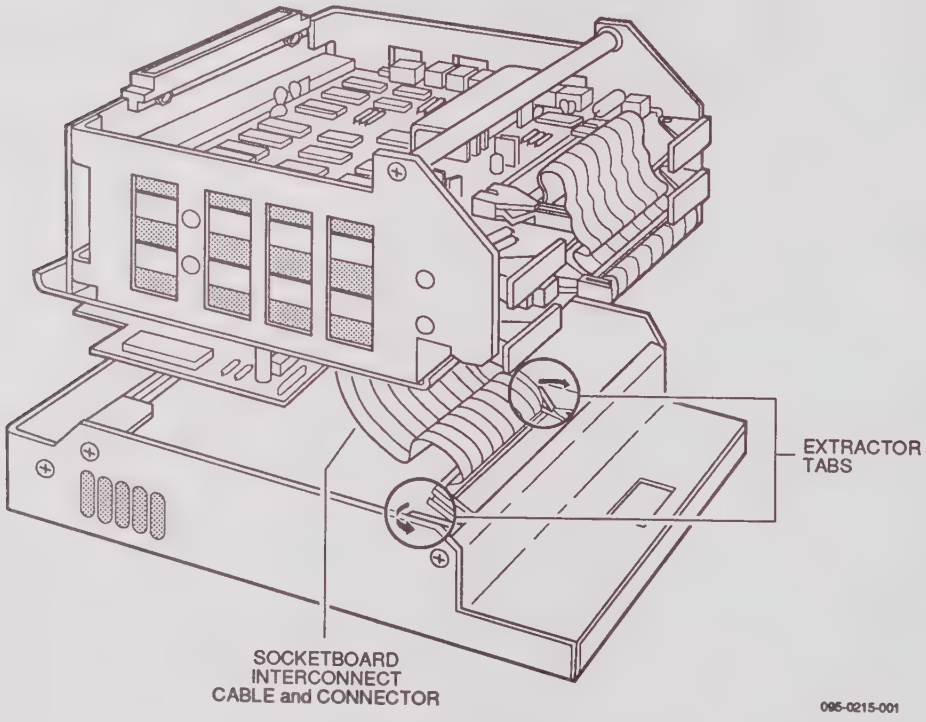


Figure 2. Socketboard Interconnect Cable

7. Remove the two Phillips-head screws and armite or mylar shield from the memory board (see Figure 3). Retain the washers and screws for reassembly. (If you are updating a UniPak 2B that was factory built, rather than a field conversion, it will not contain any washers.)
8. Pull the memory board straight up to unplug it from the card edge connector (as shown in Figure 3).

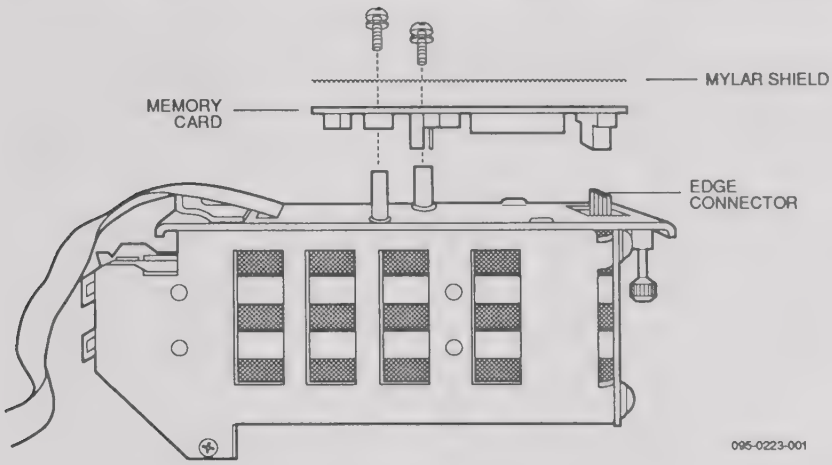


Figure 3. Memory Board Removal

9. Turn the 701-2126 memory board over so the component side faces up (Figure 4) in preparation for firmware installation.

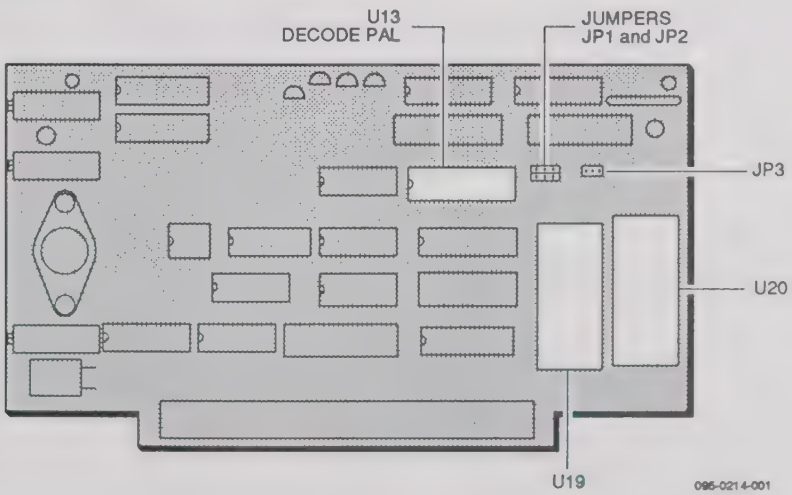


Figure 4. Update Component Location

Table 2. Jumper Configuration

Jumper	Position
JP1	Position B
JP2	Position A
JP3	Position B

Firmware Installation

The following steps describe how to install the firmware components of the update kit into your disassembled UniPak 2/2B. Follow the procedures in the order that they are presented here.

CAUTION

The software update kit EPROMs are static-sensitive. Perform the following procedures at a static-free work station to prevent static-related damage to the EPROMs.

1. Remove EPROMs U19, U20 and decode PAL U13 (see figure 4) from the memory board using an IC extractor tool or small slot-head screwdriver.
2. Refer to Table 2 for jumper configurations. If any jumpers are not in the correct locations, use the needle-nose pliers and soldering iron to change them to the correct location.

NOTE

Prior to installing the firmware, check the socket contacts to ensure that they are not damaged. If any socket contact is damaged, repair or replace that part before proceeding with the firmware installation.

3. Install the software update kit Decode PAL U13 in memory board socket U13. Refer to Table 1 for software update kit firmware part numbers and their corresponding installation locations.

WARNING

When installing EPROMs be sure to bottom justify them in the socket (Figure 5).

4. Install the software update kit EPROMs U19 and U20 in sockets U19 and U20, respectively. Refer to table 1 for software update kit component part numbers and their corresponding installation locations.

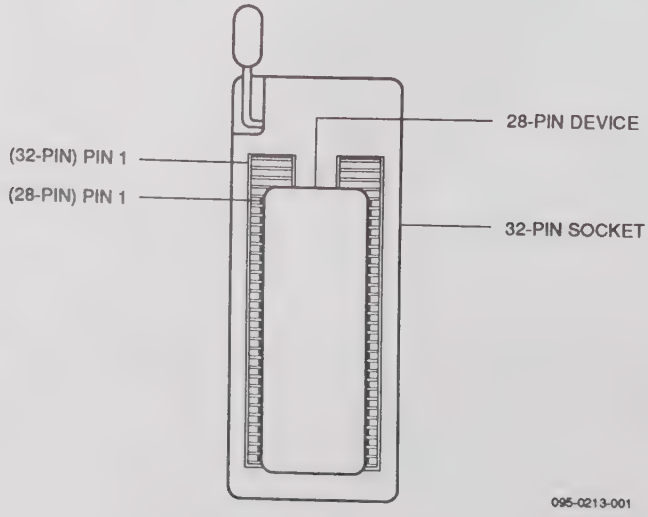


Figure 5. EPROM Installation Alignment

UniPak 2/2B Reassembly and Testing

Reassembly of the UniPak 2/2B is performed by reversing the disassembly procedures. Follow the steps listed below and refer to Figures 1 through 3 on the previous pages.

1. Plug the memory board into its card cage edge connector (figure 3) until it is firmly seated.
2. Replace the armite or mylar shield, washers (if included) and two Phillips-head screws.
3. Reinsert the card cage into the top cover with the memory board facing into the top cover (Figure 2). Tilt the card cage up and push gently forward to lock the top cover's flange between the card cage's top and bottom flanges (Figure 1, Step 2). Then gently set the card cage back into the top cover.
4. Using the medium size slot-head screwdriver, tighten the captive fastener slot screws finger tight.
5. Perform a self-test on the UniPak 2/2B by installing it in a programmer and applying power.

   If the programmer fails to power up correctly, or the self-test message is not displayed, check to make sure that all of the software update kit installation procedures (and conversion kit installation procedures, if you are installing the conversion kit) were performed correctly. If the self-test fails again, contact your local Data I/O Service Center for assistance.
6. Verify the correct firmware configuration/version number by pressing **SELECT E F START** on the programmer's keyboard. Check the programmer display for the four-character configuration number and the version number. See the bottom of Table 1 on the first page of this document for the correct configuration and version numbers.

   If the correct configuration and version numbers are not displayed, the firmware has not been installed correctly. Check to make sure that all installation procedures were performed correctly. Make sure that all PROMs are fully inserted into their sockets and are making proper contact at their connections. Install the UniPak 2/2B in a programmer and again press **SELECT E F START**. If the configuration/version number displayed still does not match that listed in Table 1, contact your local Data I/O Service Center for assistance.

   If the configuration/version number listed in Table 1 is displayed, then the update kit firmware installation is complete.
7. Using an indelible ink pen, write the serial number of your unit on the serial number label provided. Affix the enclosed label over the existing label on the back side of the front panel. The UniPak 2 label location is shown in Figure 1, Step 1. The UniPak 2B label is located on the vertical surface facing the indicated UniPak 2 label location.

   If you are installing a UniPak 2 to 2B conversion kit, complete the conversion kit installation at this time, starting with the subsection Testing the UniPak 2B.

   If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete that section before doing the acceptance test.

   If you are updating a UniPak 2B, an acceptance test was included in the user note. If you want to re-accept the UniPak 2B after updating it, perform the acceptance test procedures as directed in the enclosed acceptance test manual.

Installed
12-13-89
Fanyo

UNIPAK 2/2B™

Software Update Kit

985-0002-016 *November 1989*

Data I/O has made every attempt to ensure that the information in this document is accurate and complete. However, Data I/O assumes no liability for errors, or for any damages that result from use of this document or the equipment that it accompanies.

Data I/O reserves the right to make changes to this document without notice at any time.

ORDERING INFORMATION

When ordering this manual, use Part Number 985-0002-016.
Applies to: Engineering part numbers 953-0002-020 and up
and 953-0017-014 and up.

UniPak 2™ and UniPak 2B™ are trademarks of Data I/O Corporation.

Copyright Data I/O Corporation, 1989. All rights reserved.

INTRODUCTION

WARNING

The procedures described in this document are intended for use only by personnel qualified to service electronic equipment. Do not attempt to perform these procedures unless you are qualified to do so.

This manual provides the software update instructions necessary for updating either the UniPak 2 or the UniPak 2B. The parts included in each of the update kits are listed in Table 1 below:

Table 1. Software Update Kit Parts

Type of Kit	Description	Quantity	Data I/O Part No.	Installation Location
UniPak 2	EPROM	1	324-0059-047	U19
	EPROM	1	324-0059-048	U20
	Decode PAL	1	324-1760-010	U13
	Label	1	–	
	Documentation Notice	1	090-0332	
	UniPak 2 User Notes	1	984-0001	
UniPak 2B	EPROM	1	324-0059-047	U19
	EPROM	1	324-0059-048	U20
	Decode PAL	1	324-1760-010	U13
	Label	1	–	
	UniPak 2B Device List	1	984-0179	
	UniPak 2B Acceptance Test	1	984-0179	
	UniPak 2B User Notes	1	984-0179	

Firmware Configuration/Version Number: 5D9B VER 20.0

CAUTION

The software update kit EPROMs are static-sensitive. Observe standard handling precautions, such as performing the update kit procedures at an anti-static workstation or wearing a grounded wrist-strap, otherwise, damage to the EPROMs may result.

UNIPAK 2/2B SOFTWARE UPDATE KIT INSTALLATION

The following paragraphs describe how to install the software update kit. You will need the following tools for installation of the kit:

- One Phillips-head screwdriver (medium size, #1 or #2)
- One slot-head screwdriver (medium size)
- One pair of needle-nose pliers
- IC extractor tool, or small slot-head screwdriver
- Soldering Iron

For the Software Update Kit to work, your UniPak 2/2B must have a 701-2126 Memory Board. To determine if your pak has the correct memory board, perform the following steps:

1. Install the UniPak 2/2B in the programmer and turn the programmer on.

2. Press **SELECT**. Type **E F** on the programmer keyboard and then press **START**.

If the display does not show version 13.0 or greater, the new Memory Board must be installed. A hardware update kit (951-0045) is required.

NOTE

If you are installing only the Software Update Kit, go directly to the UniPak 2/2B Disassembly section on the following page.

If you are installing the Hardware Update Kit, go to UniPak 2/2B Disassembly section of the Hardware Update Kit manual. Complete the instructions and when instructed to do so, go to the Firmware Installation section in this manual.

If you are installing a UniPak 2 to 2B Conversion Kit and/or the Hardware Update Kit, begin installing the conversion kit first. When the conversion kit instructions direct you to install the software and/or hardware update kit:

1. a. *If you are installing a new memory board, go to step 6 of the Hardware Update Kit manual, complete the instructions and then go directly to the Firmware Installation section in this manual.*

   b. *If you are not installing a new memory board, go directly to the Firmware Installation section in this manual.*

2. *Complete the software update kit installation as directed in the Firmware Installation section of this manual.*

3. *Proceed to the Testing the UniPak 2B section of the conversion kit manual and*

   a. *If the conversion kit was installed, complete the conversion kit installation.*

   b. *If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete the installation there.*

UniPak 2/2B Disassembly

To disassemble the UniPak 2/2B for installation of the updated firmware, follow the procedures listed below.

1. Remove the UniPak 2/2B from the programmer, if it is installed.
2. Set the UniPak 2/2B face down on the flat surface of a static-free workstation.
3. Using the medium size slot-head screwdriver, unscrew the captive fasteners (Figure 1, Step 1) until they hang loosely; the fasteners will not separate from their standoffs.
4. Lift the card cage up slightly, then pull out (as shown in Figure 1, Step 2) to unlock the flanges.

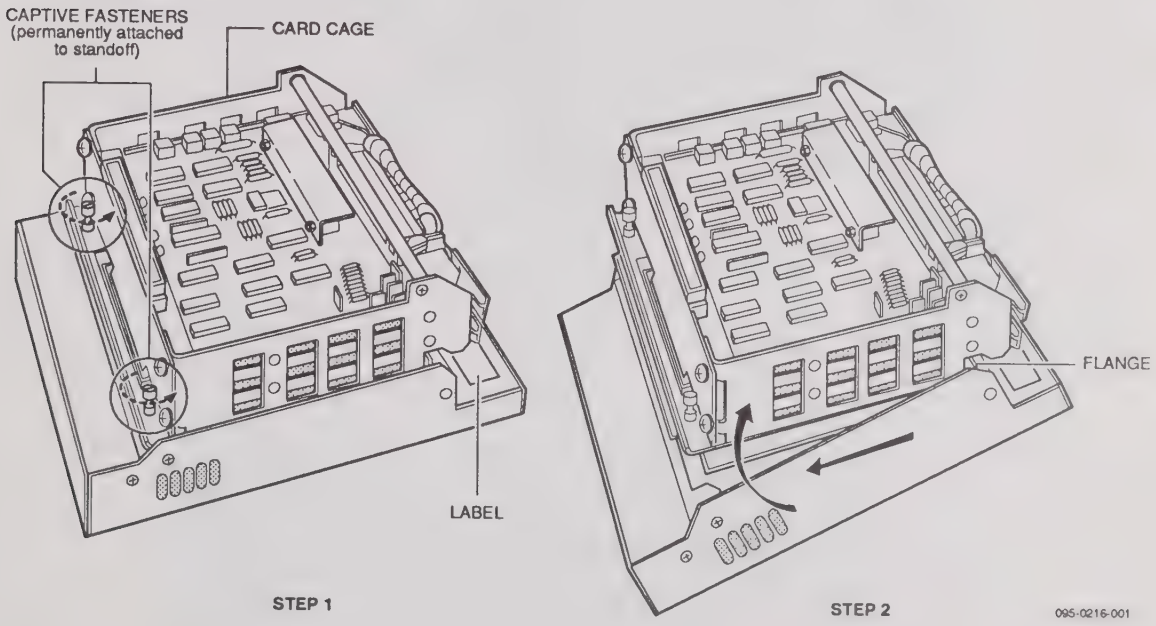


Figure 1. UniPak 2/2B Disassembly
(UniPak 2 shown)

5. Lift the card cage up and out of its top cover until you can see the socketboard interconnect cable (see Figure 2). Do not detach the socketboard interconnect cable.

6. Turn the card cage over and set it on the flat surface next to the top cover. This step exposes the armite or mylar shield which covers the memory board.

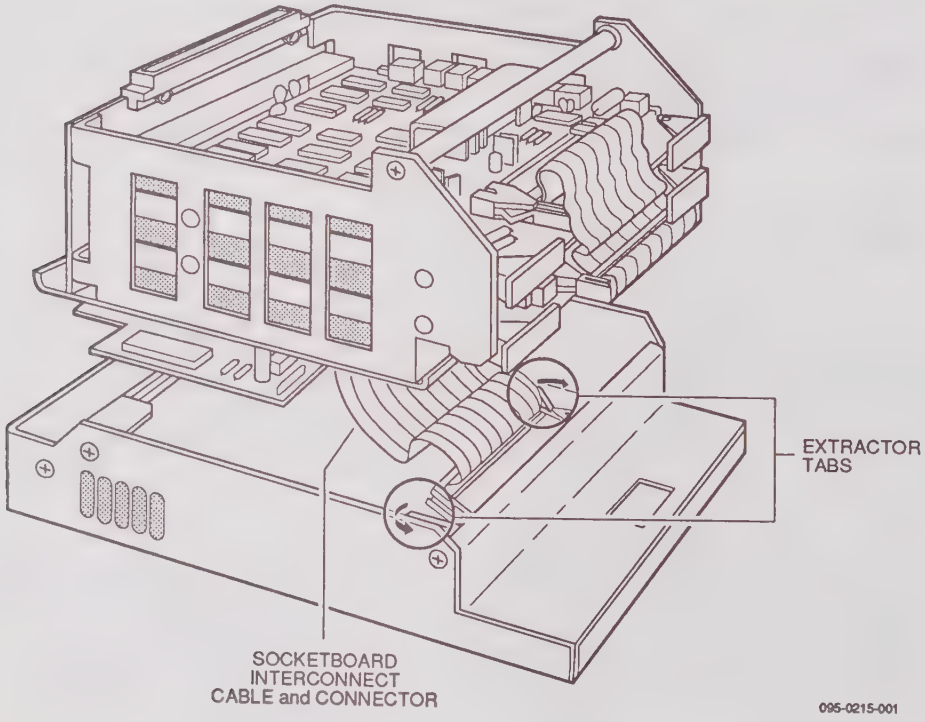


Figure 2. Socketboard Interconnect Cable

7. Remove the two Phillips-head screws and armite or mylar shield from the memory board (see Figure 3). Retain the washers and screws for reassembly. (If you are updating a UniPak 2B that was factory built, rather than a field conversion, it will not contain any washers.)
8. Pull the memory board straight up to unplug it from the card edge connector (as shown in Figure 3).

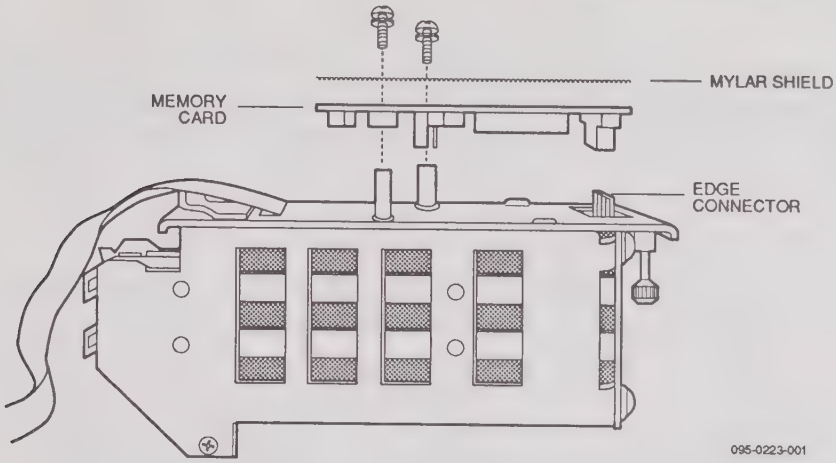


Figure 3. Memory Board Removal

9. Turn the 701-2126 memory board over so the component side faces up (Figure 4) in preparation for firmware installation.

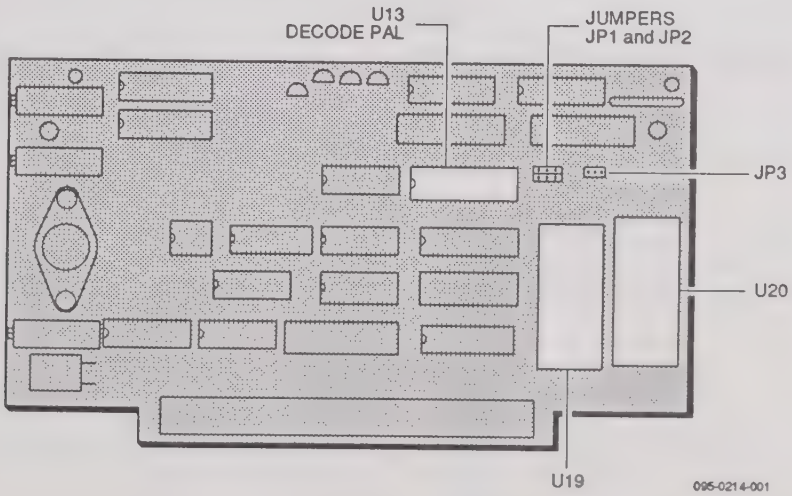


Figure 4. Update Component Location

Table 2. Jumper Configuration

Jumper	Position
JP1	Position B
JP2	Position A
JP3	Position B

Firmware Installation

The following steps describe how to install the firmware components of the update kit into your disassembled UniPak 2/2B. Follow the procedures in the order that they are presented here.

CAUTION

The software update kit EPROMs are static-sensitive. Perform the following procedures at a static-free work station to prevent static-related damage to the EPROMs.

1. Remove EPROMs U19, U20 and decode PAL U13 (see figure 4) from the memory board using an IC extractor tool or small slot-head screwdriver.
2. Refer to Table 2 for jumper configurations. If any jumpers are not in the correct locations, use the needle-nose pliers and soldering iron to change them to the correct location.

NOTE

Prior to installing the firmware, check the socket contacts to ensure that they are not damaged. If any socket contact is damaged, repair or replace that part before proceeding with the firmware installation.

3. Install the software update kit Decode PAL U13 in memory board socket U13. Refer to Table 1 for software update kit firmware part numbers and their corresponding installation locations.

WARNING

When installing EPROMs be sure to bottom justify them in the socket (Figure 5).

4. Install the software update kit EPROMs U19 and U20 in sockets U19 and U20, respectively. Refer to table 1 for software update kit component part numbers and their corresponding installation locations.

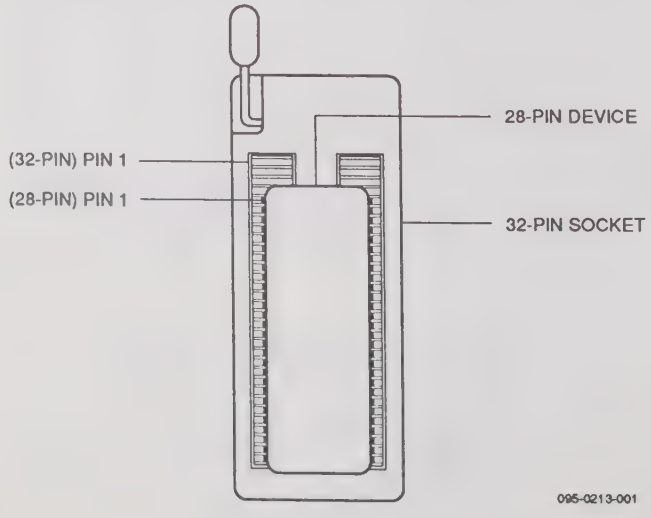


Figure 5. EPROM Installation Alignment

UniPak 2/2B Reassembly and Testing

Reassembly of the UniPak 2/2B is performed by reversing the disassembly procedures. Follow the steps listed below and refer to Figures 1 through 3 on the previous pages.

1. Plug the memory board into its card cage edge connector (figure 3) until it is firmly seated.
2. Replace the armite or mylar shield, washers (if included) and two Phillips-head screws.
3. Reinsert the card cage into the top cover with the memory board facing into the top cover (Figure 2). Tilt the card cage up and push gently forward to lock the top cover's flange between the card cage's top and bottom flanges (Figure 1, Step 2). Then gently set the card cage back into the top cover.
4. Using the medium size slot-head screwdriver, tighten the captive fastener slot screws finger tight.
5. Perform a self-test on the UniPak 2/2B by installing it in a programmer and applying power.

   If the programmer fails to power up correctly, or the self-test message is not displayed, check to make sure that all of the software update kit installation procedures (and conversion kit installation procedures, if you are installing the conversion kit) were performed correctly. If the self-test fails again, contact your local Data I/O Service Center for assistance.
6. Verify the correct firmware configuration/version number by pressing **SELECT E F START** on the programmer's keyboard. Check the programmer display for the four-character configuration number and the version number. See the bottom of Table 1 on the first page of this document for the correct configuration and version numbers.

   If the correct configuration and version numbers are not displayed, the firmware has not been installed correctly. Check to make sure that all installation procedures were performed correctly. Make sure that all PROMs are fully inserted into their sockets and are making proper contact at their connections. Install the UniPak 2/2B in a programmer and again press **SELECT E F START**. If the configuration/version number displayed still does not match that listed in Table 1, contact your local Data I/O Service Center for assistance.

   If the configuration/version number listed in Table 1 is displayed, then the update kit firmware installation is complete.
7. Using an indelible ink pen, write the serial number of your unit on the serial number label provided. Affix the enclosed label over the existing label on the back side of the front panel. The UniPak 2 label location is shown in Figure 1, Step 1. The UniPak 2B label is located on the vertical surface facing the indicated UniPak 2 label location.

   If you are installing a UniPak 2 to 2B conversion kit, complete the conversion kit installation at this time, starting with the subsection Testing the UniPak 2B.

   If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete that section before doing the acceptance test.

   If you are updating a UniPak 2B, an acceptance test was included in the user note. If you want to re-accept the UniPak 2B after updating it, perform the acceptance test procedures as directed in the enclosed acceptance test manual.

Installed 9-26-89
a Fanuc

UNIPAK 2/2B™

Software Update Kit

985-0002-015 *August 1989*

Data I/O has made every attempt to ensure that the information in this document is accurate and complete. However, Data I/O assumes no liability for errors, or for any damages that result from use of this document or the equipment that it accompanies.

Data I/O reserves the right to make changes to this document without notice at any time.

ORDERING INFORMATION

When ordering this manual, use Part Number 985-0002-015.
Applies to: Engineering part numbers 953-0002-019 and up
and 953-0017-013 and up.

UniPak 2™ and UniPak 2B™ are trademarks of Data I/O Corporation.

Copyright Data I/O Corporation, 1989. All rights reserved.

INTRODUCTION

WARNING

The procedures described in this document are intended for use only by personnel qualified to service electronic equipment. Do not attempt to perform these procedures unless you are qualified to do so.

This manual provides the software update instructions necessary for updating either the UniPak 2 or the UniPak 2B. The parts included in each of the update kits are listed in Table 1 below:

Table 1. Software Update Kit Parts

Type of Kit	Description	Quantity	Data I/O Part No.	Installation Location
UniPak 2	EPROM	1	324-0059-045	U19
	EPROM	1	324-0059-046	U20
	Decode PAL	1	324-1760-009	U13
	Label	1	–	
	Documentation Notice	1	090-0332	
	UniPak 2 User Notes	1	984-0001	
UniPak 2B	EPROM	1	324-0059-045	U19
	EPROM	1	324-0059-046	U20
	Decode PAL	1	324-1760-009	U13
	Label	1	–	
	UniPak 2B Device List	1	984-0179	
	UniPak 2B Acceptance Test	1	984-0179	
	UniPak 2B User Notes	1	984-0179	

Firmware Configuration/Version Number: 2946 VER 19.0

CAUTION

The software update kit EPROMs are static-sensitive. Observe standard handling precautions, such as performing the update kit procedures at an anti-static workstation or wearing a grounded wrist-strap, otherwise, damage to the EPROMs may result.

UNIPAK 2/2B SOFTWARE UPDATE KIT INSTALLATION

The following paragraphs describe how to install the software update kit. You will need the following tools for installation of the kit:

- One Phillips-head screwdriver (medium size, #1 or #2)
- One slot-head screwdriver (medium size)
- One pair of needle-nose pliers
- IC extractor tool, or small slot-head screwdriver
- Soldering Iron

For the Software Update Kit to work, your UniPak 2/2B must have a 701-2126 Memory Board. To determine if your pak has the correct memory board, perform the following steps:

1. Install the UniPak 2/2B in the programmer and turn the programmer on.

2. Press **SELECT**. Type **E F** on the programmer keyboard and then press **START**.

If the display does not show version 13.0 or greater, the new Memory Board must be installed. A hardware update kit (951-0045) is required.

NOTE

If you are installing only the Software Update Kit, go directly to the UniPak 2/2B Disassembly section on the following page.

If you are installing the Hardware Update Kit, go to UniPak 2/2B Disassembly section of the Hardware Update Kit manual. Complete the instructions and when instructed to do so, go to the Firmware Installation section in this manual.

If you are installing a UniPak 2 to 2B Conversion Kit and/or the Hardware Update Kit, begin installing the conversion kit first. When the conversion kit instructions direct you to install the software and/or hardware update kit:

1. a. *If you are installing a new memory board, go to step 6 of the Hardware Update Kit manual, complete the instructions and then go directly to the Firmware Installation section in this manual.*

   b. *If you are not installing a new memory board, go directly to the Firmware Installation section in this manual.*

2. *Complete the software update kit installation as directed in the Firmware Installation section of this manual.*

3. *Proceed to the Testing the UniPak 2B section of the conversion kit manual and*

   a. *If the conversion kit was installed, complete the conversion kit installation.*

   b. *If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete the installation there.*

UniPak 2/2B Disassembly

To disassemble the UniPak 2/2B for installation of the updated firmware, follow the procedures listed below.

1. Remove the UniPak 2/2B from the programmer, if it is installed.
2. Set the UniPak 2/2B face down on the flat surface of a static-free workstation.
3. Using the medium size slot-head screwdriver, unscrew the captive fasteners (Figure 1, Step 1) until they hang loosely; the fasteners will not separate from their standoffs.
4. Lift the card cage up slightly, then pull out (as shown in Figure 1, Step 2) to unlock the flanges.

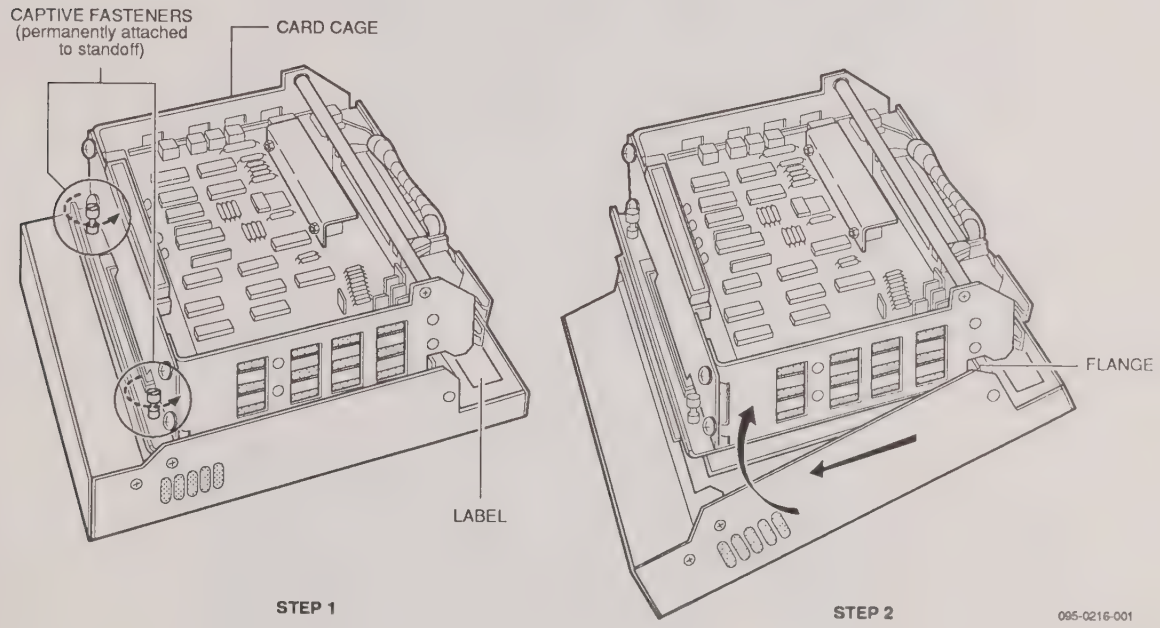


Figure 1. UniPak 2/2B Disassembly
(UniPak 2 shown)

5. Lift the card cage up and out of its top cover until you can see the socketboard interconnect cable (see Figure 2). Do not detach the socketboard interconnect cable.
6. Turn the card cage over and set it on the flat surface next to the top cover. This step exposes the armite or mylar shield which covers the memory board.

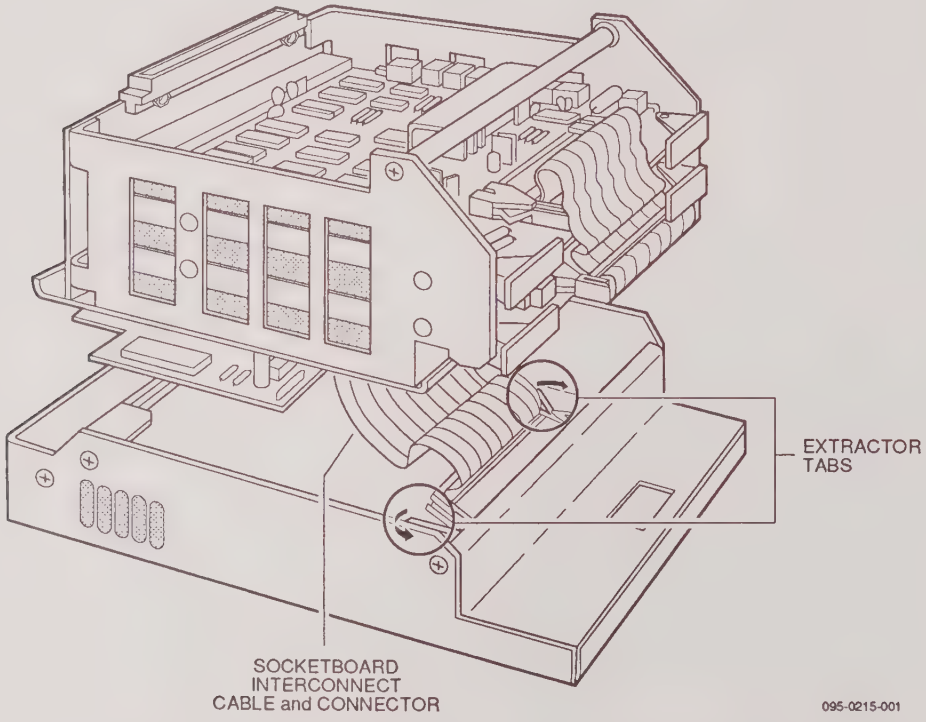


Figure 2. Socketboard Interconnect Cable

7. Remove the two Phillips-head screws and armite or mylar shield from the memory board (see Figure 3). Retain the washers and screws for reassembly. (If you are updating a UniPak 2B that was factory built, rather than a field conversion, it will not contain any washers.)
8. Pull the memory board straight up to unplug it from the card edge connector (as shown in Figure 3).

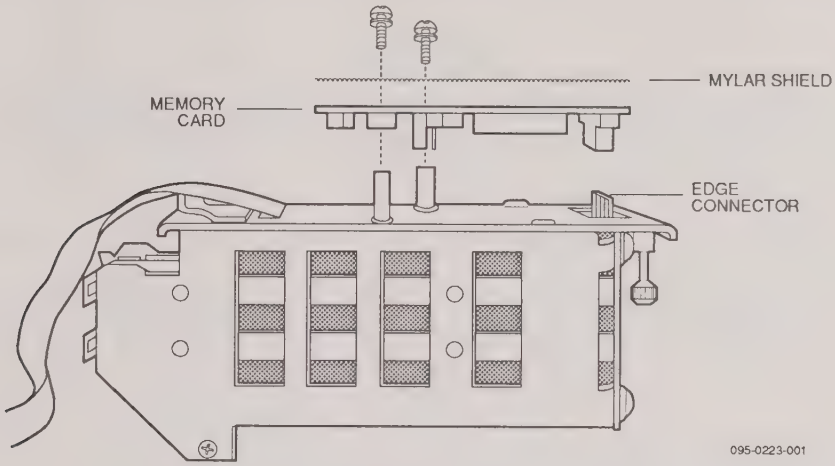


Figure 3. Memory Board Removal

9. Turn the 701-2126 memory board over so the component side faces up (Figure 4) in preparation for firmware installation.

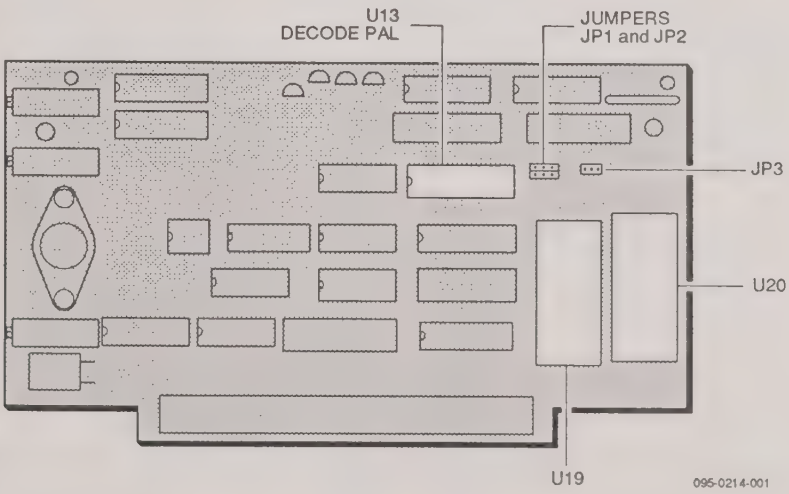


Figure 4. Update Component Location

Table 2. Jumper Configuration

Jumper	Position
JP1	Position B
JP2	Position A
JP3	Position B

Firmware Installation

The following steps describe how to install the firmware components of the update kit into your disassembled UniPak 2/2B. Follow the procedures in the order that they are presented here.

CAUTION

The software update kit EPROMs are static-sensitive. Perform the following procedures at a static-free work station to prevent static-related damage to the EPROMs.

1. Remove EPROMs U19, U20 and decode PAL U13 (see figure 4) from the memory board using an IC extractor tool or small slot-head screwdriver.
2. Refer to Table 2 for jumper configurations. If any jumpers are not in the correct locations, use the needle-nose pliers and soldering iron to change them to the correct location.

NOTE

Prior to installing the firmware, check the socket contacts to ensure that they are not damaged. If any socket contact is damaged, repair or replace that part before proceeding with the firmware installation.

3. Install the software update kit Decode PAL U13 in memory board socket U13. Refer to Table 1 for software update kit firmware part numbers and their corresponding installation locations.

WARNING

When installing EPROMs be sure to bottom justify them in the socket (Figure 5).

4. Install the software update kit EPROMs U19 and U20 in sockets U19 and U20, respectively. Refer to table 1 for software update kit component part numbers and their corresponding installation locations.

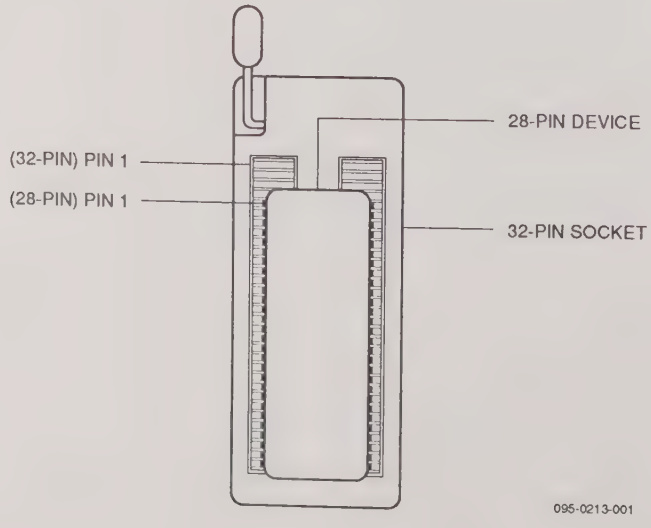


Figure 5. EPROM Installation Alignment

UniPak 2/2B Reassembly and Testing

Reassembly of the UniPak 2/2B is performed by reversing the disassembly procedures. Follow the steps listed below and refer to Figures 1 through 3 on the previous pages.

1. Plug the memory board into its card cage edge connector (figure 3) until it is firmly seated.
2. Replace the armite or mylar shield, washers (if included) and two Phillips-head screws.
3. Reinsert the card cage into the top cover with the memory board facing into the top cover (Figure 2). Tilt the card cage up and push gently forward to lock the top cover's flange between the card cage's top and bottom flanges (Figure 1, Step 2). Then gently set the card cage back into the top cover.
4. Using the medium size slot-head screwdriver, tighten the captive fastener slot screws finger tight.
5. Perform a self-test on the UniPak 2/2B by installing it in a programmer and applying power.

   If the programmer fails to power up correctly, or the self-test message is not displayed, check to make sure that all of the software update kit installation procedures (and conversion kit installation procedures, if you are installing the conversion kit) were performed correctly. If the self-test fails again, contact your local Data I/O Service Center for assistance.
6. Verify the correct firmware configuration/version number by pressing **SELECT E F START** on the programmer's keyboard. Check the programmer display for the four-character configuration number and the version number. See the bottom of Table 1 on the first page of this document for the correct configuration and version numbers.

   If the correct configuration and version numbers are not displayed, the firmware has not been installed correctly. Check to make sure that all installation procedures were performed correctly. Make sure that all PROMs are fully inserted into their sockets and are making proper contact at their connections. Install the UniPak 2/2B in a programmer and again press **SELECT E F START**. If the configuration/version number displayed still does not match that listed in Table 1, contact your local Data I/O Service Center for assistance.

   If the configuration/version number listed in Table 1 is displayed, then the update kit firmware installation is complete.
7. Using an indelible ink pen, write the serial number of your unit on the serial number label provided. Affix the enclosed label over the existing label on the back side of the front panel. The UniPak 2 label location is shown in Figure 1, Step 1. The UniPak 2B label is located on the vertical surface facing the indicated UniPak 2 label location.

   If you are installing a UniPak 2 to 2B conversion kit, complete the conversion kit installation at this time, starting with the subsection Testing the UniPak 2B.

   If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete that section before doing the acceptance test.

   If you are updating a UniPak 2B, an acceptance test was included in the user note. If you want to re-accept the UniPak 2B after updating it, perform the acceptance test procedures as directed in the enclosed acceptance test manual.

UNIPAK 2/2B™

Software Update Kit

985-0002-014 *March 1989*

Installed 4-17-89

Data I/O has made every attempt to ensure that the information in this document is accurate and complete. However, Data I/O assumes no liability for errors, or for any damages that result from use of this document or the equipment that it accompanies.

Data I/O reserves the right to make changes to this document without notice at any time.

ORDERING INFORMATION

When ordering this manual, use Part Number 985-0002-014.
Applies to: Engineering part numbers 953-0002-019 and up
and 953-0017-013 and up.

UniPak 2™ and UniPak 2B™ are trademarks of Data I/O Corporation.

Copyright Data I/O Corporation, 1989. All rights reserved.

INTRODUCTION

WARNING

The procedures described in this document are intended for use only by personnel qualified to service electronic equipment. Do not attempt to perform these procedures unless you are qualified to do so.

This manual provides the software update instructions necessary for updating either the UniPak 2 or the UniPak 2B. The parts included in each of the update kits are listed in Table 1 below:

Table 1. Software Update Kit Parts

Type of Kit	Description	Quantity	Data I/O Part No.	Installation Location
UniPak 2	EPROM	1	324-0059-043	U19
	EPROM	1	324-0059-044	U20
	Decode PAL	1	324-1760-008	U13
	Label	1	–	
	Documentation Notice	1	090-0332	
	UniPak 2 User Notes	1	984-0001	
UniPak 2B	EPROM	1	324-0059-043	U19
	EPROM	1	324-0059-044	U20
	Decode PAL	1	324-1760-008	U13
	Label	1	–	
	UniPak 2B Device List	1	984-0179	
	UniPak 2B Acceptance Test	1	984-0179	
	UniPak 2B User Notes	1	984-0179	

Firmware Configuration/Version Number: A2D6 VER 18.0

CAUTION

The software update kit EPROMs are static-sensitive. Observe standard handling precautions, such as performing the update kit procedures at an anti-static workstation or wearing a grounded wrist-strap, otherwise, damage to the EPROM(s) may result.

UNIPAK 2/2B SOFTWARE UPDATE KIT INSTALLATION

The following paragraphs describe how to install the software update kit. You will need the following tools for installation of the kit:

- One Phillips-head screwdriver (medium size, #1 or #2)
- One slot-head screwdriver (medium size)
- One pair of needle-nose pliers
- IC extractor tool, or small slot-head screwdriver
- Soldering Iron

For the Software Update Kit to work, your UniPak 2/2B must have a 701-2126 Memory Board. To determine if your pak has the correct memory board, perform the following steps:

1. Install the UniPak 2/2B in the programmer and turn the programmer on.

2. Press **SELECT**. Type **E F** on the programmer keyboard and then press **START**.

If the display does not show version 13.0 or greater, the new Memory Board must be installed. A hardware update kit (951-0045) is required.

NOTE

If you are installing only the Software Update Kit, go directly to the UniPak 2/2B Disassembly section on the following page.

If you are installing the Hardware Update Kit, go to UniPak 2/2B Disassembly section of the Hardware Update Kit manual. Complete the instructions and when instructed to do so, go to the Firmware Installation section in this manual.

If you are installing a UniPak 2 to 2B Conversion Kit and/or the Hardware Update Kit, begin installing the conversion kit first. When the conversion kit instructions direct you to install the software and/or hardware update kit:

1. a. *If you are installing a new memory board, go to step 6 of the Hardware Update Kit manual, complete the instructions and then go directly to the Firmware Installation section in this manual.*

   b. *If you are not installing a new memory board, go directly to the Firmware Installation section in this manual.*

2. *Complete the software update kit installation as directed in the Firmware Installation section of this manual.*

3. *Proceed to the Testing the UniPak 2B section of the conversion kit manual and*

   a. *If the conversion kit was installed, complete the conversion kit installation.*

   b. *If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete the installation there.*

UniPak 2/2B Disassembly

To disassemble the UniPak 2/2B for installation of the updated firmware, follow the procedures listed below.

1. Remove the UniPak 2/2B from the programmer, if it is installed.
2. Set the UniPak 2/2B face down on the flat surface of a static-free workstation.
3. Using the medium size slot-head screwdriver, unscrew the captive fasteners (figure 1, step 1) until they hang loosely; the fasteners will not separate from their standoffs.
4. Lift the card cage up slightly, then pull out (as shown in figure 1, step 2) to unlock the flanges.

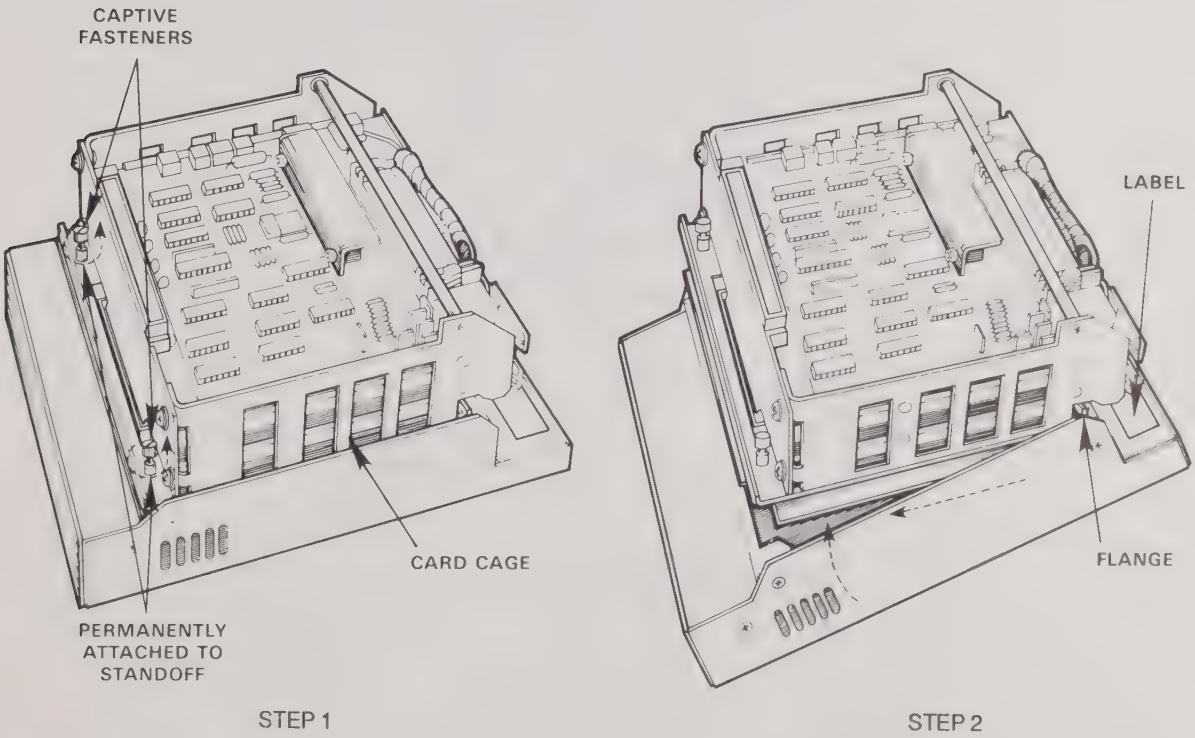


Figure 1. UniPak 2/2B Disassembly
(UniPak 2 shown)

5. Lift the card cage up and out of its top cover until you can see the socketboard interconnect cable (see figure 2). Do not detach the socketboard interconnect cable.
6. Turn the card cage over and set it on the flat surface next to the top cover. This step exposes the armite or mylar shield which covers the memory board.

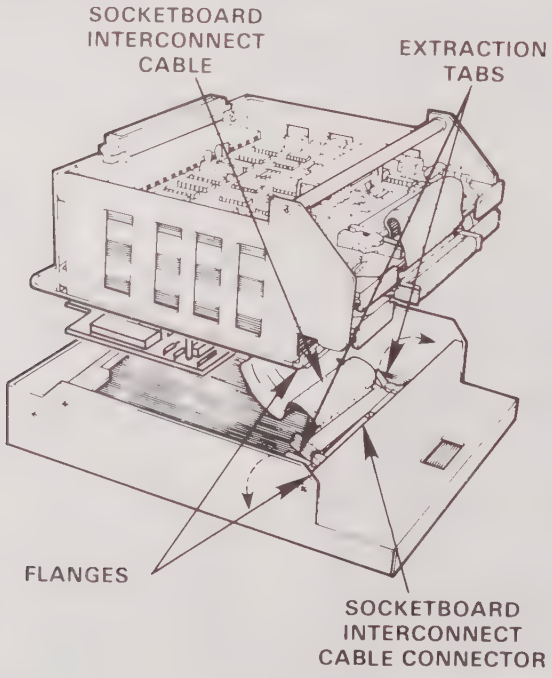


Figure 2. Socketboard Interconnect Cable

7. Remove the two Phillips-head screws and armite or mylar shield from the memory board (see figure 3). Retain the washers and screws for reassembly. (If you are updating a UniPak 2B that was factory built, rather than a field conversion, it will not contain any washers.)
8. Pull the memory board straight up to unplug it from the card edge connector (as shown in figure 3).

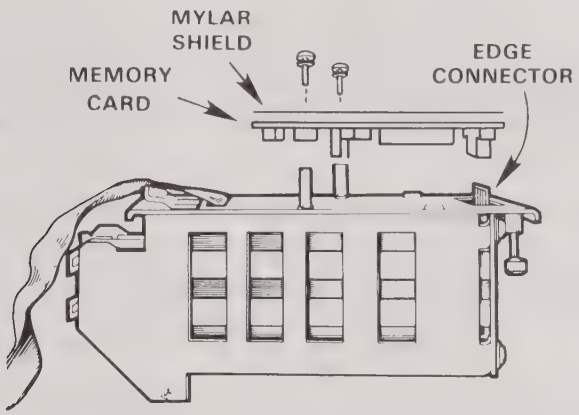


Figure 3. Memory Board Removal

9. Turn the 701-2126 memory board over so the component side faces up (figure 4) in preparation for firmware installation.

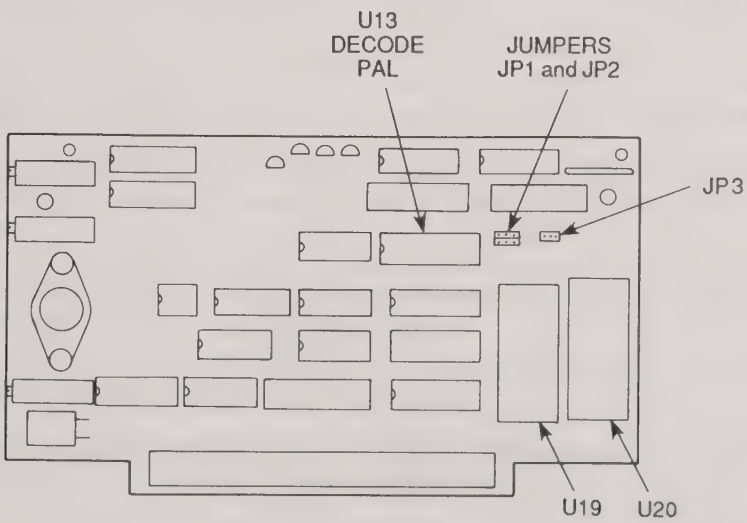


Figure 4. Update Component Location

Table 2. Jumper Configuration

Jumper	Position
JP1	Position B
JP2	Position A
JP3	Position B

Firmware Installation

The following steps describe how to install the firmware components of the update kit into your disassembled UniPak 2/2B. Follow the procedures in the order that they are presented here.

CAUTION

The software update kit EPROMs are static-sensitive. Perform the following procedures at a static-free work station to prevent static-related damage to the EPROM(s).

1. Remove EPROMs U19, U20 and decode PAL U13 (see figure 4) from the memory board using the IC extractor tool or the small slot-head screwdriver.
2. Refer to Table 2 for jumper configurations. If any jumpers are not in the correct locations, use the needle-nose pliers and soldering iron to change them to the correct location.

NOTE

Prior to installing the firmware, check the socket contacts to ensure that they are not damaged. If any socket contact is damaged, repair or replace that part before proceeding with the firmware installation.

3. Install the software update kit Decode PAL U13 in memory board socket U13. Refer to table 1 for software update kit firmware part numbers and their corresponding installation locations.

WARNING

When installing EPROM(s) be sure to bottom justify them in the socket (figure 5).

4. Install the software update kit EPROMs U19 and U20 in sockets U19 and U20, respectively. Refer to table 1 for software update kit component part numbers and their corresponding installation locations.

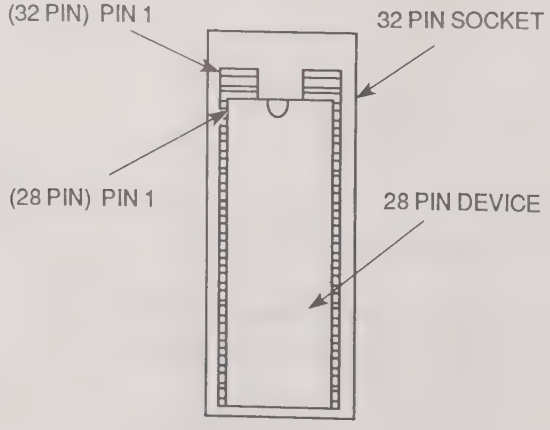


Figure 5. EPROM Installation Alignment

UniPak 2/2B Reassembly and Testing

Reassembly of the UniPak 2/2B is performed by reversing the disassembly procedures. Follow the steps listed below and refer to figures 1 through 3 on the previous pages.

1. Plug the memory board into its card cage edge connector (figure 3) until it is firmly seated.
2. Replace the armite or mylar shield, washers (if included) and two Phillips-head screws.
3. Reinsert the card cage into the top cover with the memory board facing into the top cover (figure 2). Tilt the card cage up and push gently forward to lock the top cover's flange between the card cage's top and bottom flanges (figure 1b). Then gently set the card cage back into the top cover.
4. Using the medium size slot-head screwdriver, tighten the captive fastener slot screws finger tight.
5. Perform a self-test on the UniPak 2/2B by installing it in a programmer and applying power.

   If the programmer fails to power up correctly, or the self-test message is not displayed, check to make sure that all of the software update kit installation procedures (and conversion kit installation procedures, if you are installing the conversion kit) were performed correctly. If the self-test fails again, contact your local Data I/O Service Center for assistance.
6. Verify the correct firmware configuration/version number by pressing SELECT E F START on the programmer's keyboard. Check the programmer display for the four-character configuration number and the version number. See the bottom of table 1 on the first page of this document for the correct configuration and version numbers.

   If the correct configuration and version numbers are not displayed, the firmware has not been installed correctly. Check to make sure that all installation procedures were performed correctly. Make sure that all PROMs are fully inserted into their sockets and are making proper contact at their connections. Install the UniPak 2/2B in a programmer and again press SELECT E F START. If the configuration/version number displayed still does not match that listed in table 1, contact your local Data I/O Service Center for assistance.

   If the configuration/version number listed in table 1 is displayed, then the update kit firmware installation is complete.
7. Using an indelible ink pen, write the serial number of your unit on the serial number label provided. Affix the enclosed label over the existing label on the back side of the front panel. The UniPak 2 label location is shown in figure 1b. The UniPak 2B label is located on the vertical surface facing the indicated UniPak 2 label location.

   If you are installing a UniPak 2 to 2B conversion kit, complete the conversion kit installation at this time, starting with the subsection Testing the UniPak 2B.

   If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete that section before doing the acceptance test.

   If you are updating a UniPak 2B, an acceptance test was included in the user note. If you want to re-accept the UniPak 2B after updating it, perform the acceptance test procedures as directed in the enclosed acceptance test manual.

UNIPAK 2/2B™

Software Update Kit

985-0002-013 November 1988

Data I/O has made every attempt to ensure that the information in this document is accurate and complete. However, Data I/O assumes no liability for errors, or for any damages that result from use of this document or the equipment that it accompanies.

Data I/O reserves the right to make changes to this document without notice at any time.

ORDERING INFORMATION

When ordering this manual, use Part Number 985-0002-013.
Applies to: Engineering part numbers 953-0002-017 and up
and 953-0017-011 and up.

UniPak 2™ and UniPak 2B™ are trademarks of Data I/O Corporation.

Copyright Data I/O Corporation, 1988. All rights reserved.

INTRODUCTION

WARNING

The procedures described in this document are intended for use only by personnel qualified to service electronic equipment. Do not attempt to perform these procedures unless you are qualified to do so.

This manual provides the software update instructions necessary for updating either the UniPak 2 or the UniPak 2B. The parts included in each of the update kits are listed in Table 1 below:

Table 1. Software Update Kit Parts

Type of Kit	Description	Quantity	Data I/O Part No.	Installation Location
UniPak 2	EPROM	1	324-0059-041	U19
	EPROM	1	324-0059-042	U20
	Decode PAL	1	324-1760-007	U13
	Label	1	–	
	UniPak 2 Operator's Manual	1	981-0001	
	UniPak 2 User Notes	1	984-0001	
UniPak 2B	EPROM	1	324-0059-041	U19
	EPROM	1	324-0059-042	U20
	Decode PAL	1	324-1760-007	U13
	Label	1	–	
	UniPak 2B Device List	1	984-0179	
	UniPak 2B Acceptance Test	1	984-0179	
	UniPak 2B User Notes	1	984-0179	

Firmware Configuration/Version Number: FEC2 VER 17.0

CAUTION

The software update kit EPROMs are static-sensitive. Observe standard handling precautions, such as performing the update kit procedures at an anti-static workstation or wearing a grounded wrist-strap, otherwise, damage to the EPROM(s) may result.

UNIPAK 2/2B SOFTWARE UPDATE KIT INSTALLATION

The following paragraphs describe how to install the software update kit. You will need the following tools for installation of the kit:

- One Phillips-head screwdriver (medium size, #1 or #2)
- One slot-head screwdriver (medium size)
- One pair of needle-nose pliers
- IC extractor tool, or small slot-head screwdriver
- Soldering Iron

For the Software Update Kit to work, your UniPak 2/2B must have a 701-2126 Memory Board. To determine if your pak has the correct memory board, perform the following steps:

1. Install the UniPak 2/2B in the programmer and turn the programmer on.

2. Press **SELECT**. Type **E F** on the programmer keyboard and then press **START**.

If the display does not show version 13.0 or greater, the new Memory Board must be installed. A hardware update kit (951-0045) is required.

NOTE

If you are installing only the Software Update Kit, go directly to the UniPak 2/2B Disassembly section on the following page.

If you are not installing the Conversion Kit, but are installing the Hardware Update Kit, go to UniPak 2/2B Disassembly section of the Hardware Update Kit manual. Complete the instructions and when instructed to do so, go to the Firmware Installation section in this manual.

If you are installing a UniPak 2 to 2B Conversion Kit and/or the Hardware Update Kit, begin installing the conversion kit first. When the conversion kit instructions direct you to install the software and/or hardware update kit:

1. a. *If you are installing a new memory board, go to step 6 of the Hardware Update Kit manual, complete the instructions and then go directly to the Firmware Installation section in this manual.*

   b. *If you are not installing a new memory board, go directly to the Firmware Installation section in this manual.*

2. *Complete the software update kit installation as directed in the Firmware Installation section of this manual.*

3. *Proceed to the Testing the UniPak 2B section of the converstion kit manual and*

   a. *if the conversion kit was installed, complete the conversion kit installation.*

   b. *If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete the installation there.*

UniPak 2/2B Disassembly

To disassemble the UniPak 2/2B for installation of the updated firmware, follow the procedures listed below.

1. Remove the UniPak 2/2B from the programmer, if it is installed.
2. Set the UniPak 2/2B face down on the flat surface of a static-free workstation.
3. Using the medium size slot-head screwdriver, unscrew the captive fasteners (figure 1, step 1) until they hang loosely; the fasteners will not separate from their standoffs.
4. Lift the card cage up slightly, then pull out (as shown in figure 1, step 2) to unlock the flanges.

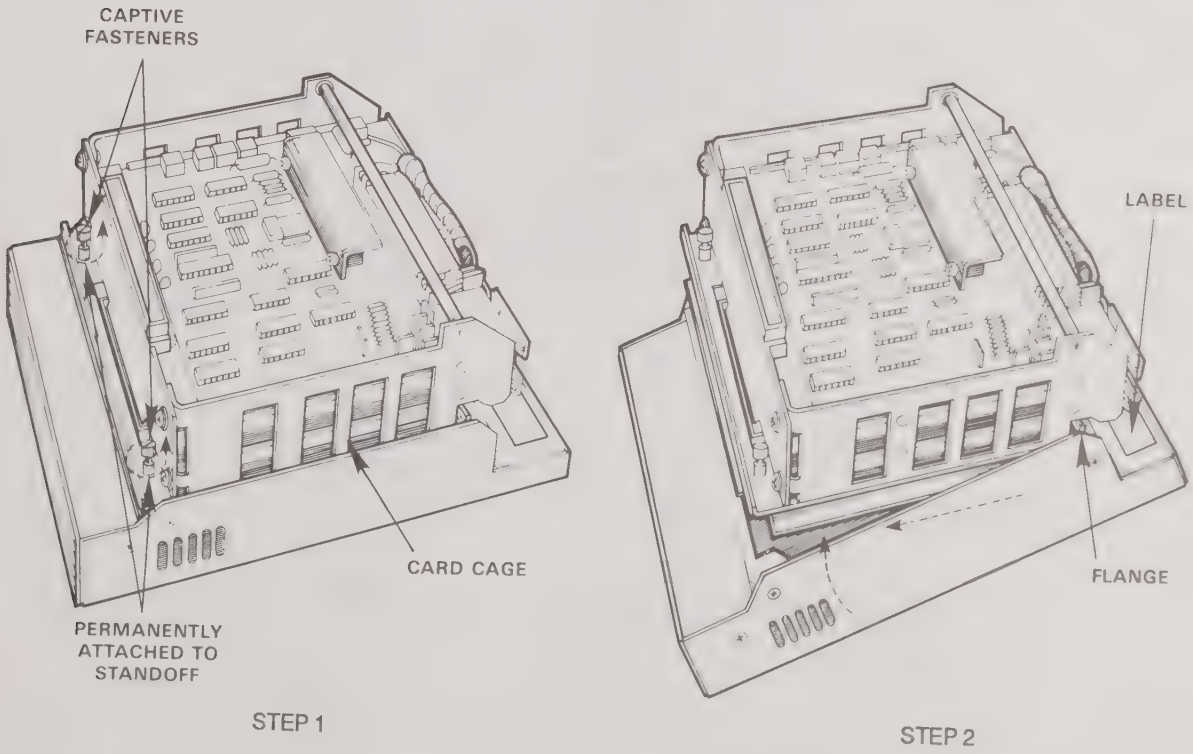


Figure 1. UniPak 2/2B Disassembly
(UniPak 2 shown)

5. Lift the card cage up and out of its top cover until you can see the socketboard interconnect cable (see figure 2). Do not detach the socketboard interconnect cable.
6. Turn the card cage over and set it on the flat surface next to the top cover. This step exposes the armite or mylar shield which covers the memory board.

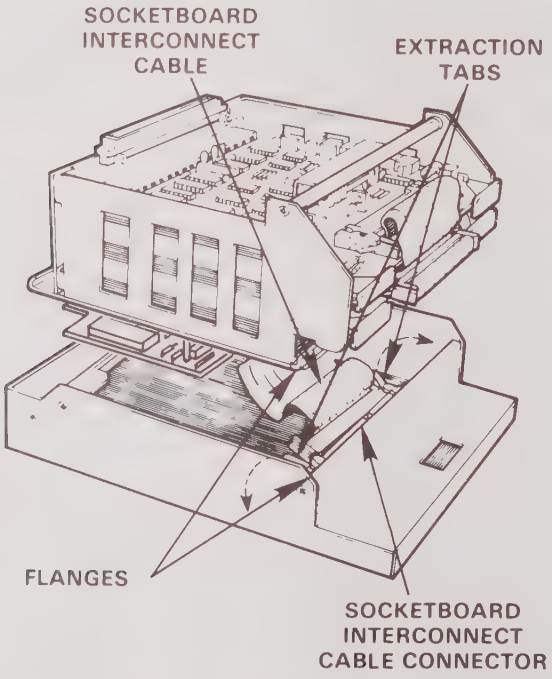


Figure 2. Socketboard Interconnect Cable

7. Remove the two Phillips-head screws and armite or mylar shield from the memory board (see figure 3). Retain the washers and screws for reassembly. (If you are updating a UniPak 2B that was factory built, rather than a field conversion, it will not contain any washers.)
8. Pull the memory board straight up to unplug it from the card edge connector (as shown in figure 3).

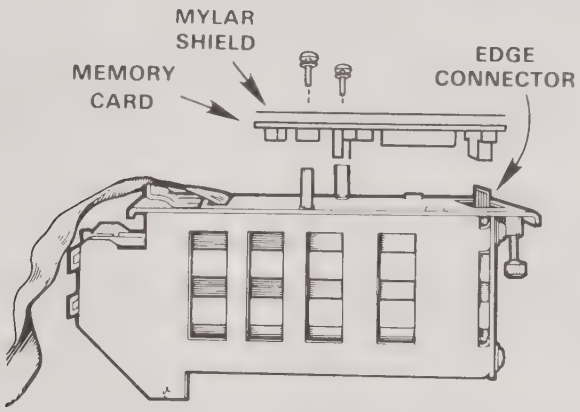


Figure 3. Memory Board Removal

9. Turn the 701-2126 memory board over so the component side faces up (figure 4) in preparation for firmware installation.

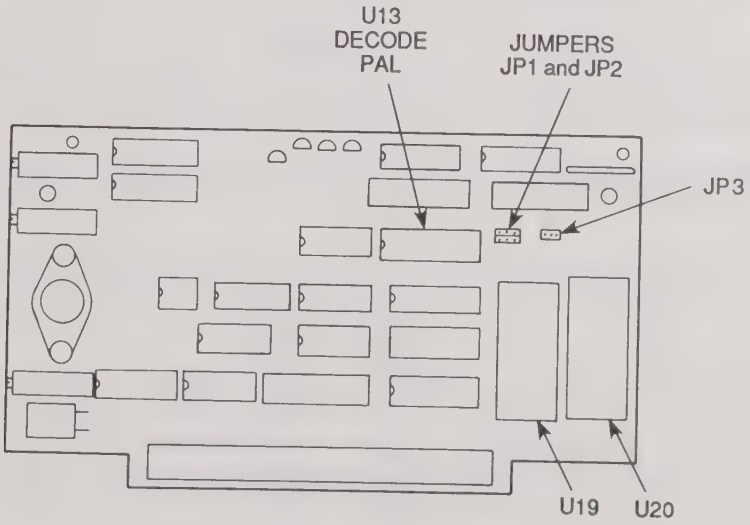


Figure 4. Update Component Location

Table 2. Jumper Configuration

Jumper	Position
JP1	Position B
JP2	Position A
JP3	Position B

Firmware Installation

The following steps describe how to install the firmware components of the update kit into your disassembled UniPak 2/2B. Follow the procedures in the order that they are presented here.

CAUTION

The software update kit EPROMs are static-sensitive. Perform the following procedures at a static-free work station to prevent static-related damage to the EPROM(s).

1. Remove EPROMs U19, U20 and decode PAL U13 (see figure 4) from the memory board using the IC extractor tool or the small slot-head screwdriver.
2. Refer to Table 2 for jumper configurations. If any jumpers are not in the correct locations, use the needle-nose pliers and soldering iron to change them to the correct location.

NOTE

Prior to installing the firmware, check the socket contacts to ensure that they are not damaged. If any socket contact is damaged, repair or replace that part before proceeding with the firmware installation.

3. Install the software update kit Decode PAL U13 in memory board socket U13. Refer to table 1 for software update kit firmware part numbers and their corresponding installation locations.

WARNING

When installing EPROM(s) be sure to bottom justify them in the socket (figure 5).

4. Install the software update kit EPROMs U19 and U20 in sockets U19 and U20, respectively. Refer to table 1 for software update kit component part numbers and their corresponding installation locations.

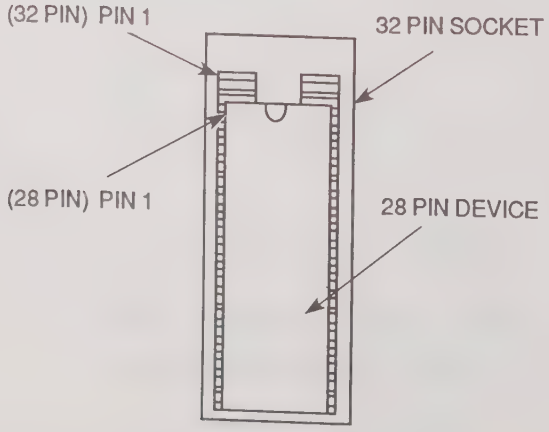


Figure 5. EPROM Installation Alignment

UniPak 2/2B Reassembly and Testing

Reassembly of the UniPak 2/2B is performed by reversing the disassembly procedures. Follow the steps listed below and refer to figures 1 through 3 on the previous pages.

1. Plug the memory board into its card cage edge connector (figure 3) until it is firmly seated.
2. Replace the armite or mylar shield, washers (if included) and two Phillips-head screws.
3. Reinsert the card cage into the top cover with the memory board facing into the top cover (figure 2). Tilt the card cage up and push gently forward to lock the top cover's flange between the card cage's top and bottom flanges (figure 1b). Then gently set the card cage back into the top cover.
4. Using the medium size slot-head screwdriver, tighten the captive fastener slot screws finger tight.
5. Perform a self-test on the UniPak 2/2B by installing it in a programmer and applying power.

   If the programmer fails to power up correctly, or the self-test message is not displayed, check to make sure that all of the software update kit installation procedures (and conversion kit installation procedures, if you are installing the conversion kit) were performed correctly. If the self-test fails again, contact your local Data I/O Service Center for assistance.
6. Verify the correct firmware configuration/version number by pressing SELECT E F START on the programmer's keyboard. Check the programmer display for the four-character configuration number and the version number. See the bottom of table 1 on the first page of this document for the correct configuration and version numbers.

   If the correct configuration and version numbers are not displayed, the firmware has not been installed correctly. Check to make sure that all installation procedures were performed correctly. Make sure that all PROMs are fully inserted into their sockets and are making proper contact at their connections. Install the UniPak 2/2B in a programmer and again press SELECT E F START. If the configuration/version number displayed still does not match that listed in table 1, contact your local Data I/O Service Center for assistance.

   If the configuration/version number listed in table 1 is displayed, then the update kit firmware installation is complete.
7. Using an indelible ink pen, write the serial number of your unit on the serial number label provided. Affix the enclosed label over the existing label on the back side of the front panel. The UniPak 2 label location is shown in figure 1b. The UniPak 2B label is located on the vertical surface facing the indicated UniPak 2 label location.

   If you are installing a UniPak 2 to 2B conversion kit, complete the conversion kit installation at this time, starting with the subsection Testing the UniPak 2B.

   If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete that section before doing the acceptance test.

   If you are updating a UniPak 2B, an acceptance test was included in the user note. If you want to re-accept the UniPak 2B after updating it, perform the acceptance test procedures as directed in the enclosed acceptance test manual.

UNIPAK 2/2B™

Software Update Kit

985-0002-012 *July 1988*

Installed
8-19-88
a Taylor

Data I/O has made every attempt to ensure that the information in this document is accurate and complete. However, Data I/O assumes no liability for errors, or for any damages that result from use of this document or the equipment that it accompanies.

Data I/O reserves the right to make changes to this document without notice at any time.

ORDERING INFORMATION

When ordering this manual, use Part Number 985-0002-012.
Applies to: Engineering part numbers 953-0002-017 and up
and 953-0017-011 and up.

UniPak 2™ and UniPak 2B™ are trademarks of Data I/O Corporation.

Copyright Data I/O Corporation, 1988. All rights reserved.

INTRODUCTION

WARNING

The procedures described in this document are intended for use only by personnel qualified to service electronic equipment. Do not attempt to perform these procedures unless you are qualified to do so.

This manual provides the software update instructions necessary for updating either the UniPak 2 or the UniPak 2B. The parts included in each of the update kits are listed in Table 1 below:

Table 1. Software Update Kit Parts

Type of Kit	Description	Quantity	Data I/O Part No.	Installation Location
UniPak 2	EPROM	1	324-0059-039	U19
	EPROM	1	324-0059-040	U20
	Decode PAL	1	324-1760-006	U13
	Label	1	–	
	UniPak 2 Operator's Manual	1	981-0001	
	UniPak 2 User Notes	1	984-0001	
UniPak 2B	EPROM	1	324-0059-039	U19
	EPROM	1	324-0059-040	U20
	Decode PAL	1	324-1760-006	U13
	Label	1	–	
	UniPak 2B Device List	1	984-0179	
	UniPak 2B Acceptance Test	1	984-0179	
	UniPak 2B User Notes	1	984-0179	

Firmware Configuration/Version Number: A62C VER 16.0

CAUTION

The software update kit EPROMs are static-sensitive. Observe standard handling precautions, such as performing the update kit procedures at an anti-static workstation or wearing a grounded wrist-strap, otherwise, damage to the EPROM(s) may result.

UNIPAK 2/2B SOFTWARE UPDATE KIT INSTALLATION

The following paragraphs describe how to install the software update kit. You will need the following tools for installation of the kit:

- One Phillips-head screwdriver (medium size, #1 or #2)
- One slot-head screwdriver (medium size)
- One pair of needle-nose pliers
- IC extractor tool, or small slot-head screwdriver
- Soldering Iron

For the Software Update Kit to work, your UniPak 2/2B must have a 701-2126 Memory Board. To determine if your pak has the correct memory board, perform the following steps:

1. Install the UniPak 2/2B in the programmer and turn the programmer on.

2. Press **SELECT**. Type **E F** on the programmer keyboard and then press **START**.

If the display does not show version 13.0 or greater, the new Memory Board must be installed. A hardware update kit (951-0045) is required.

NOTE

If you are installing only the Software Update Kit, go directly to the UniPak 2/2B Disassembly section on the following page.

If you are not installing the Conversion Kit, but are installing the Hardware Update Kit, go to UniPak 2/2B Disassembly section of the Hardware Update Kit manual. Complete the instructions and when instructed to do so, go to the Firmware Installation section in this manual.

If you are installing a UniPak 2 to 2B Conversion Kit and/or the Hardware Update Kit, begin installing the conversion kit first. When the conversion kit instructions direct you to install the software and/or hardware update kit:

1. a. *If you are installing a new memory board, go to step 6 of the Hardware Update Kit manual, complete the instructions and then go directly to the Firmware Installation section in this manual.*

   b. *If you are not installing a new memory board, go directly to the Firmware Installation section in this manual.*

2. *Complete the software update kit installation as directed in the Firmware Installation section of this manual.*

3. *Proceed to the Testing the UniPak 2B section of the converstion kit manual and*

   a. *if the conversion kit was installed, complete the conversion kit installation.*

   b. *If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete the installation there.*

UniPak 2/2B Disassembly

To disassemble the UniPak 2/2B for installation of the updated firmware, follow the procedures listed below.

1. Remove the UniPak 2/2B from the programmer, if it is installed.
2. Set the UniPak 2/2B face down on the flat surface of a static-free workstation.
3. Using the medium size slot-head screwdriver, unscrew the captive fasteners (figure 1, step 1) until they hang loosely; the fasteners will not separate from their standoffs.
4. Lift the card cage up slightly, then pull out (as shown in figure 1, step 2) to unlock the flanges.

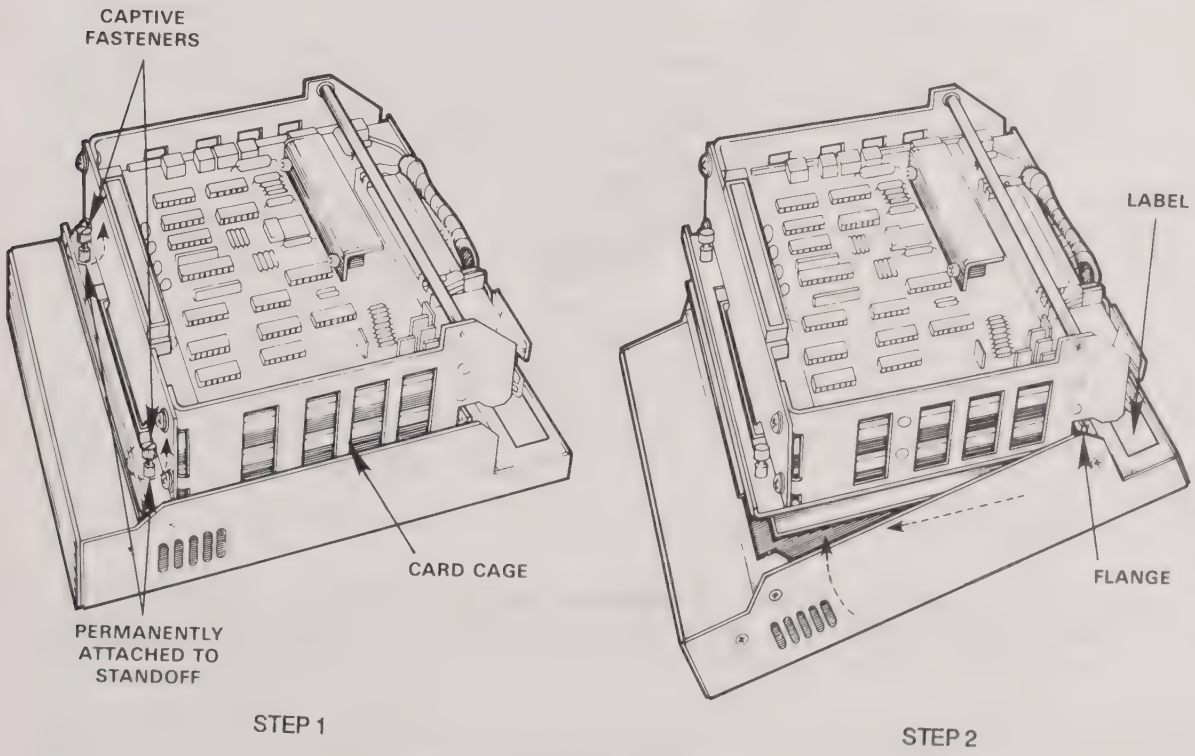


Figure 1. UniPak 2/2B Disassembly
(UniPak 2 shown)

5. Lift the card cage up and out of its top cover until you can see the socketboard interconnect cable (see figure 2). Do not detach the socketboard interconnect cable.
6. Turn the card cage over and set it on the flat surface next to the top cover. This step exposes the armite or mylar shield which covers the memory board.

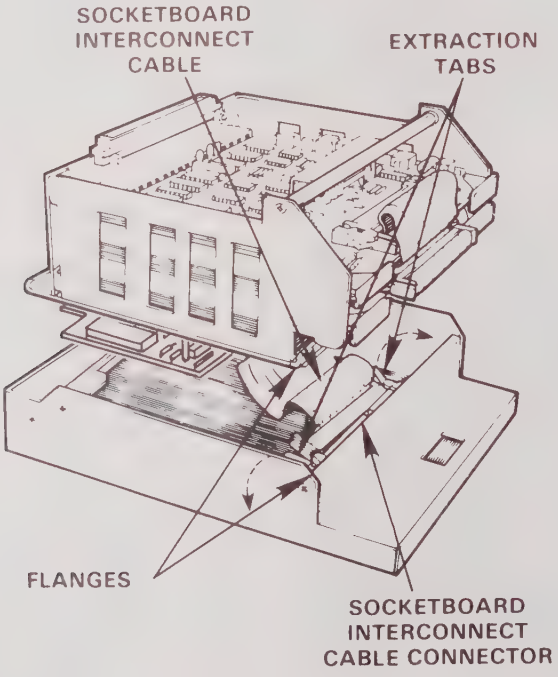


Figure 2. Socketboard Interconnect Cable

UniPak 2/2B Reassembly and Testing

Reassembly of the UniPak 2/2B is performed by reversing the disassembly procedures. Follow the steps listed below and refer to figures 1 through 3 on the previous pages.

1. Plug the memory board into its card cage edge connector (figure 3) until it is firmly seated.
2. Replace the armite or mylar shield, washers (if included) and two Phillips-head screws.
3. Reinsert the card cage into the top cover with the memory board facing into the top cover (figure 2). Tilt the card cage up and push gently forward to lock the top cover's flange between the card cage's top and bottom flanges (figure 1b). Then gently set the card cage back into the top cover.
4. Using the medium size slot-head screwdriver, tighten the captive fastener slot screws finger tight.
5. Perform a self-test on the UniPak 2/2B by installing it in a programmer and applying power.

   If the programmer fails to power up correctly, or the self-test message is not displayed, check to make sure that all of the software update kit installation procedures (and conversion kit installation procedures, if you are installing the conversion kit) were performed correctly. If the self-test fails again, contact your local Data I/O Service Center for assistance.
6. Verify the correct firmware configuration/version number by pressing SELECT E F START on the programmer's keyboard. Check the programmer display for the four-character configuration number and the version number. See the bottom of table 1 on the first page of this document for the correct configuration and version numbers.

   If the correct configuration and version numbers are not displayed, the firmware has not been installed correctly. Check to make sure that all installation procedures were performed correctly. Make sure that all PROMs are fully inserted into their sockets and are making proper contact at their connections. Install the UniPak 2/2B in a programmer and again press SELECT E F START. If the configuration/version number displayed still does not match that listed in table 1, contact your local Data I/O Service Center for assistance.

   If the configuration/version number listed in table 1 is displayed, then the update kit firmware installation is complete.
7. Using an indelible ink pen, write the serial number of your unit on the serial number label provided. Affix the enclosed label over the existing label on the back side of the front panel. The UniPak 2 label location is shown in figure 1b. The UniPak 2B label is located on the vertical surface facing the indicated UniPak 2 label location.

   If you are installing a UniPak 2 to 2B conversion kit, complete the conversion kit installation at this time, starting with the subsection Testing the UniPak 2B.

   If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete that section before doing the acceptance test.

   If you are updating a UniPak 2B, an acceptance test was included in the user note. If you want to re-accept the UniPak 2B after updating it, perform the acceptance test procedures as directed in the enclosed acceptance test manual.

7. Remove the two Phillips-head screws and armite or mylar shield from the memory board (see figure 3). Retain the washers and screws for reassembly. (If you are updating a UniPak 2B that was factory built, rather than a field conversion, it will not contain any washers.)
8. Pull the memory board straight up to unplug it from the card edge connector (as shown in figure 3).

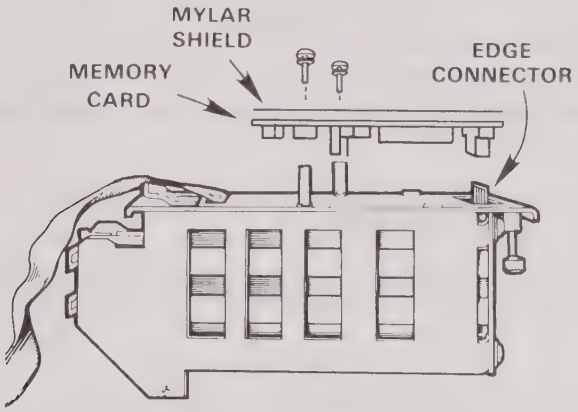


Figure 3. Memory Board Removal

9. Turn the 701-2126 memory board over so the component side faces up (figure 4) in preparation for firmware installation.

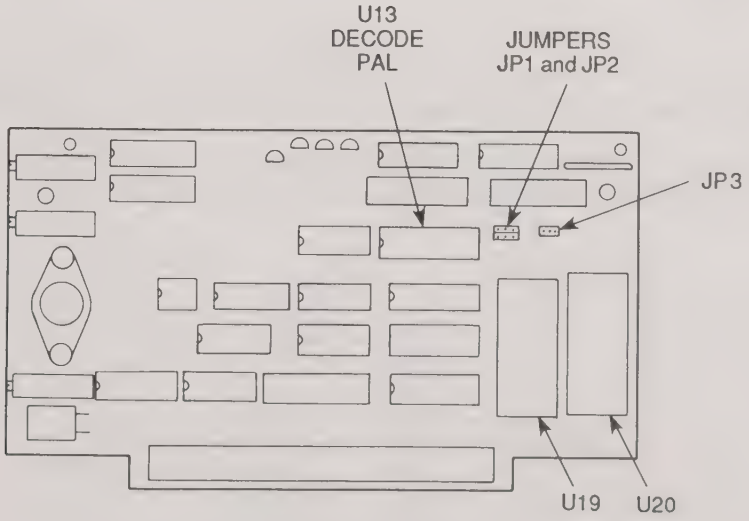


Figure 4. Update Component Location

Table 2. Jumper Configuration

Jumper	Position
JP1	Position B
JP2	Position A
JP3	Position A

Firmware Installation

The following steps describe how to install the firmware components of the update kit into your disassembled UniPak 2/2B. Follow the procedures in the order that they are presented here.

CAUTION

The software update kit EPROMs are static-sensitive. Perform the following procedures at a static-free work station to prevent static-related damage to the EPROM(s).

1. Remove EPROMs U19, U20 and decode PAL U13 (see figure 4) from the memory board using the IC extractor tool or the small slot-head screwdriver.
2. Refer to Table 2 for jumper configurations. If any jumpers are not in the correct locations, use the needle-nose pliers and soldering iron to change them to the correct location.

NOTE

Prior to installing the firmware, check the socket contacts to ensure that they are not damaged. If any socket contact is damaged, repair or replace that part before proceeding with the firmware installation.

3. Install the software update kit Decode PAL U13 in memory board socket U13. Refer to table 1 for software update kit firmware part numbers and their corresponding installation locations.

WARNING

When installing EPROM(s) be sure to bottom justify them in the socket (figure 5).

4. Install the software update kit EPROMs U19 and U20 in sockets U19 and U20, respectively. Refer to table 1 for software update kit component part numbers and their corresponding installation locations.

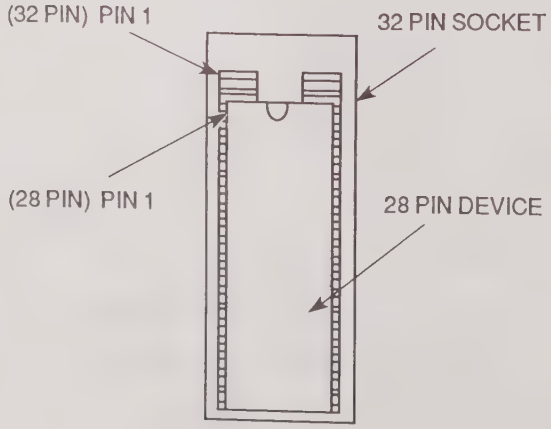


Figure 5. EPROM Installation Alignment

UNIPAK 2/2B™

Software Update Kit

985-0002-011 *April 88*

Data I/O has made every attempt to ensure that the information in this document is accurate and complete. However, Data I/O assumes no liability for errors, or for any damages that result from use of this document or the equipment that it accompanies.

Data I/O reserves the right to make changes to this document without notice at any time.

ORDERING INFORMATION

When ordering this manual, use Part Number 985-0002-011.
Applies to: Engineering part numbers 953-0002-016 and up
and 953-0017-010 and up.

UniPak 2™ and UniPak 2B™ are trademarks of Data I/O Corporation.

Copyright Data I/O Corporation, 1988. All rights reserved.

INTRODUCTION

WARNING

The procedures described in this document are intended for use only by personnel qualified to service electronic equipment. Do not attempt to perform these procedures unless you are qualified to do so.

This manual provides the software update instructions necessary for updating either the UniPak 2 or the UniPak 2B. The parts included in each of the update kits are listed in table 1 below:

Table 1. Software Update Kit Parts

Type of Kit	Description	Quantity	Data I/O Part No.	Installation Location
UniPak 2	EPROM	1	324-0059-037	U19
	EPROM	1	324-0059-038	U20
	Decode PAL	1	324-1760-005	U13
	Label	1	–	
	UniPak 2 Operator's Manual	1	981-0001	
	UniPak 2 User Notes	1	984-0001	
UniPak 2B	EPROM	1	324-0059-037	U19
	EPROM	1	324-0059-038	U20
	Decode PAL	1	324-1760-005	U13
	Label	1	–	
	UniPak 2B Device List	1	984-0179	
	UniPak 2B Acceptance Test	1	984-0179	
	UniPak 2B User Notes	1	984-0179	

Firmware Configuration/Version Number: 3443 VER 15.0

CAUTION

The software update kit EPROMs are static-sensitive. Observe standard handling precautions, such as performing the update kit procedures at an anti-static workstation or wearing a grounded wrist-strap, otherwise, damage to the EPROM(s) may result.

UniPak 2/2B Software Update Kit Installation

The following paragraphs describe how to install the software update kit. You will need the following tools for installation of the kit:

- One Phillips-head screwdriver (medium size, #1 or #2)
- One slot-head screwdriver (medium size)
- One pair of needle-nose pliers
- IC extractor tool, or small slot-head screwdriver
- Soldering Iron

For the Software Update Kit to work, your UniPak 2/2B must have a 701-2126 Memory Board. To determine if your pak has the correct memory board, perform the following steps:

1. Install the UniPak 2/2B in the programmer and turn the programmer on.

2. Press **SELECT**. Type **E F** on the programmer keyboard and then press **START**.

If the display does not show version 13.0 or greater, the new Memory Board must be installed. A hardware update kit (951-0045) is required.

NOTE

If you are installing only the Software Update Kit, go directly to the UniPak 2/2B Disassembly section on the following page.

If you are not installing the Conversion Kit, but are installing the Hardware Update Kit, go to UniPak 2/2B Disassembly section of the Hardware Update Kit manual. Complete the instructions and when instructed to do so, go to the Firmware Installation section in this manual.

If you are installing a UniPak 2 to 2B Conversion Kit and/or the Hardware Update Kit, begin installing the conversion kit first. When the conversion kit instructions direct you to install the software and/or hardware update kit:

1. a. *If you are installing a new memory board, go to step 6 of the Hardware Update Kit manual, complete the instructions and then go directly to the Firmware Installation section in this manual.*

   b. *If you are not installing a new memory board, go directly to the Firmware Installation section in this manual.*

2. *Complete the software update kit installation as directed in the Firmware Installation section of this manual.*

3. *Proceed to the Testing the UniPak 2B section of the converstion kit manual and*

   a. *if the conversion kit was installed, complete the conversion kit installation.*

   b. *If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete the installation there.*

UniPak 2/2B Disassembly

To disassemble the UniPak 2/2B for installation of the updated firmware, follow the procedures listed below.

1. Remove the UniPak 2/2B from the programmer, if it is installed.
2. Set the UniPak 2/2B face down on the flat surface of a static-free workstation.
3. Using the medium size slot-head screwdriver, unscrew the captive fasteners (figure 1, step 1) until they hang loosely; the fasteners will not separate from their standoffs.
4. Lift the card cage up slightly, then pull out (as shown in figure 1, step 2) to unlock the flanges.

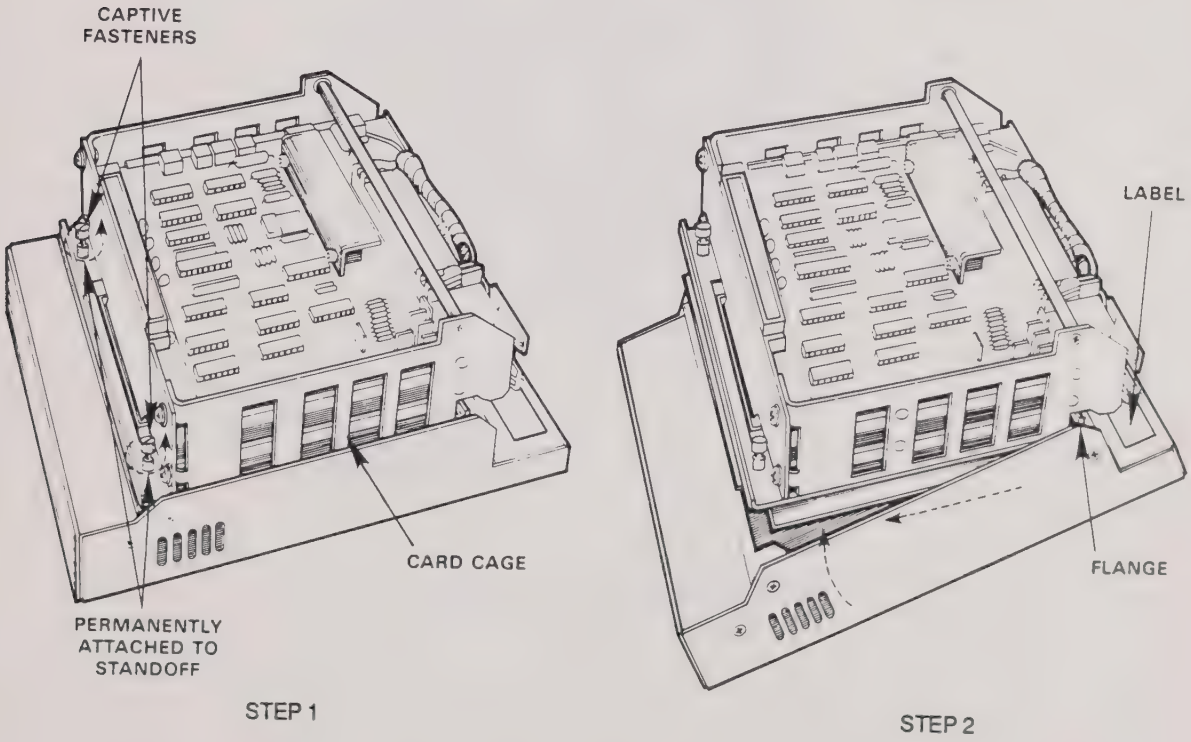


Figure 1. UniPak 2/2B Disassembly (UniPak 2 shown)

5. Lift the card cage up and out of its top cover until you can see the socketboard interconnect cable (see figure 2). Do not detach the socketboard interconnect cable.

6. Turn the card cage over and set it on the flat surface next to the top cover. This step exposes the armite or mylar shield which covers the memory board.

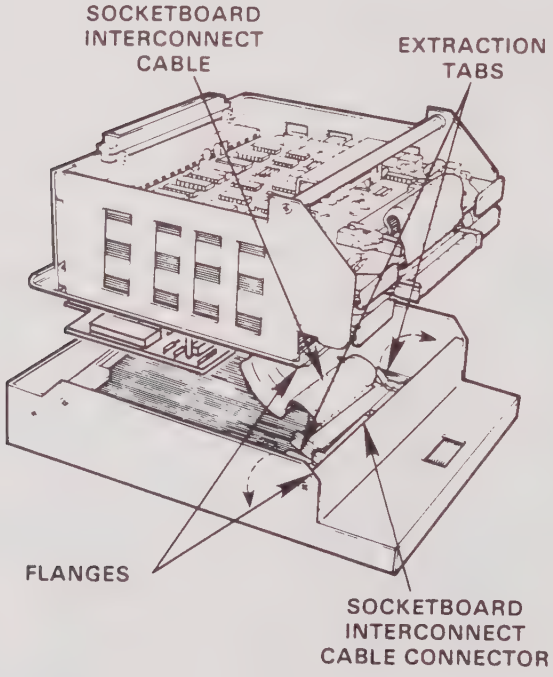


Figure 2. Socketboard Interconnect Cable

7. Remove the two Phillips-head screws and armite or mylar shield from the memory board (see figure 3). Retain the washers and screws for reassembly. (If you are updating a UniPak 2B that was factory built, rather than a field conversion, it will not contain any washers.)

8. Pull the memory board straight up to unplug it from the card edge connector (as shown in figure 3).

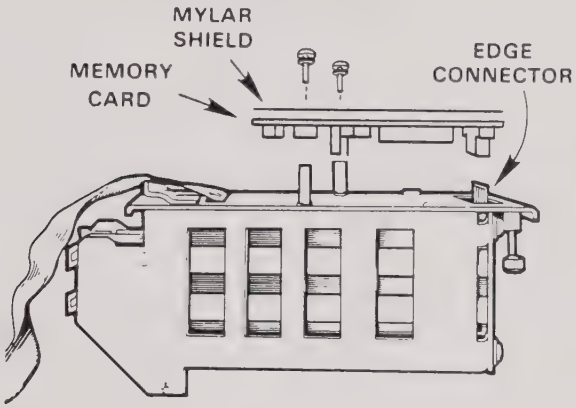


Figure 3. Memory Board Removal

9. Turn the 701-2126 memory board over so the component side faces up (figure 4) in preparation for firmware installation.

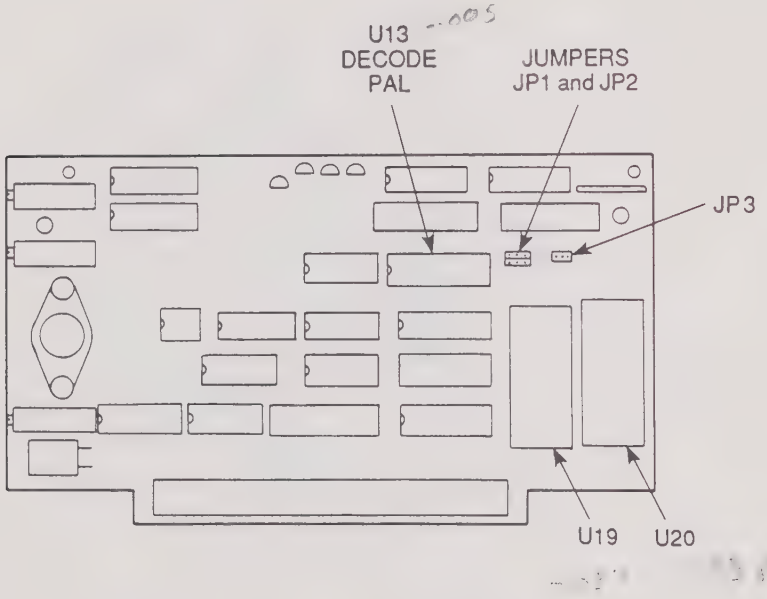


Figure 4. Update Component Location

Table 2. Jumper Configuration

Jumper	Position
JP1	Position A
JP2	Position A
JP3	Position B

Firmware Installation

The following steps describe how to install the firmware components of the update kit into your disassembled UniPak 2/2B. Follow the procedures in the order that they are presented here.

CAUTION

The software update kit EPROMs are static-sensitive. Perform the following procedures at a static-free work station to prevent static-related damage to the EPROM(s).

1. Remove EPROMs U19, U20 and decode PAL U13 (see figure 4) from the memory board using the IC extractor tool or the small slot-head screwdriver.

2. Refer to Table 2 for jumper configurations. If any jumpers are not in the correct locations, use the needle-nose pliers and soldering iron to change them to the correct location.

NOTE

Prior to installing the firmware, check the socket contacts to ensure that they are not damaged. If any socket contact is damaged, repair or replace that part before proceeding with the firmware installation.

3. Install the software update kit Decode PAL U13 in memory board socket U13. Refer to table 1 for software update kit firmware part numbers and their corresponding installation locations.

WARNING

When installing EPROM(s) be sure to bottom justify them in the socket (figure 5).

4. Install the software update kit EPROMs U19 and U20 in sockets U19 and U20, respectively. Refer to table 1 for software update kit component part numbers and their corresponding installation locations.

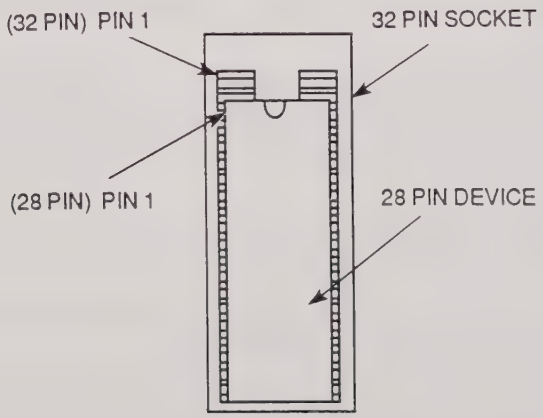


Figure 5. EPROM Installation Alignment

UniPak 2/2B Reassembly and Testing

Reassembly of the UniPak 2/2B is performed by reversing the disassembly procedures. Follow the steps listed below and refer to figures 1 through 3 on the previous pages.

1. Plug the memory board into its card cage edge connector (figure 3) until it is firmly seated.

2. Replace the armite or mylar shield, washers (if included) and two Phillips-head screws.

3. Reinsert the card cage into the top cover with the memory board facing into the top cover (figure 2). Tilt the card cage up and push gently forward to lock the top cover's flange between the card cage's top and bottom flanges (figure 1b). Then gently set the card cage back into the top cover.

4. Using the medium size slot-head screwdriver, tighten the captive fastener slot screws finger tight.

5. Perform a self-test on the UniPak 2/2B by installing it in a programmer and applying power.

   If the programmer fails to power up correctly, or the self-test message is not displayed, check to make sure that all of the software update kit installation procedures (and conversion kit installation procedures, if you are installing the conversion kit) were performed correctly. If the self-test fails again, contact your local Data I/O Service Center for assistance.

6. Verify the correct firmware configuration/version number by pressing `SELECT E F START` on the programmer's keyboard. Check the programmer display for the four-character configuration number and the version number. See the bottom of table 1 on the first page of this document for the correct configuration and version numbers.

   If the correct configuration and version numbers are not displayed, the firmware has not been installed correctly. Check to make sure that all installation procedures were performed correctly. Make sure that all PROMs are fully inserted into their sockets and are making proper contact at their connections. Install the UniPak 2/2B in a programmer and again press `SELECT E F START`. If the configuration/version number displayed still does not match that listed in table 1, contact your local Data I/O Service Center for assistance.

   If the configuration/version number listed in table 1 is displayed, then the update kit firmware installation is complete.

7. Using an indelible ink pen, write the serial number of your unit on the serial number label provided. Affix the enclosed label over the existing label on the back side of the front panel. The UniPak 2 label location is shown in figure 1b. The UniPak 2B label is located on the vertical surface facing the indicated UniPak 2 label location.

   If you are installing a UniPak 2 to 2B conversion kit, complete the conversion kit installation at this time, starting with the subsection Testing the UniPak 2B.

   If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete that section before doing the acceptance test.

   If you are updating a UniPak 2B, an acceptance test was included in the user note. If you want to re-accept the UniPak 2B after updating it, perform the acceptance test procedures as directed in the enclosed acceptance test manual.

UNIPAK 2/2B™

Software Update Kit

985-0002-009 NOVEMBER 87

12-17-87

Data I/O has made every attempt to ensure that the information in this document is accurate and complete. However, Data I/O assumes no liability for errors, or for any damages that result from use of this document or the equipment that it accompanies.

Data I/O reserves the right to make changes to this document without notice at any time.

ORDERING INFORMATION

When ordering this manual, use Part Number 985-0002-009.
Applies to: Engineering part numbers 953-0002-015 and up
and 953-0017-009 and up.

UniPak 2™ and UniPak 2B™ are trademarks of Data I/O Corporation.

Copyright Data I/O Corporation, 1987. All rights reserved.

INTRODUCTION

WARNING

The procedures described in this document are intended for use only by personnel qualified to service electronic equipment. Do not attempt to perform these procedures unless you are qualified to do so.

This manual provides the software update instructions necessary for updating either the UniPak 2 or the UniPak 2B. The parts included in each of the update kits are listed in table 1 below:

Table 1. Software Update Kit Parts

Type of Kit	Description	Quantity	Data I/O Part No.	Installation Location
UniPak 2	EPROM	1	324-0059-033	U19
	EPROM	1	324-0059-034	U20
	Decode PAL	1	324-1760-004	U13
	Label	1	–	
	UniPak 2 Operator's Manual	1	981-0001	
	UniPak 2 User Notes	1	984-0001	
UniPak 2B	EPROM	1	324-0059-033	U19
	EPROM	1	324-0059-034	U20
	Decode PAL	1	324-1760-004	U13
	Label	1	–	
	UniPak 2B Device List	1	984-0179	
	UniPak 2B Acceptance Test	1	984-0179	
	UniPak 2B User Notes	1	984-0179	

Firmware Configuration/Version Number: DE72 VER 14.0

CAUTION

The software update kit EPROMs are static-sensitive. Observe standard handling precautions, such as performing the update kit procedures at an anti-static workstation or wearing a grounded wrist-strap, otherwise, damage to the EPROM(s) may result.

UniPak 2/2B Software Update Kit Installation

The following paragraphs describe how to install the software update kit. You will need the following tools for installation of the kit:

- One Phillips-head screwdriver (medium size, #1 or #2)
- One slot-head screwdriver (medium size)
- IC extractor tool, or small slot-head screwdriver

For the Software Update Kit to work, your UniPak 2/2B must have a 701-2126 Memory Board. To determine if your pak has the correct memory board, perform the following steps:

1. Install the UniPak 2/2B in the programmer and turn the programmer on.

2. Press **SELECT**. Type **E F** on the programmer keyboard and then press **START**.

If the display does not show version 13.0 or greater, the new Memory Board must be installed. A hardware update kit (951-0045) is required.

NOTE

If you are installing only the Software Update Kit, go directly to the UniPak 2/2B Disassembly section on the following page.

If you are not installing the Conversion Kit, but are installing the Hardware Update Kit, go to UniPak 2/2B Disassembly section of the Hardware Update Kit manual. Complete the instructions and when instructed to do so, go to the Firmware Installation section in this manual.

If you are installing a UniPak 2 to 2B Conversion Kit and/or the Hardware Update Kit, begin installing the conversion kit first. When the conversion kit instructions direct you to install the software and/or hardware update kit:

1. a. *If you are installing a new memory board, go to step 6 of the Hardware Update Kit manual, complete the instructions and then go directly to the Firmware Installation section in this manual.*

   b. *If you are not installing a new memory board, go directly to the Firmware Installation section in this manual.*

2. *Complete the software update kit installation as directed in the Firmware Installation section of this manual.*

3. *Proceed to the Testing the UniPak 2B section of the converstion kit manual and*

   a. *if the conversion kit was installed, complete the conversion kit installation.*

   b. *If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete the installation there.*

UniPak 2/2B Disassembly

To disassemble the UniPak 2/2B for installation of the updated firmware, follow the procedures listed below.

1. Remove the UniPak 2/2B from the programmer, if it is installed.
2. Set the UniPak 2/2B face down on the flat surface of a static-free workstation.
3. Using the medium size slot-head screwdriver, unscrew the captive fasteners (figure 1, step 1) until they hang loosely; the fasteners will not separate from their standoffs.
4. Lift the card cage up slightly, then pull out (as shown in figure 1, step 2) to unlock the flanges.

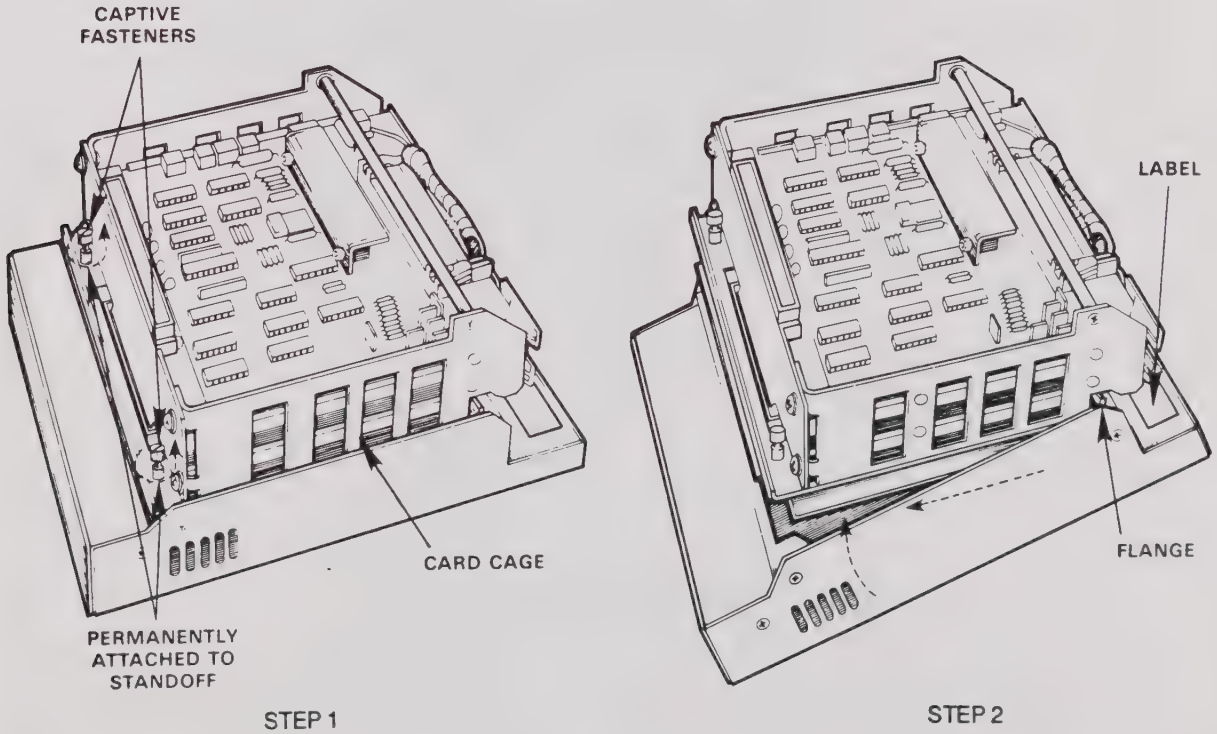


Figure 1. UniPak 2/2B Disassembly (UniPak 2 shown)

5. Lift the card cage up and out of its top cover until you can see the socketboard interconnect cable (see figure 2). Do not detach the socketboard interconnect cable.

6. Turn the card cage over and set it on the flat surface next to the top cover. This step exposes the armite or mylar shield which covers the memory board.

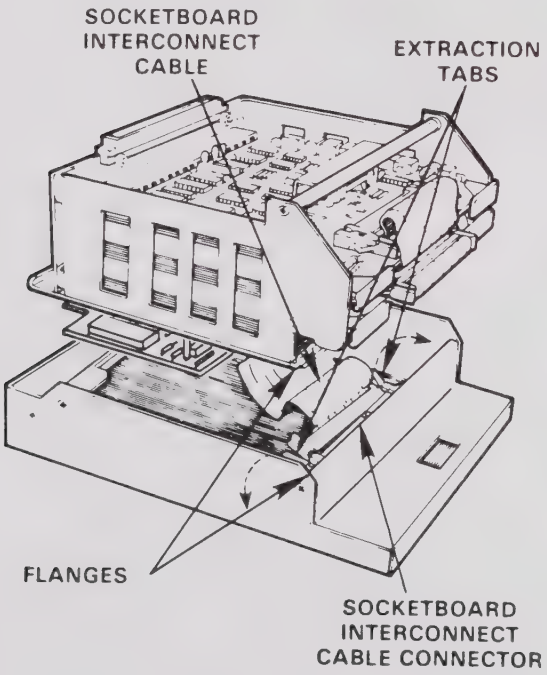


Figure 2. Socketboard Interconnect Cable

7. Remove the two Phillips-head screws and armite or mylar shield from the memory board (see figure 3). Retain the washers and screws for reassembly. (If you are updating a UniPak 2B that was factory built, rather than a field conversion, it will not contain any washers.)

8. Pull the memory board straight up to unplug it from the card edge connector (as shown in figure 3).

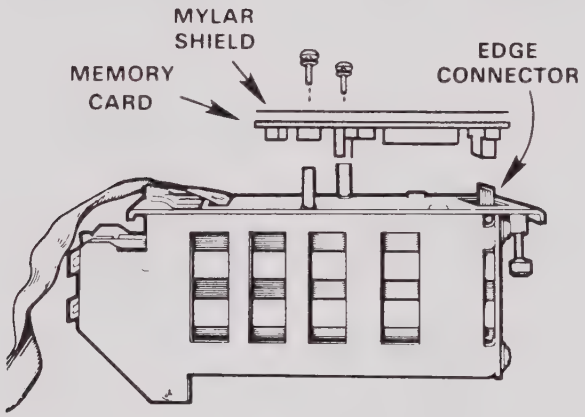


Figure 3. Memory Board Removal

9. Turn the 701-2126 memory board over so the component side faces up (figure 4) in preparation for firmware installation.

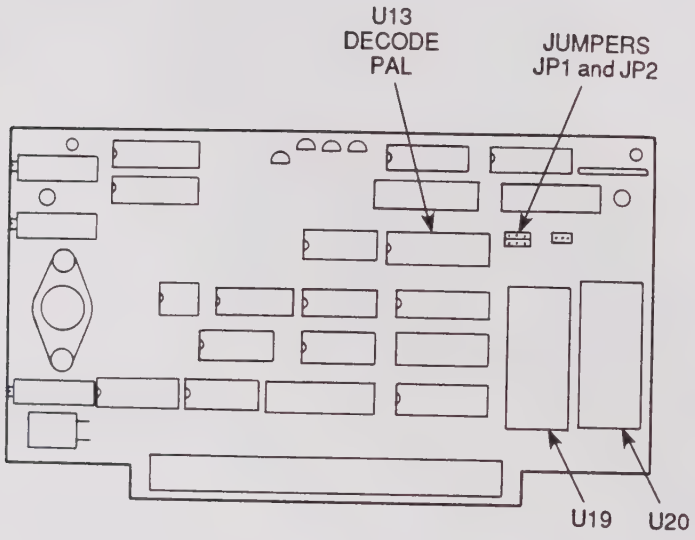


Figure 4. Update Component Location

Firmware Installation

The following steps describe how to install the firmware components of the update kit into your disassembled UniPak 2/2B. Follow the procedures in the order that they are presented here.

CAUTION

The software update kit EPROMs are static-sensitive. Perform the following procedures at a static-free work station to prevent static-related damage to the EPROM(s).

1. Remove EPROMs U19, U20 and decode PAL U13 (see figure 4) from the memory board using the IC extractor tool or the small slot-head screwdriver.

NOTE

Prior to installing the firmware, check the socket contacts to ensure that they are not damaged. If any socket contact is damaged, repair or replace that part before proceeding with the firmware installation.

2. Install the software update kit Decode PAL U13 in memory board socket U13. Refer to table 1 for software update kit firmware part numbers and their corresponding installation locations.

WARNING

When installing EPROM(s) be sure to bottom justify them in the socket (figure 5).

3. Install the software update kit EPROMs U19 and U20 in sockets U19 and U20, respectively. Refer to table 1 for software update kit component part numbers and their corresponding installation locations.

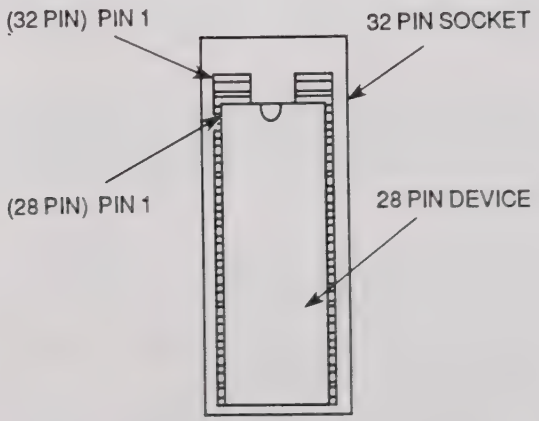


Figure 5. EPROM Installation Alignment

UniPak 2/2B Reassembly and Testing

Reassembly of the UniPak 2/2B is performed by reversing the disassembly procedures. Follow the steps listed below and refer to figures 1 through 3 on the previous pages.

1. Plug the memory board into its card cage edge connector (figure 3) until it is firmly seated.

2. Replace the armite or mylar shield, washers (if included) and two Phillips-head screws.

3. Reinsert the card cage into the top cover with the memory board facing into the top cover (figure 2). Tilt the card cage up and push gently forward to lock the top cover's flange between the card cage's top and bottom flanges (figure 1b). Then gently set the card cage back into the top cover.

4. Using the medium size slot-head screwdriver, tighten the captive fastener slot screws finger tight.

5. Perform a self-test on the UniPak 2/2B by installing it in a programmer and applying power.

   If the programmer fails to power up correctly, or the self-test message is not displayed, check to make sure that all of the software update kit installation procedures (and conversion kit installation procedures, if you are installing the conversion kit) were performed correctly. If the self-test fails again, contact your local Data I/O Service Center for assistance.

6. Verify the correct firmware configuration/version number by pressing `SELECT E F START` on the programmer's keyboard. Check the programmer display for the four-character configuration number and the version number. See the bottom of table 1 on the first page of this document for the correct configuration and version numbers.

   If the correct configuration and version numbers are not displayed, the firmware has not been installed correctly. Check to make sure that all installation procedures were performed correctly. Make sure that all PROMs are fully inserted into their sockets and are making proper contact at their connections. Install the UniPak 2/2B in a programmer and again press `SELECT E F START`. If the configuration/version number displayed still does not match that listed in table 1, contact your local Data I/O Service Center for assistance.

   If the configuration/version number listed in table 1 is displayed, then the update kit firmware installation is complete.

7. Using an indelible ink pen, write the serial number of your unit on the serial number label provided. Affix the enclosed label over the existing label on the back side of the front panel. The UniPak 2 label location is shown in figure 1b. The UniPak 2B label is located on the vertical surface facing the indicated UniPak 2 label location.

   If you are installing a UniPak 2 to 2B conversion kit, complete the conversion kit installation at this time, starting with the subsection Testing the UniPak 2B.

   If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete that section before doing the acceptance test.

   If you are updating a UniPak 2B, an acceptance test was included in the user note. If you want to re-accept the UniPak 2B after updating it, perform the acceptance test procedures as directed in the enclosed acceptance test manual.

UNIPAK 2/2B™

Hardware Update Kit

985-0051-001 *JULY 87*

Data I/O has made every attempt to ensure that the information in this document is accurate and complete. However, Data I/O assumes no liability for errors, or for any damages that result from use of this document or the equipment that it accompanies.

Data I/O reserves the right to make changes to this document without notice at any time.

ORDERING INFORMATION

When ordering this manual, use Part Number 985-0051-001.
Applies to: Engineering part numbers 951-0045-001 and up.

UniPak 2™ and UniPak 2B™ are trademarks of Data I/O Corporation.

Copyright Data I/O Corporation, 1987. All rights reserved.

INTRODUCTION

WARNING

The procedures described in this document are intended for use only by personnel qualified to service electronic equipment. Do not attempt to perform these procedures unless you are qualified to do so. Minor calibration is required to install this kit. If you do not wish to do this yourself, return the kit and the UniPak 2/2B to a Data I/O service center for installation.

This manual provides the hardware update instructions necessary for installing the memory board in either the UniPak 2 or the UniPak 2B. This hardware update kit will also require either the UniPak 2 software update kit (953-0002) if the unit is remaining a UniPak 2, or the UniPak 2B software update kit (953-0017) if the unit is a UniPak 2B or is being converted to a UniPak 2B. The parts included in the hardware update kit are listed in table 1 below:

Table 1. Software Update Kit Parts

Description	Quantity	Data I/O Part No.	Installation Location
Memory Board	1	701-2126	
Calibration Resistor	1	103-2024	

CAUTION

The hardware update kit is static-sensitive. Observe standard handling precautions, such as performing the update kit procedures at an anti-static workstation or wearing a grounded wrist-strap, otherwise, damage to the PAL(s) may result.

UNIPAK 2/2B HARDWARE UPDATE KIT INSTALLATION

The following paragraphs describe how to install the hardware update kit. You will need the following tools for installation of the kit:

- One Phillips-head screwdriver (medium size, #1 or #2)
- One slot-head screwdriver (medium size)
- One slot-head screwdriver (small size)

NOTE

If you are also installing a UniPak 2 to 2B conversion kit , begin installing the conversion kit first. When the conversion kit instructions direct you to install the software and/or hardware update kit:

1. *Go to step 6 of the following subsection, complete the instructions and then go directly to the firmware installation subsection of the Software Update Kit manual.*

2. *Complete the software update kit installation as directed.*

3. *After completing the software update kit installation, proceed to Testing the UniPak 2B subsection of the Conversion Kit Manual if the conversion kit is being installed and complete the conversion kit installation.*

4. *After completing the software update kit installation and the conversion kit installation, if installed, go to the calibration section of the Hardware Update Kit manual.*

UniPak 2/2B Disassembly

To disassemble the UniPak 2/2B for installation of the new memory board, follow the procedures listed below.

1. Remove the UniPak 2/2B from the programmer, if it is installed.
2. Set the UniPak 2/2B face down on the flat surface of a static-free work station.
3. Using the medium size slot-head screwdriver, unscrew the captive fasteners (figure 1, step 1) until they hang loosely; the fasteners will not separate from their standoffs.
4. Lift the card cage up slightly, then pull out (as shown in figure 1, step 2) to unlock the flanges.

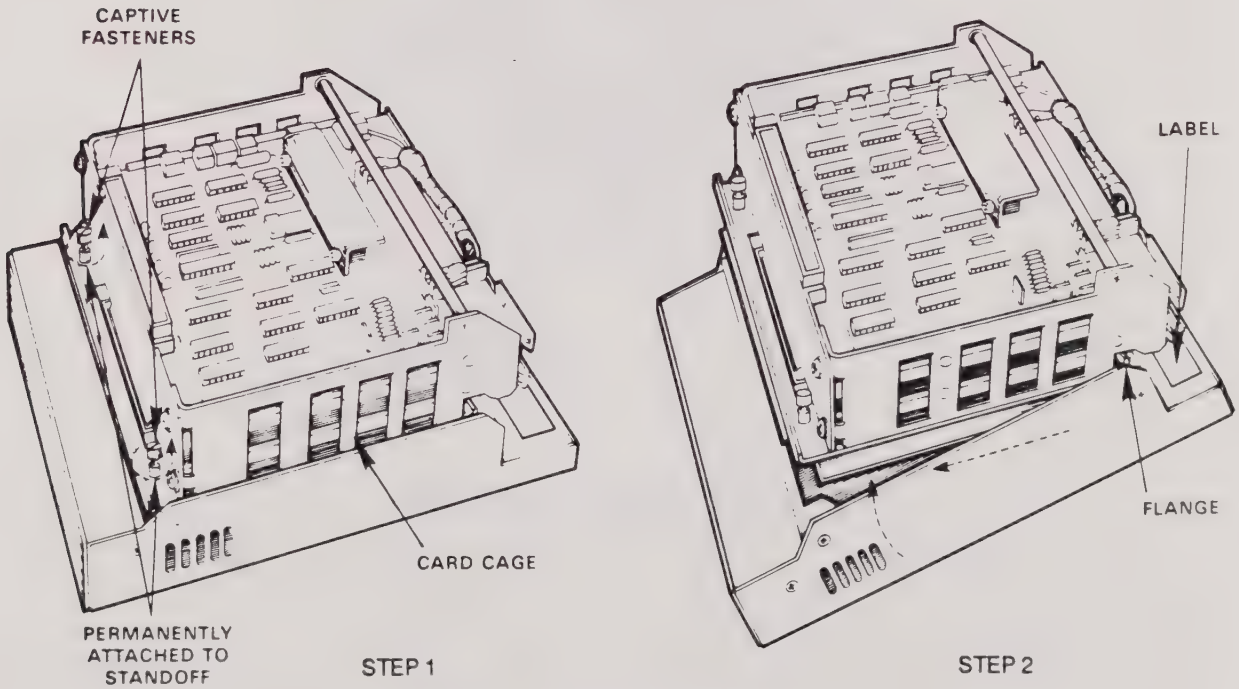


Figure 1. UniPak 2/2B Disassembly (UniPak 2 shown)

5. Lift the card cage up and out of its top cover until you can see the socketboard interconnect cable (figure 2). Do not detach the socketboard interconnect cable.

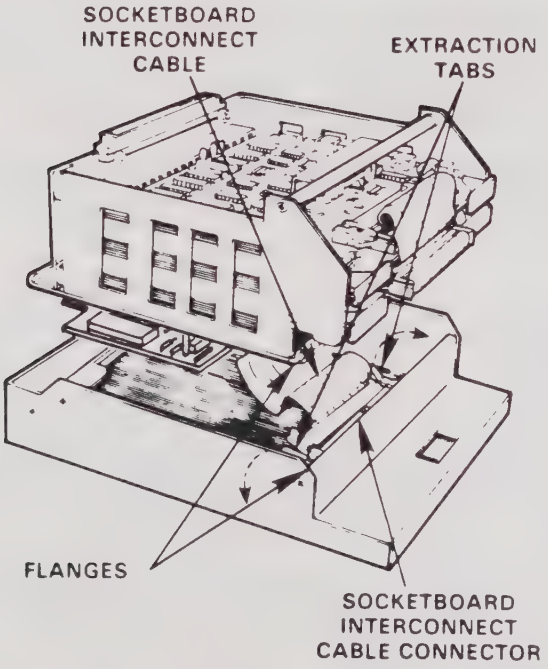


Figure 2. Socketboard Interconnect Cable (UniPak 2 shown)

6. Turn the card cage over and set it on the flat surface next to the top cover. This step exposes the armite or mylar shield which covers the memory board.

7. Remove the two Phillips-head screws and armite or mylar shield from the memory board (figure 3). Retain the washers and screws for reassembly. (If you are updating a UniPak 2B that was factory built, rather than a field conversion, it will not contain any washers.)

8. Pull the old memory board straight up to unplug it from the card edge connector (as shown in figure 3), and discard it.

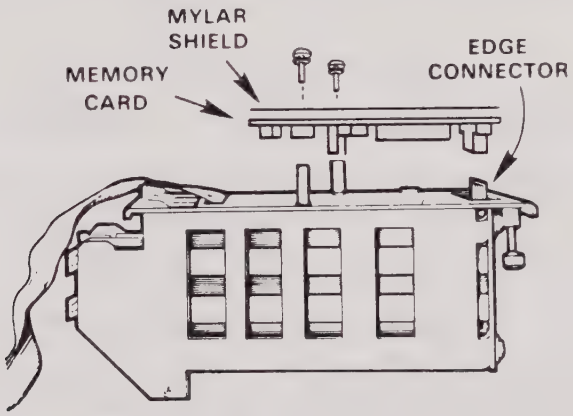


Figure 3. Memory Board Removal

9. Set the 701-2126 memory board so the component side faces up (figure 4) in preparation for the Software Update Kit installation.

CAUTION

The Software Update Kit is static sensitive. Observe standard handling precautions, such as performing the procedures at an anti-static workstation and wearing a grounded wrist-strap; otherwise, damage to the devices may result.

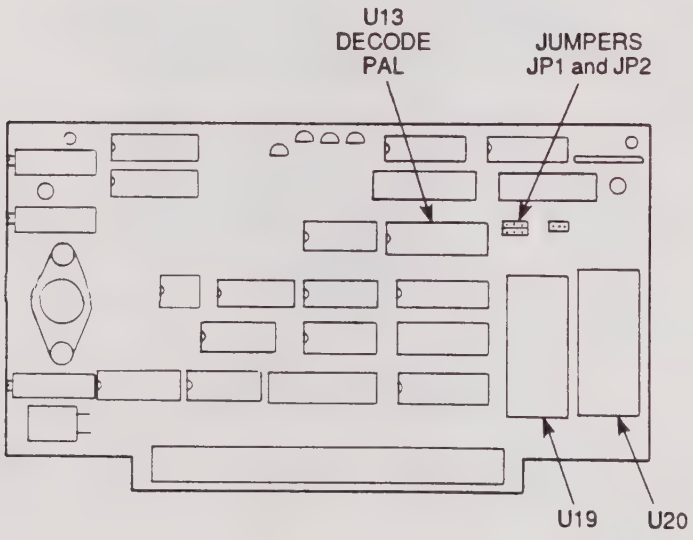


Figure 4. Update Component Location

10. Go to the Firmware Installation subsection of the Software Update Kit manual and complete the firmware installation there. IC INSTALLED ON BOARD

11. When firmware instructions are complete, go to Testing the UniPak 2B subsection of the Conversion Kit manual if installed, complete instructions there, and go to calibration section below when instructed to do so. If no Conversion Kit was installed, complete calibration section below before doing the optional acceptance test procedure.

CALIBRATION

WARNING

If you do not wish to do this youself, return the kit and the UniPak 2/2B to a Data I/O service center for installation.

The new memory board was tested and pre-calibrated at the factory before it was shipped to you, but the steps in the calibration procedure must be performed with the new board installed in its new host UniPak 2/2B and programmer to insure optimum performance.

1. Remove the UniPak 2/2B from the programmer, if it is installed.
2. Set the UniPak 2/2B face down on the flat surface of a static-free workstation.
3. Using the medium size slot-head screwdriver, unscrew the captive fasteners (figure 1, step 1) until they hang loosely; the fasteners will not separate from their standoffs.
4. Lift the card cage up slightly, then pull out (shown in figure 1, step 2) to unlock the flanges.
5. Install the UniPak 2 or 2B in the programmer as shown in figure 5.
6. Place the bag the memory board came in between the memory board and the front panel to prevent contact between the memory board and the front panel (as shown in figure 5).

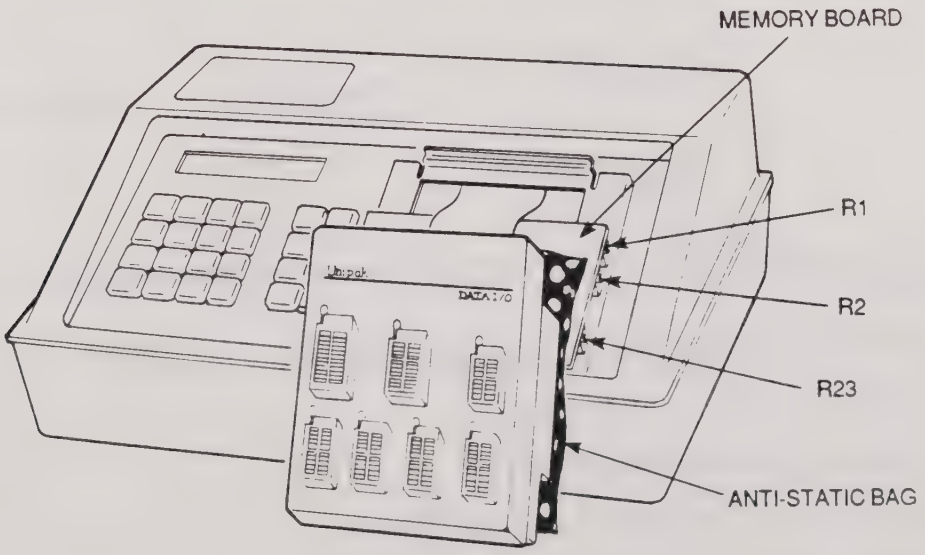


Figure 5. Memory Board Position for Calibration

7. Power up the base machine.

8. Using the 20V scale on the DMM, connect common to pin 12 of socket 1 on the UniPak 2B, or socket 2 on the UniPak 2. Connect the other lead to pin 8 of socket 1 on the UniPak 2B or socket 2 on the UniPak 2.

9. Enter calibration step 01 per table 2 to adjust R23 on the new memory board until the meter reads 15.0 V.

Table 2. Key Sequence to Access the Calibration Mode

Programmer System	Enter Calibration Mode	Key Sequence To: Increment Step No.	Decrement Step No.
19	Press SELECT Press C2 Press ENTER Enter Step Number Press Start	Press ENTER	Press REVIEW
29A/29B	Press SELECT Press C1 Press START Enter Step Number Press Start	Press START	Press REVIEW
100A	Press SELECT Press 12 Enter Step Number Press Start	Press START	Press BACKSPACE

10. Disconnect meter lead from pin 8, set meter to 200 mA scale and set up meter for current measurements.

11. Insert a 100Ω resistor in pin 9 of socket 1 on the UniPak 2B or socket 2 on the UniPak 2.

12. Press START twice, the display should read 03.

13. Connect meter lead to free end of the resistor.

14. Adjust R2 on the new memory board until meter reads 20.0 mA.

15. Press START once, display should read 04.

16. Adjust R1 on the new memory board until the meter reads 120.0 mA.

17. Exit calibration, hit any blue key on the 29A, 29B, 100A, select C0 on the System 19.

18. Power down the programmer.

19. Reinsert the card cage into the top cover with the memory board facing into the top cover (figure 1, page 3). Tilt the card cage up and push gently forward to lock the top cover's flange between the card cage's top and bottom flanges (figure 2). Then gently set the card cage back into the top cover.

20. Using the medium size slot-head screwdriver, tighten the captive fastener slot screws finger tight.

21. Perform the optional acceptance test procedure for the UniPak 2B.

Done 7-12-87

UNIPAK 2/2B™

Software Update Kit

985-0002-008 *JULY 87*

Data I/O has made every attempt to ensure that the information in this document is accurate and complete. However, Data I/O assumes no liability for errors, or for any damages that result from use of this document or the equipment that it accompanies.

Data I/O reserves the right to make changes to this document without notice at any time.

ORDERING INFORMATION

When ordering this manual, use Part Number 985-0002-008.
Applies to: Engineering part numbers 953-0002-014 and up
and 953-0017-008 and up.

UniPak 2™ and UniPak 2B™ are trademarks of Data I/O Corporation.

Copyright Data I/O Corporation, 1987. All rights reserved.

INTRODUCTION

WARNING

The procedures described in this document are intended for use only by personnel qualified to service electronic equipment. Do not attempt to perform these procedures unless you are qualified to do so.

This manual provides the software update instructions necessary for updating either the UniPak 2 or the UniPak 2B. The parts included in each of the update kits are listed in table 1 below:

Table 1. Software Update Kit Parts

Type of Kit	Description	Quantity	Data I/O Part No.	Installation Location
UniPak 2	EPROM	1	324-0059-031	U19
	EPROM	1	324-0059-032	U20
	Decode PAL	1	324-1760-003	U13
	Label	1	--	
	UniPak 2 Operator's Manual	1	981-0001	
	UniPak 2 User Notes	1	984-0001	
UniPak 2B	EPROM	1	324-0059-031	U19
	EPROM	1	324-0059-032	U20
	Decode PAL	1	324-1760-003	U13
	Label	1	--	
	UniPak 2B Device List	1	984-0179	
	UniPak 2B Acceptance Test	1	984-0179	
	UniPak 2B User Notes	1	984-0179	

Firmware Configuration/Version Number: 0F36 VER 13.0

CAUTION

The software update kit EPROMs are static-sensitive. Observe standard handling precautions, such as performing the update kit procedures at an anti-static workstation or wearing a grounded wrist-strap, otherwise, damage to the EPROM(s) may result.

UNIPAK 2/2B SOFTWARE UPDATE KIT INSTALLATION

The following paragraphs describe how to install the software update kit. You will need the following tools for installation of the kit:

- One Phillips-head screwdriver (medium size, #1 or #2)
- One slot-head screwdriver (medium size)
- IC extractor tool, or small slot-head screwdriver

For the Software Update Kit to work, your UniPak 2/2B must have a 701-2126 Memory Board. To determine if your pak has the correct memory board, perform the following steps:

1. Install the UniPak 2/2B in the programmer and turn the programmer on.

2. Press SELECT. Type EF on the programmer keyboard and then press START.

If the display does not show version 13.0 or greater, the new Memory Board must be installed. A hardware update kit (951-0045) is required.

NOTE

If you are only installing the Software Update Kit, go directly to the UniPak 2/2B Disassembly section on the following page.

If you are not installing the Conversion Kit, but are installing the Hardware Update Kit, go to UniPak 2/2B Disassembly section of the Hardware Update Kit manual complete the instructions and when instructed to do so, go to the Firmware Installation section in this manual.

If you are installing a UniPak 2 to 2B Conversion Kit and/or the Hardware Update Kit, begin installing the conversion kit first. When the conversion kit instructions direct you to install the software and/or hardware update kit:

1. *Go to step 6 of the Hardware Update Kit manual if you are installing a new memory board, complete the instructions and then go directly to the Firmware Installation section in this manual, otherwise go directly to the Firmware Installation section in this manual.*

2. *Complete the software update kit installation as directed in the Firmware Installation section of this manual.*

3. *After completing the software update kit installation, proceed to the Testing the UniPak 2B section of the converstion kit manual and complete the conversion kit installation, if the conversion kit was installed.*

4. *If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete the installation there.*

UniPak 2/2B Disassembly

To disassemble the UniPak 2/2B for installation of the updated firmware, follow the procedures listed below.

1. Remove the UniPak 2/2B from the programmer, if it is installed.
2. Set the UniPak 2/2B face down on the flat surface of a static-free workstation.
3. Using the medium size slot-head screwdriver, unscrew the captive fasteners (figure 1, step 1) until they hang loosely; the fasteners will not separate from their standoffs.
4. Lift the card cage up slightly, then pull out (as shown in figure 1, step 2) to unlock the flanges.

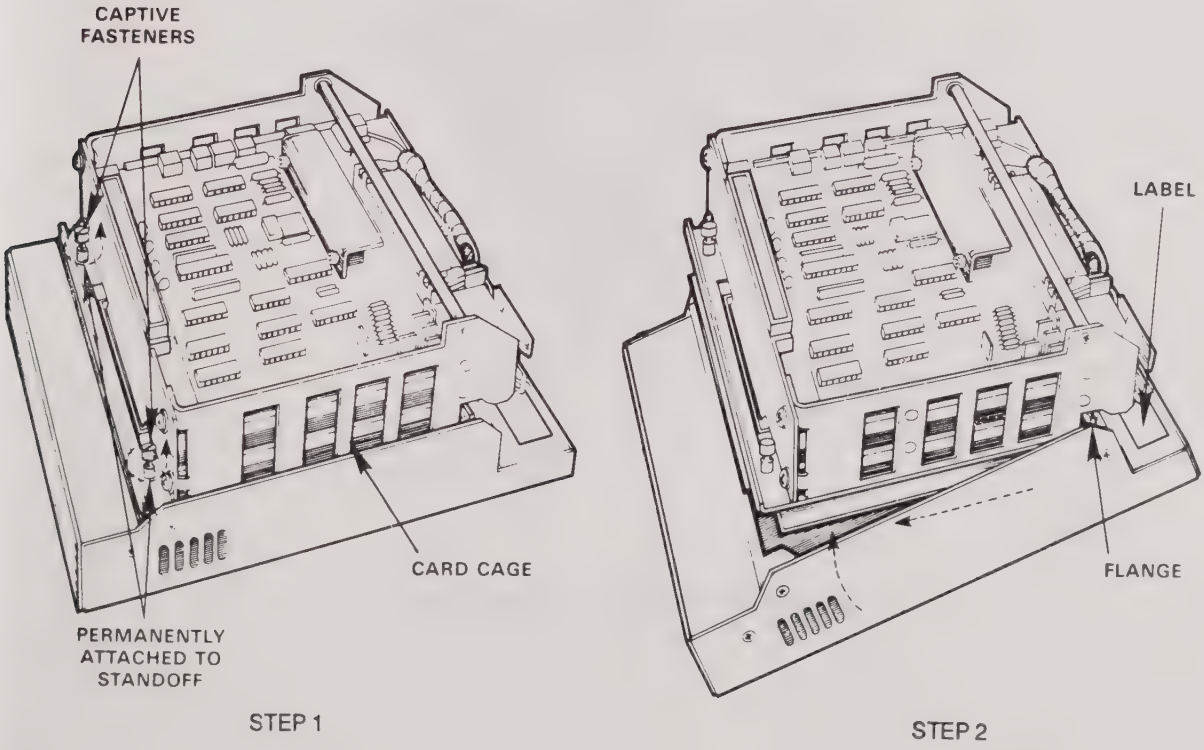


Figure 1. UniPak 2/2B Disassembly (UniPak 2 shown)

5. Lift the card cage up and out of its top cover until you can see the socketboard interconnect cable (see figure 2). Do not detach the socketboard interconnect cable.

6. Turn the card cage over and set it on the flat surface next to the top cover. This step exposes the armite or mylar shield which covers the memory board.

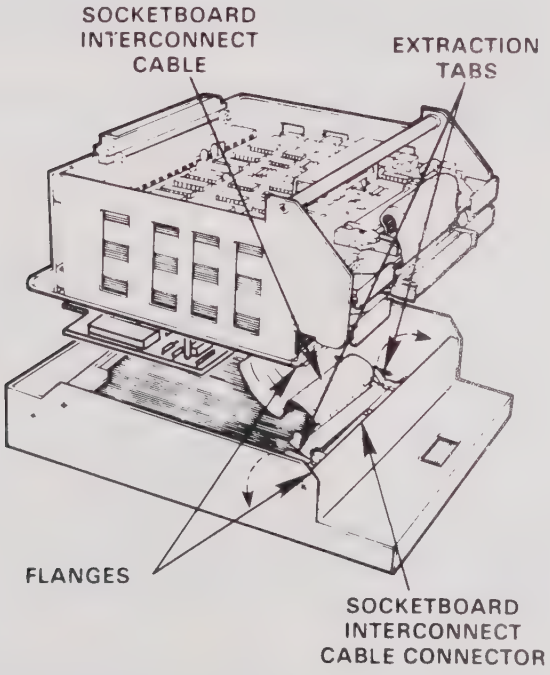


Figure 2. Socketboard Interconnect Cable

7. Remove the two Phillips-head screws and armite or mylar shield from the memory board (see figure 3). Retain the washers and screws for reassembly. (If you are updating a UniPak 2B that was factory built, rather than a field conversion, it will not contain any washers.)

8. Pull the memory board straight up to unplug it from the card edge connector (as shown in figure 3).

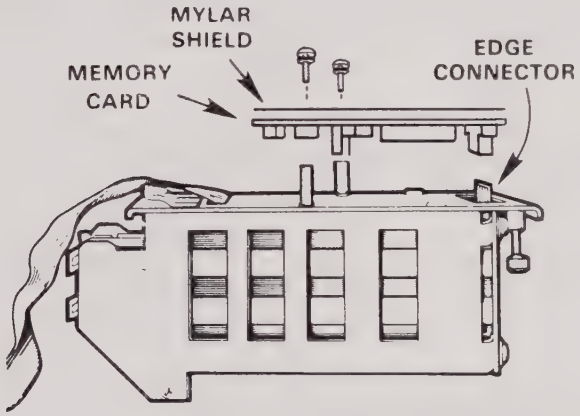


Figure 3. Memory Board Removal

9. Turn the 701-2126 memory board over so the component side faces up (figure 4) in preparation for firmware installation.

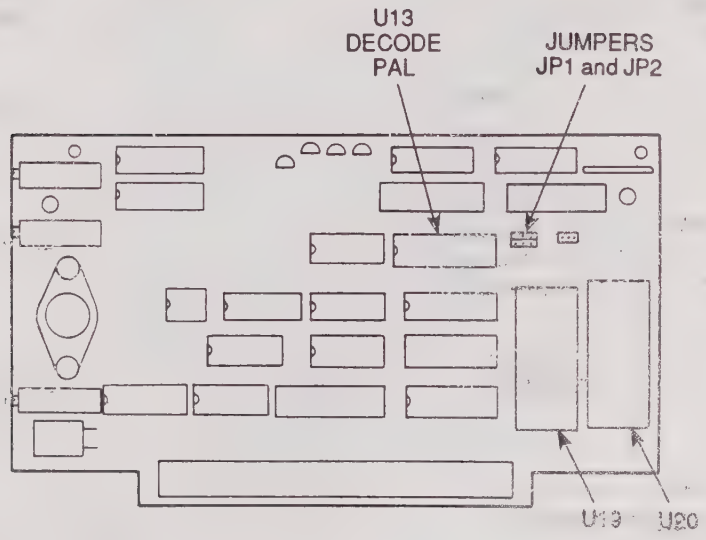


Figure 4. Update Component Location

Firmware Installation

The following steps describe how to install the firmware components of the update kit into your disassembled UniPak 2/2B. Follow the procedures in the order that they are presented here.

CAUTION

The software update kit EPROMs are static-sensitive. Perform the following procedures at a static-free work station to prevent static-related damage to the EPROM(s).

1. Remove EPROMs U19, U20 and decode PAL U13 (see figure on previous page) from the memory board using the IC extractor tool or the small slot-head screwdriver.

NOTE

Prior to installing the firmware, check the socket contacts to ensure that they are not damaged. If any socket contact is damaged, repair or replace that part before proceeding with the firmware installation.

2. Install the software update kit Decode PAL U13 in memory board socket U13. Refer to table 1 for software update kit firmware part numbers and their corresponding installation locations.

WARNING

When installing EPROM(s) be sure to bottom justify them in the socket (figure 5).

3. Install the software update kit EPROMs U19 and U20 in sockets U19 and U20, respectively. Refer to table 1 for software update kit component part numbers and their corresponding installation locations.

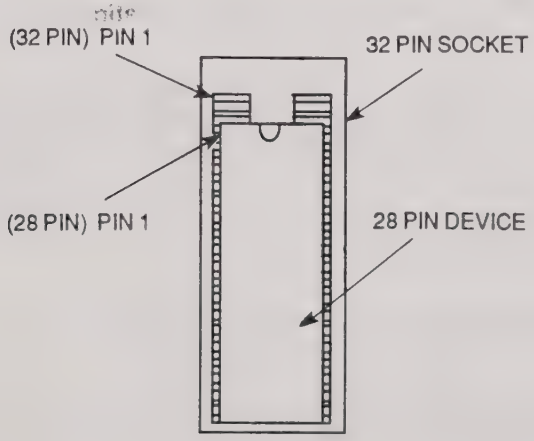


Figure 5. EPROM Installation Alignment

UniPak 2/2B Reassembly and Testing

Reassembly of the UniPak 2/2B is performed by reversing the disassembly procedures. Follow the steps listed below and refer to figures 1 through 3 on the previous pages.

1. Plug the memory board into its card cage edge connector (figure 3) until it is firmly seated.

2. Replace the armite or mylar shield, washers (if included) and two Phillips-head screws.

3. Reinsert the card cage into the top cover with the memory board facing into the top cover (figure 2). Tilt the card cage up and push gently forward to lock the top cover's flange between the card cage's top and bottom flanges (figure 1b). Then gently set the card cage back into the top cover.

4. Using the medium size slot-head screwdriver, tighten the captive fastener slot screws finger tight.

5. Perform a self-test on the UniPak 2/2B by installing it in a programmer and applying power.

   If the programmer fails to power up correctly, or the self-test message is not displayed, check to make sure that all of the software update kit installation procedures (and conversion kit installation procedures, if you are installing the conversion kit) were performed correctly. If the self-test fails again, contact yur local Data I/O Service Center for assistance.

6. Verify the correct firmware configuration/version number by pressing `SELECT E F START` on the programmer's keyboard. Check the programmer display for the four-character configuration number and the version number. See the bottom of table 1 on the first page of this document for the correct configuration and version numbers.

   If the correct configuration and version numbers are not displayed, the firmware has not been installed correctly. Check to make sure that all installation procedures were performed correctly. Make sure that all PROMs are fully inserted into their sockets and are making proper contact at their connections. Install the UniPak 2/2B in a programmer and again press `SELECT E F START`. If the configuration/version number displayed still does not match that listed in table 1, contact your local Data I/O Service Center for assistance.

   If the configuration/version number listed in table 1 is displayed, then the update kit firmware installation is complete.

7. Using an indelible ink pen, write the serial number of your unit on the serial number label provided. Affix the enclosed label over the existing label on the back side of the front panel. The UniPak 2 label location is shown in figure 1b. The UniPak 2B label is located on the vertical surface facing the indicated UniPak 2 label location.

   If you are installing a UniPak 2 to 2B conversion kit, complete the conversion kit installation at this time, starting with the subsection Testing the UniPak 2B.

   If a hardware update kit was installed, go to the calibration section of the Hardware Update Kit manual and complete that section before doing the acceptance test.

   If you are updating a UniPak 2B, an acceptance test was included in the user note. If you want to re-accept the UniPak 2B after updating it, perform the acceptance test procedures as directed in the enclosed acceptance test manual.

What's Changed in Version 20.0

* Support for 4Kb PROM in 24-pin DIP: **Harris** 6641/2
* Support for 16Kb PROM in 24-pin DIP: **Cypress** 7C291A; **Harris** 6616/7
* Support for 512Kb EEPROM in 32-pin DIP: **Seeq** 48F512
* Support for 1Mb EEPROM in 32-pin DIP: **Seeq** 48F010
* Support for 16Kb micro in 24-pin DIP: **Signetics** 87C751

Attention: Owners of UniPak 2 Versions 1.0 thru 12.0

If you own a UniPak 2 (not 2B) version 1.0 thru 12.0 (purchased before 1986), you do not have the current *UniPak 2 Operator Manual* (that was released with version 13.0). Since you are now updating your UniPak 2 to version 20.0, you will find it helpful to have a copy of this current manual. Contact your local **Data I/O** sales representative for further information. Be sure to have the serial number of your UniPak 2 available when you call. To locate the serial number, remove your UniPak from the mainframe, and look for a label at the top of the reverse side.

Attention: Owners of Model 29B Versions 1.0 thru 5.0

If you run your UniPak 2/2B on an old Model 29B mainframe versions 1.0 thru 5.0 (purchased before 1988), you will not be able to program 23 (50%) of the new devices that were added to UniPak 2/2B version 20.0 because they use three-digit family/pinout codes (that were added in the Model 29B version 6.0). You can upgrade your old Model 29B mainframe to version 6.0 with a user-installable update kit. Contact your local **Data I/O** sales representative for further information.

12-13-89

Attention: Owners of Models 17, 19, 100A, or 29A

If you run your UniPak 2/2B on an obsolete Model 17, 19, 100A or 29A mainframe, you will not be able to program 23 (50%) of the new devices that were added to UniPak 2/2B version 20.0 because they use three-digit family/pinout codes (that are only supported by the Model 29B version 6.0). You can move up to the current Model 29B mainframe at a substantial discount by trading in your obsolete mainframe. Contact your local **Data I/O** sales representative for further information.

DATA I/O Corporation
10525 Willows Road NE, Redmond, WA 98073-9746
Phone 206-881-6444, Telex 15-2167, FAX 206+882-1043

CUSTOMER SERVICE LETTER

PRODUCT: UniPak 2/2B

DATE: 1 December 1989

AUTHOR: Leo Nikora

NUMBER: 983-0025-006

UniPak 2/2B Version 20.0

Version 20.0 of the UniPak 2 and 2B for use with the Models 17, 19, 100A, 29A, and 29B mainframes gives you support for 46 new programmable memory devices, increasing the total number of devices supported by the UniPak to 1,386!

What's New in Version 20.0

- Support for 1Kb PROM in 16-pin PLCC: **Signetics** 82S129
- Support for 2Kb PROM in 16-pin DIP: **Signetics** 82US23
- Support for 8Kb PROM in 28-pin PLCC: **Signetics** 82S183
- Support for 16Kb PROM in 28-pin DIP: **AMD** 27C45
- Support for 16Kb EEPROM in 32-pin PLCC: **Xicor** 2816A
- Support for 16Kb EEPROM in 32-pin LCC: **Xicor** 2816A/B
- Support for 32Kb PROM in 24-pin DIP: **AMD** 27C43; **Raytheon** 29771/SM, 29773/SM
- Support for 64Kb PROM in 24-pin LCC: **Raytheon** 29791/DM, 29793/DM
- Support for 64Kb EPROM in 32-pin LCC: **Fujitsu** 27C64
- Support for 64Kb EEPROM in 32-pin PLCC and LCC: **Xicor** 2864B
- Support for 128Kb EPROM in 32-pin LCC: **Fujitsu** 27C128
- Support for 256Kb EPROM in 28-pin DIP: **SGS** 27C256B, 87C257; **TI** 87C257
- Support for 256Kb PEROM in 28-pin DIP: **Atmel** 29C256
- Support for 256Kb EPROM in 32-pin LCC: **AMD** 27C256; **Fujitsu** 27C256A
- Support for 256Kb EEPROM in 28-pin DIP: **Samsung** 28C256
- Support for 512Kb EPROM in 28-pin DIP: **AMD** 28F512-P1; **Atmel** 27C512R; **SGS** 27C512
- Support for 512Kb EPROM in 32-pin DIP: **Seeq** 47F512
- Support for 1Mb EPROM in 32-pin DIP: **AMD** 27C100; **SGS-Thomson** 27C1000/1
- Support for 1Mb EPROM in 32-pin PLCC: **Fujitsu** 27C1001; **Mitsubishi** 27C101
- Support for 1Mb EPROM in 40-pin DIP: **Intel** 27C213; **Wafer Scale** 27C210L
- Support for 1Mb EPROM in 44-pin PLCC: **Intel** 27960; **Wafer Scale** 27C210L
- Support for 1Mb EPROM in 44-pin JLCC: **Intel** 27960
- Support for 1Mb EEPROM in 32-pin DIP: **Atmel** 28MC010; **Xicor** 28C010
- Support for 2Mb EPROM in 32-pin DIP: **Mitsubishi** 27C201
- Support for 2Mb EPROM in 40-pin DIP: **Mitsubishi** 27C202
- Support for 32Kb micro in 44-pin JLCC: **Signetics** 87C51

DATA I/O Corporation
10525 Willows Road NE, Redmond, WA 98073-9746
Phone 206-881-6444, Telex 15-2167, FAX 206+882-1043

DATA I/O

10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444 Telex 15-2167